# Dead-Zone Digital Controller for Improved Dynamic Response of Power Factor Preregulators

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*Abstract* – **This paper presents a simple control method for improvement of dynamic responses in a digitally controlled low-harmonic rectifier with power factor correction (PFC). The controller uses a fixed or self-adjusting dead zone in analog-to-digital conversion to eliminate the output capacitor ripple from the voltage control loop. The proposed control methods are tested in a completely digitally controlled 200 W boost PFC operating at 200 kHz switching frequency. Experimental results show that the simple controller implementation results in low current harmonics and significantly improved output voltage transient responses.**

## I. INTRODUCTION

Digital control of switching power converters is becoming more and more common not only in high-power, low-frequency applications but also in low-to-medium power, high-frequency applications including dc-dc converters, and single-phase universal-input power factor correctors (PFC).

Recent publications [1-8] have shown completely digitally controlled PFCs with performance comparable to state of the art analog realizations. Moreover, digital controller implementation can lead to a number of advantages including a reduction in the number of passive components, programmability and improved dynamic responses [1,4,6,7]. In low-to-medium power applications, the key objective in successful realizations of digital controllers is to achieve system improvements without penalties in system complexity or cost.

Figure 1 shows a block diagram of a digitally controlled PFC rectifier. Switching converter is controlled by two loops: an inner, current loop that forces the input current $i_g(t)$ to follow the rectified input voltage waveform $v_g(t)$ according to:

$$i_g(t) = \frac{v_g(t)}{R_e} = k v_g(t) \qquad (1)$$

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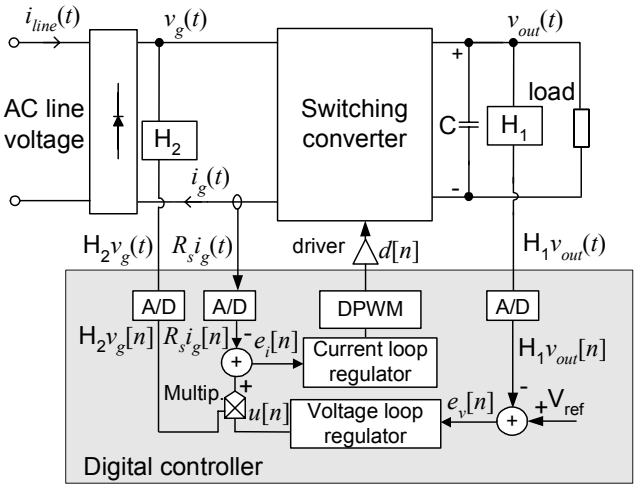


Fig.1. Block diagram of a digitally controlled PFC rectifier.

and an outer voltage loop that changes the value $k$ (i.e. the emulated resistance $R_e$) to regulate the output voltage.

In order to maintain low distortion of the input current, the change of the emulated resistance must not be influenced by the output capacitor ripple at even harmonics of the line frequency [9,10]. In conventional designs, the elimination of the even harmonics of the line frequency from the voltage loop is accomplished by closing the voltage loop at a low frequency (usually 10-20 Hz), which is significantly lower than the frequency of the second line harmonic. As a result, the dynamic response of the low-bandwidth voltage controller is poor and over-design of the power stage and a downstream DC-DC converter may be required to account for increased voltage overshoots and dips during transients.

A number of analog and digital methods for improvement of voltage loop characteristics have been presented [1,4,8,11-14]. In all of these methods, additional analog or digital processing is performed, which requires more complicated hardware for implementation.

Relatively simple analog control methods based on an error amplifier that has a gain dependent on the amplitude of the

error signal have been presented in [11,14]. In steady state, when the error is small, the error-amplifier gain is small and the output voltage ripple component does not significantly affect operation of the current loop. In transients, when the error is large, the gain of the error amplifier is increased to improve the response speed. The "dead-zone" digital controller proposed in this paper is based on a similar idea. The implementation includes only a simple modification of the analog-to-digital converter characteristic and does not require any additional hardware or processing.

The paper is organized as follows: the control method based on a dead zone in analog-to-digital conversion is presented in Section II. Section III describes the voltage regulator design. An adaptive adjustment of the dead zone, which results in improved static voltage regulation, is presented in Section IV. Experimental results obtained from a digitally controlled boost PFC prototype are presented in Section V.

## II. DEAD-ZONE CONTROL METHOD

In a properly operating PFC rectifier, the difference between the instantaneous input power and the constant output load power $P_{load}$ causes the output capacitor voltage ripple at twice the line frequency $f_{line}$. The peak-to-peak amplitude of this voltage ripple $\Delta v_c$ is approximately [10]:

$$2\Delta v_C \approx \frac{P_{load}}{\omega C V_{out}} \tag{2}$$

where $C$ is the output capacitance value, $V_{out}$ is the DC output voltage and $\omega=2\pi f_{line}$. The maximum value of this ripple is one of the design constraints that determines the value of the output capacitor. In the dead-zone control method, the maximum ripple amplitude is also used to set the resolution of the analog-to-digital converter for the output voltage sensing.

Figure 2 shows a block diagram of the digital voltage loop regulator based on the dead-zone approach. The attenuated output voltage $H_1 v_{out}(t)$, which can be written as a sum of its DC value and ripple component:

$$H_1 v_{out}(t) = H_1 V_{out} + H_1 v_{ripple}(t) \tag{3}$$

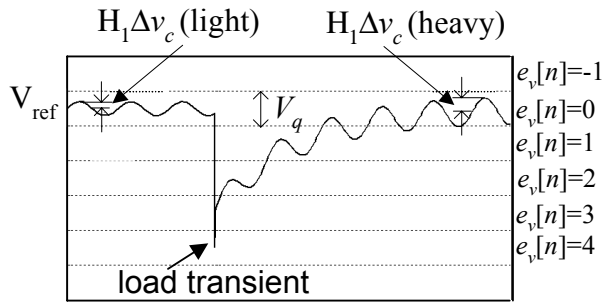


Fig.3 Variation of the output voltage around the reference value during a load transient for the properly selected resolution of the analog-to-digital converter in a dead-zone controller.

is sampled and measured each $T_s=1/f_{vs}$ seconds, where $f_{vs}$ is the output voltage sampling frequency. Sampled and converted value $H_1 v_{out}[n]$ is compared with the reference value $V_{ref}$ and the resulting output voltage error signal is processed by the voltage loop regulator. The output of the voltage loop regulator $u[n]$ is multiplied by a value proportional to the input voltage $H_1 v_g[n]$ (see Fig.1) resulting in the current loop reference.

From Fig.2 it can be seen that the output of the analog-to-digital converter produces the same value at the output as long as the voltage variation around the mid-point of an A/D bin is smaller than $V_q/2$, where $V_q$ is the quantization step of the analog-to-digital converter.

By setting the quantization level around the reference voltage to be larger than the attenuated worst-case ripple $H_1\Delta v_{c\_max}$:

$$V_q > H_1 \cdot \left(2\Delta v_{c\_max}\right) = H_1 \cdot \frac{P_{load\_max}}{\omega C V_{out}} \tag{4}$$

the output voltage ripple can be eliminated from the voltage loop. The worst-case ripple is obtained when the output power is at the maximum $P_{load\_max}$.

Figure 3 shows the output voltage ripple and the low-resolution A/D converter quantization levels around the reference voltage in steady state and during a load transient that causes a change of the output voltage. In steady state the

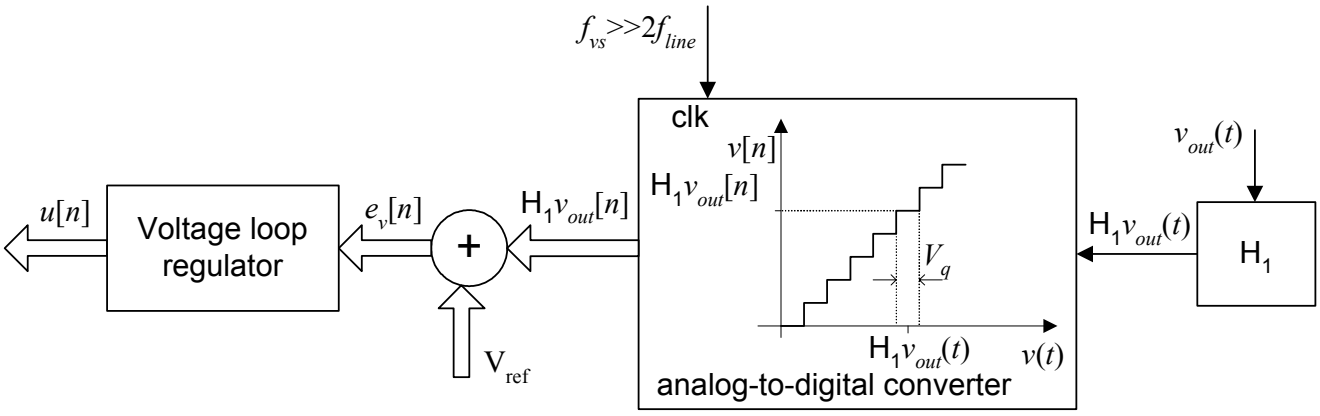


Fig.2. Block diagram of the dead-zone digital voltage loop regulator.

voltage error $e_v[n]$ is zero and the second harmonic ripple does not affect operation of the voltage loop. During the transient, the voltage error signal is not zero and the voltage loop regulator reacts in order to return the output voltage to regulation. In order to capture the moment when the transition from zero error range occurs and to react fast to the load transient, the output voltage is sampled at a frequency significantly higher than the second harmonic frequency.

In the approach illustrated by the block diagram of Fig.2 and Eq. (4), the error in the DC output voltage is smaller than the difference between one half of the quantization step and the peak amplitude of the capacitor voltage ripple. The DC output voltage regulation error can increase when the actual output capacitor voltage ripple is smaller than the maximum value. This happens when the rectifier operates at light loads, or if the load is capacitive. In most cases, the maximum possible steady-state error $V_q/(2H_1)$, which corresponds to the zero-ripple case, is acceptable. A modification of the dead-zone controller to improve the static voltage regulation further is presented in Section IV.

## III. REGULATOR DESIGN

The voltage loop regulator can be designed starting from the large signal model of a PFC rectifier shown in Fig. 4 [9]. The input port behaves as a lossless resistor $R_e$ where the emulated resistance $R_e$ is controlled by the output of the voltage loop regulator. The power absorbed by the resistor, averaged over a switching cycle, is given by:

$$\left\langle p_{ac}(t)\right\rangle_{T_s} = \frac{V_{line}^{\ 2}}{R_e}\cdot\sin^2(\omega t) = \frac{V_{line}^{\ 2}}{R_e}\left(1-\cos(2\omega t)\right) \quad (5)$$

where $V_{line}$ is the amplitude of the input line voltage. This is a nonlinear, time-varying system. A "quasi-static" small-signal model derived from the model of Fig. 4 has gains that vary with time as the line voltage changes. The approach taken here was to design the regulator for the worst-case quasi-static operating point, which is at the maximum of the rectified line voltage. The same approach has been applied and tested in [1].

Because of the relatively large quantization level $V_q$ of the A/D converter in the dead-zone controller, the A/D converter characteristic should also be taken into account as another nonlinearity in the system. This nonlinearity can be accounted for using the describing function method [15, 16]. A describing function of the A/D converter is found as the ratio of the amplitude of the fundamental component of the A/D converter output and the amplitude $V_M$ of a sinusoidal input to the A/D converter. The describing function of the A/D converter with the quantization level equal to $V_q$ is given by:

$$D\left(\frac{V_q}{V_M}\right) = \begin{cases} 0, \\ for, V_M < \dfrac{V_q}{2} \\ \dfrac{4V_q\sum_{n=1}^{M}\cos\left(\arcsin\left(\dfrac{(2M-1)V_q}{2V_M}\right)\right)}{\pi V_M} \\ for, V_M \in \left[\dfrac{(2M-1)V_q}{2} : \dfrac{(2M+1)V_q}{2}\right] \end{cases} \quad (6)$$

which is plotted in Fig.5 as a function of $V_M/V_q$. The describing function or the "gain" of the A/D converter depends on the signal amplitude and can be as large as $4/\pi$.

In the experimental prototype, a constant-coefficient PI regulator was used. The regulator was designed based on the worst-case conditions: the maximum possible amplitude of the rectified line voltage, the largest load, and the maximum "gain" of the A/D converter.

The control law of the simple digital PI regulator is given by:

$$u[n] = u[n-1] + K_1\left(e_v[n] - a_1 e_v[n-1]\right) \quad (7)$$

The regulator characteristics can be adjusted by the change of the gain $K_1$ and the coefficient $a_1$, which determines the frequency of the regulator zero.

## IV. SELF-ADJUSTING DEAD-ZONE CONTROLLER

A modification of the fixed dead-zone controller that eliminates the output voltage steady-state error for light loads or capacitive load conditions and further improves the voltage loop dynamic response is shown in Fig.6.

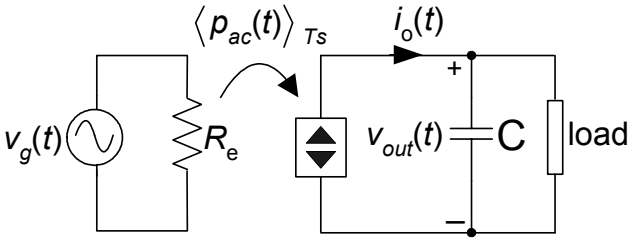


Fig.4. Large signal model of a PFC rectifier.

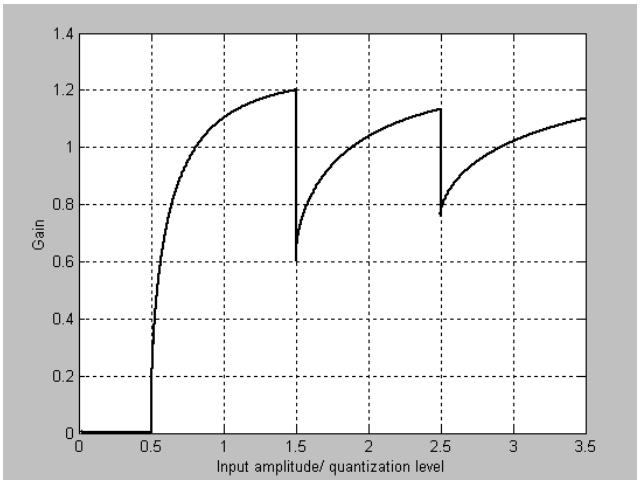


Fig. 5. Describing function of the analog-to-digital converter as a function of the ratio of the input signal amplitude $V_M$ and the quantization level $V_q$.

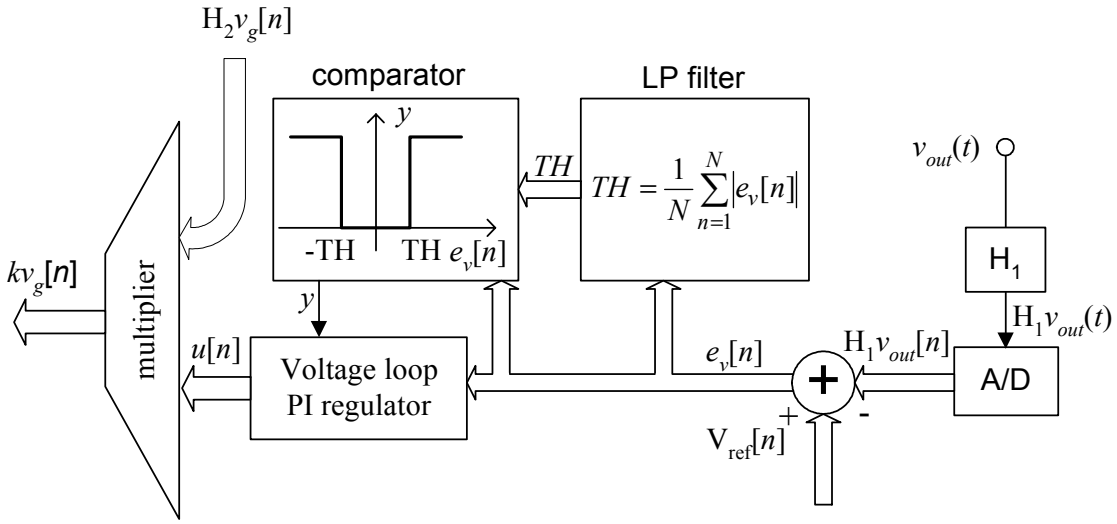


Fig.6. Voltage loop regulator with the self-adjusting dead-zone controller.

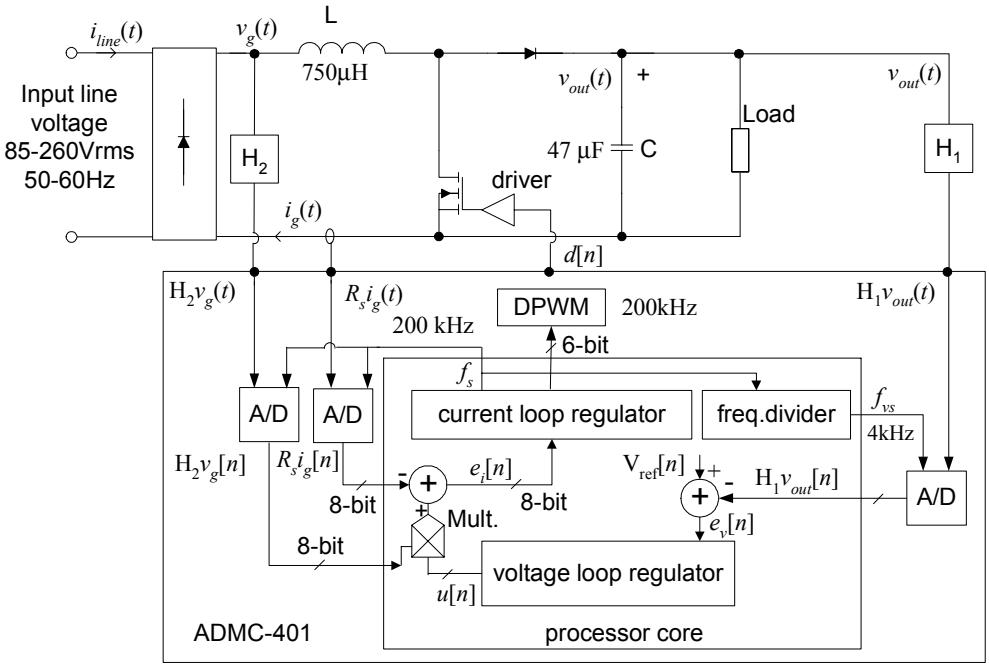


Fig.7. Experimental system.

In this modification of the method presented in Section III, a higher-resolution analog-to-digital converter ($V_q < 2\Delta v_c$), a comparator and a modified voltage loop regulator that operates in one of two possible modes are used to eliminate the steady-state error and improve the dynamic response. As long as the amplitude of the voltage error signal $e_v[n]$ is smaller than the threshold *TH,* the comparator output $y$ is low and the voltage loop regulator operates in a low-bandwidth mode with the voltage loop closed in the 10-20 Hz range. The low-bandwidth mode results in zero steady state error and elimination of the second harmonic from the voltage loop. During a transient, the voltage error signal exceeds the threshold value, sets the comparator to high level and causes a change of the voltage loop regulator to a high-bandwidth mode that provides faster response. The change of the PI regulator mode is performed through a change of the controller coefficient values $K_1$ and $a_1$ in Eq. (7). Selection of the coefficient values for the low-bandwidth mode is based on the low-frequency model of the rectifier obtained by averaging over half line cycle [9,10].

As an additional improvement, an adaptive threshold adjustment can be implemented as shown in Fig.6. A block that performs rectification and low-pass filtering of the voltage error signal adjusts the threshold to a value slightly higher than the steady-state voltage ripple amplitude. The threshold adjustment improves the transient response for light-load and/or capacitive load situations.

## V. TEST SYSTEM AND EXPERIMENTAL RESULTS

An experimental prototype based on the diagram shown in Fig.7 has been used to test the presented control methods.

### *A. Test system*

An experimental 200 W boost PFC operating at 200 kHz switching frequency is controlled by an ADMC 401 16-bit DSP evaluation board. To implement the fixed dead-zone voltage loop controller described in Section II, resolution of the analog to digital converter was limited to 6-bits. In the implementation of the self-adjusting dead-zone controller of Section IV, 8-bits of the A/D converter output were used.

Although the ADMC-401 includes a 16-bit fixed-point processor, 8-bit arithmetic was used for all computations in order to show that the complete system could be implemented with a simpler hardware. The output voltage is controlled at 380 V, and sampled at 4 kHz. This frequency satisfies the requirement $f_{vs} >> 2f_{line}$, and at the same time allows implementation of both high-bandwidth and low-bandwidth digital regulators using 8-bit arithmetic.

The operating point of the analog to digital converter in the fixed dead-zone controller is selected to give an equivalent output voltage quantization step equal to 30 V around the DC operating point. This quantization step is slightly larger than the maximum expected peak-to-peak ripple across the output filter capacitor.

The input current is sampled at 200 kHz using the variable-delay sampling method and the current control loop described in [1].

The same hardware structure was used for verification of both the fixed dead-zone and the self-adjusting dead-zone control methods. All modifications required to implement the self-adjusting dead-zone controller were completed in software.

### *B. Experimental results*

Experimental results include comparisons of load transient responses with the dead-zone controllers against transient responses obtained using a conventional, low-bandwidth voltage controller. In addition, harmonics of the input line current and the corresponding power factor were measured

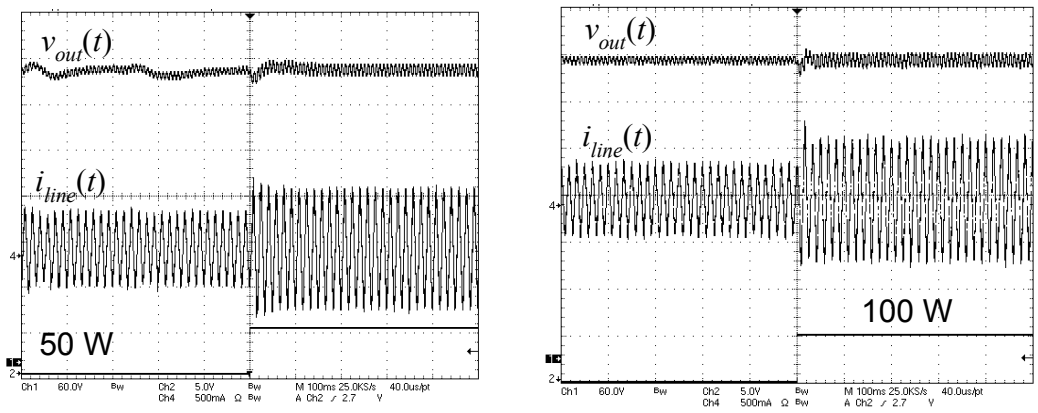


Fig.8. Operating waveforms at 50 W load and 100 W load in the experimental PFC with the fixed dead-zone controller (left) and the self-adjusting dead-zone controller (right). Time scale: 100 ms/div, Ch-1: $V_{out}(t)$, 60 V/div, Ch2: load transient, Ch-4: $i_{line}(t)$, 0.5 A/div.

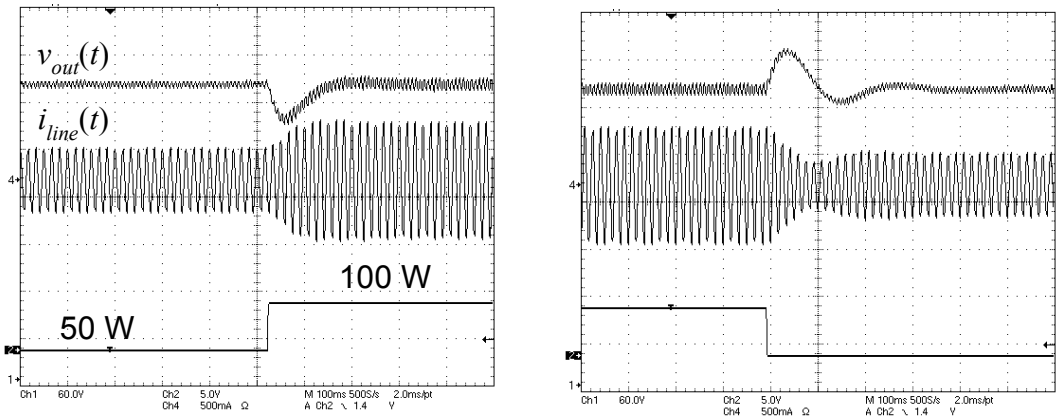


Fig.9. Load transient responses of the experimental PFC with a conventional, slow controller for 50 W - 100 W and 100 W – 50 W load changes. Time scale: 100 ms/div, Ch-1: $v_{out}(t)$, 60 V/div, Ch2: load transient, Ch-4: $i_{line}(t)$, 0.5 A/div.

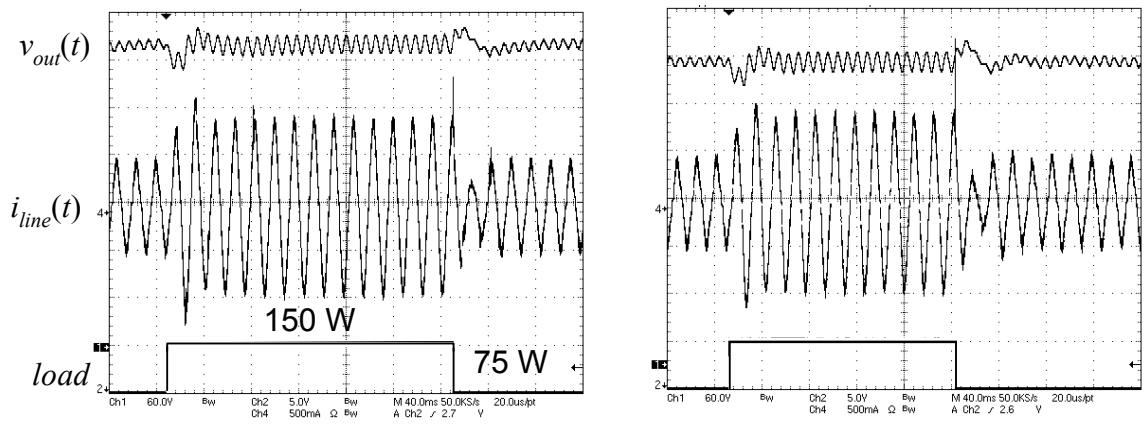


Fig.10. Load transient responses for 75 W - 150 W output load changes in the experimental PFC with the fixed dead-zone controller (left) and the self-adjusting dead-zone controller (right). Time scale: 50ms/div, Ch-1: $v_{out}(t)$, 50 V/div, Ch2: load transient, Ch-4: $i_{line}(t)$, 0.5 A/div.

under various operating conditions.

Figure 8 shows steady-state operation and light-to-medium load transient responses (50 W to 100 W) for the fixed dead-zone and the self-adjusting dead-zone control methods.

For the light load case (50 W), when the fixed dead-zone method is applied, it can be observed that the output voltage varies within the quantization step of the A/D converter and the DC output voltage can have an error with respect to the reference. The amplitude of the output voltage variation and the DC voltage error cannot be larger than one half of the A/D quantization step. When the load is increased to medium (100 W), the output voltage ripple increases, and the output voltage variations can no longer be observed. When the self-adjusting dead-zone method is applied, there are no variations of the steady-state voltage.

Total harmonic distortion of the input current in both cases varied between 4.6% for the heavy load to 9% for the light load case. The harmonic distortion for the heavy load case is lower because the error of the analog-to-digital converter for the current measurement is relatively lower than for the light-load case.

Attempting to increase the bandwidth of the voltage loop without the modifications needed to eliminate even harmonics of the line frequency from the loop results in much higher harmonic distortion, as shown in [1].

Figure 9 shows 50 W-100 W load transient responses obtained with the conventional, slow voltage loop controller. This controller is the same as the controller in the low-bandwidth mode of the self-adjusting dead-zone method. Large overshoots and dips of the output voltage can be observed, with settling times that extend over a number of line periods. The overshoots cause additional voltage stresses on the components, while the voltage dips could cause loss of regulation at high input line voltage, and increased current stresses on a downstream converter.

Figure 10 shows load transient responses of the dead-zone controllers for the 75 W-150 W output load change. Both dead-zone methods result in similar load transient responses. Compared to the conventional design, the responses are much faster, and the voltage overshoots and dips are significantly smaller, allowing for less conservative design of the power stage and the downstream DC-DC converter.

## VI. CONCLUSIONS

This paper describes a dead-zone control method for improvement of voltage loop dynamic responses in digitally controlled power factor correctors (PFC). Implementation of the dead-zone controller is based on a simple modification of the analog-to-digital converter characteristic and does not require any additional hardware or processing. The dead zone is the range of output voltages that produce a zero error at the output of the A/D converter. By selecting the A/D converter resolution, i.e., the quantization step of the A/D converter around the reference, the dead zone is selected to be larger than the expected output voltage ripple at twice the line frequency. In steady state, the output voltage error is zero and the second harmonic ripple does not affect operation of the voltage loop. In transients, a fast voltage loop can be designed to quickly bring the output voltage back to regulation, without increasing distortion of the input line current.

Two versions of the dead-zone controller are presented – using a fixed dead zone, or a self-adjusting dead-zone. In the fixed dead-zone controller, the dead zone has constant value, designed for the maximum expected output voltage ripple. In the self-adjusting version, the dead zone is adjusted to match the actual output voltage ripple. With changes in controller software and a relatively small increase in processing load, the self-adjusting dead-zone controller offers improved static voltage regulation. Both dead-zone controllers offer much faster voltage transient responses and significantly reduced voltage overshoots and dips compared to standard, low-bandwidth voltage controllers in PFC systems.

Experimental results obtained on a digitally controlled 200 W boost PFC operating at 200 KHz switching frequency show an order of magnitude faster load transient responses with the dead-zone controllers compared to the responses with a conventional voltage-loop controller.

Advantages of the proposed methods include: smaller output voltage variations, potential for less conservative design of the PFC and downstream DC-DC converters, and simpler controller implementation compared to alternative methods for improvement of voltage-loop dynamic responses in power factor preregulators.

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