Digital Controller Chip Set
for Isolated DC Power Supplies

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Abstract – **This paper describes a digital controller chip set for high-frequency DC-DC power converters with galvanic isolation. The secondary-side controller includes an A/D converter and a transmitter that sends a digital error signal as serial data through an opto-coupler. The primary-side controller includes a serial-data receiver, a programmable digital PID regulator, and a high-resolution (10-bit) digital pulse-width modulator. The digital error signal transmission through the isolation boundary eliminates the problem of gain variation when the opto-coupler is used in linear mode. The chip set is tested as a replacement for a conventional analog current-mode controller in a 3.3 V, 20 A, 400 KHz DC power supply. Experimental results with the digital controller show improved dynamic responses compared to the responses obtained with the analog controller.**

I. INTRODUCTION

Digital controllers for switching power supplies can offer a number of advantages including a reduction of the number of passive components, programmability, implementation of more advanced control algorithms and additional processing options, as well as reduced sensitivity to parameter variations. It has been shown that a complete digital controller operating at switching frequencies in the MHz range can be realized in simple hardware with a potential of outperforming standard analog solutions in terms of size, power and cost [1,2]. In this paper, we present an extension of the work reported in [1-4] to the area of digital controllers for isolated DC-DC converters.

Figure 1(a) shows a block diagram of a DC power supply with galvanic isolation and analog controller implementation. The secondary-side controller includes a reference generator and an error amplifier. The analog signal at the output of the error amplifier is transmitted to the primary side through an opto-coupler that operates in linear mode as a gain stage. The primary-side controller includes a pulse-width modulator or a current-mode modulator, a start-up circuitry and drivers for the power transistors. This architecture is frequently used in isolated DC power supplies such as the example described in [5]. A drawback of this approach is that the opto-coupler gain
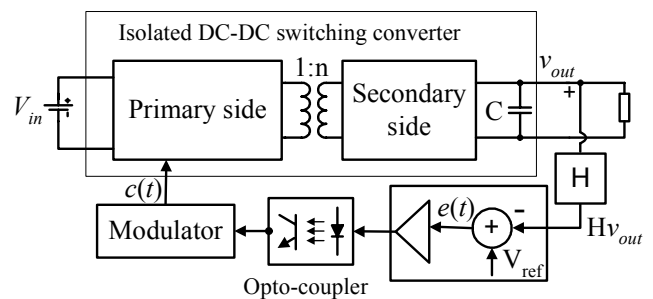
Fig.1.a. Block diagram of a typical DC power supply with galvanic isolation and a standard analog controller.
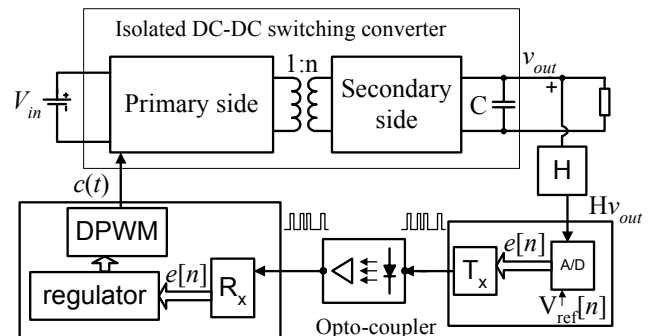

Fig.1.b. Block diagram of a DC-DC converter with galvanic isolation, digital controller and digital serial communication through the isolation boundary.

can vary significantly from component to component and over temperature. To ensure closed-loop voltage regulation with adequate stability margins, a conservative design approach is taken: the feedback loop is designed for worst-case conditions, which can result in slower dynamic responses.

The approach presented in this paper is based on digital controller implementation and digital signal transmission through isolation boundary as shown in Fig. 1(b). The secondary-side controller includes an A/D converter that outputs a digital error signal e[n]. The digital error signal is transmitted as serial data through an opto-coupler that operates as a logic gate. The primary-side controller includes a serial data receiver that restores the digital error signal e[n], a digital

regulator that implements a discrete-time control law, and a digital pulse-width modulator (DPWM). In the digital realization, the loop performance is not affected by variations in opto-coupler or error-amplifier parameters, which allows for a less conservative design of the feedback loop. To demonstrate a practical implementation of this approach, an ASIC chip set including the primary-side digital controller and the secondary-side transmitter has been designed and the results are reported in this paper.

The paper is organized as follows: a system description corresponding to the block diagram of Fig. 1(b) is given in Section II. Section III describes architecture and implementation of building blocks in the chip set, including the serial data transmitter, the serial data receiver, the digital regulator and a high-resolution (10-bit) DPWM with programmable switching frequency. In Section IV, we present experimental results obtained with a test system that includes the digital controller chip set and a power converter stage taken from the 3.3 V, 20 A, 400 KHz power supply described in [5].

II. DIGITAL CONTROLLER FOR DC POWER SUPPLIES WITH ISOLATION TRANSFORMER

Figure 2 shows a block diagram of the digital controller chip set designed to implement the system shown in Fig. 1(b).

The secondary-side ASIC takes the data from an A/D converter and generates the digital error signal $e[n]$. The serial transmitter sends the error signal as serial data to the opto-coupler OC_2. The primary side ASIC consists of a serial data receiver, a regulator and a digital pulse width modulator (DPWM). Communication and synchronization between the primary and the secondary side are performed through the opto-couplers OC_1 and OC_2.

The serial data transmission through the opto-coupler eliminates the problem of gain variations when the opto-coupler is used in linear mode, but introduces a delay between the time the error signal is generated on the secondary side and the time the error signal is available on the controller primary side. It is of interest to minimize this delay since it adversely affects achievable dynamic performance of the closed-loop power supply.

In a closed-loop voltage regulator, the A/D conversion is only needed in a relatively small window around the reference voltage [1-3]. As a result, only a few bits are needed to represent the error signal, which helps reduce the time it takes to send the data serially through the opto-coupler. In our implementation, the details of which can be found in Section III, the error signal is a 4-bit value, and the additional delay introduced by the serial data transmission is equal to one switching cycle.

On the primary side, the serial data receiver restores the 4-bit error signal, which is then taken by the digital regulator that implements a discrete-time control law. The regulator output is a 10-bit digital value that represents the duty cycle command for the digital pulse-width modulator (DPWM). The DPWM generates a pulsating drive waveform for the power transistor switch at the switching frequency f_{sw}. The duty cycle of the output gate-drive waveform is $d[n]$. In addition to the output drive waveform, the DPWM generates a system clock at sixteen times the switching frequency.

The serial data transmission from the secondary side to the primary side is synchronized to the system clock. It should be noted that the synchronization on the secondary side could be achieved using a signal derived from the secondary side of the power-stage transformer. This would eliminate the need for the opto-coupler OC_1 and the need for a start or stop sequence in the serial data generated by the transmitter. However, to simplify system testing, in our prototype chip set, the opto-coupler OC_1 has been used to provide the system clock signal to the secondary side.

III. CHIP SET IMPLEMENTATION

In the chip set implementation, the digital regulator is functionally the same as the look-up table based regulator described in [1-3]. A more detailed description is given here for the new ASIC blocks: the serial transmitter and receiver, and the high-resolution (10-bit) DPWM with programmable switching frequency.
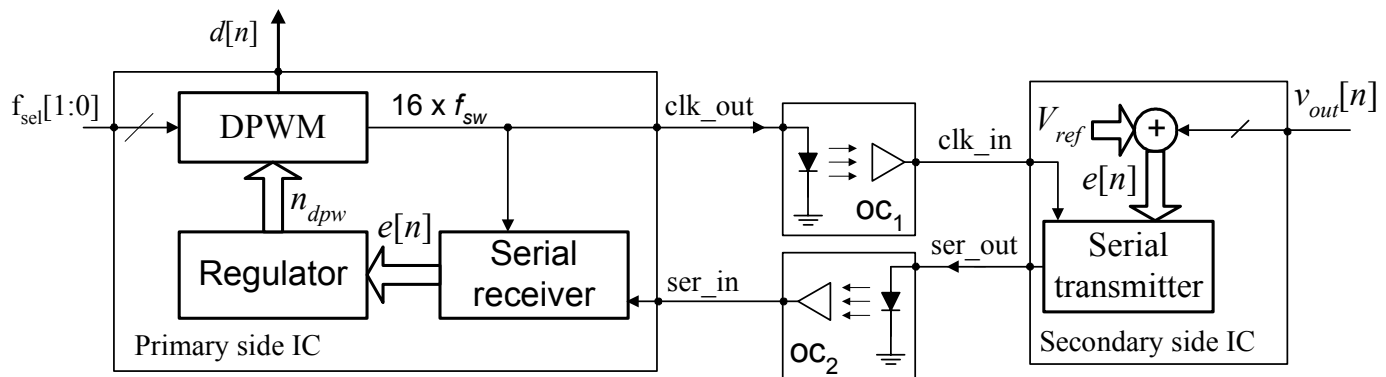

Fig.2. Block diagram of the digital controller with a serial communication block.
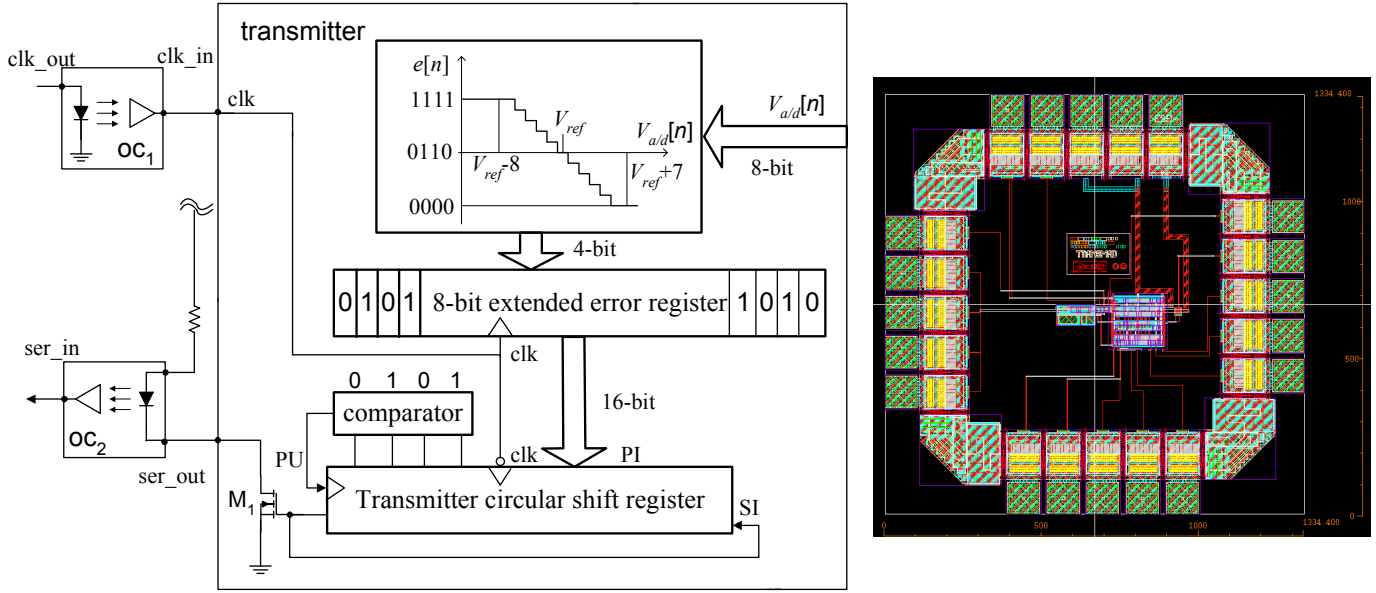
Fig.3. Block diagram of the serial transmitter and layout of the secondary-side controller chip.

A. Serial Transmitter

Figure 3 shows a block diagram of the serial data transmitter and a layout of the secondary-side chip. Parallel data is taken from an external 8-bit analog-to-digital converter that samples the output voltage. A 4-bit error signal is formed in a narrow range around the reference value, corresponding to analog voltages in the range from $V_{ref}-8\Delta V_q$ to $V_{ref}+7\Delta V_q$, where ΔV_q is the quantization step, which is the analog equivalent of the least significant bit (LSB) value. For the output voltages that are higher than $V_{ref}+7\Delta V_q$, or lower than $V_{ref}-8\Delta V_q$, the output digital error signal takes the minimum (0000) or the maximum (1111) value, respectively. The LSB voltage ΔV_q is selected such that the static output DC voltage regulation is within 0.5 % of the nominal value. On the secondary-side chip, a simple on-chip A/D converter with the same characteristic can be designed as described in [1,2].

The 4-bit error signal is expanded to an 8-bit value, and then transferred to a 16-bit buffer register. The expansion is performed according to the scheme presented in Figure 4.
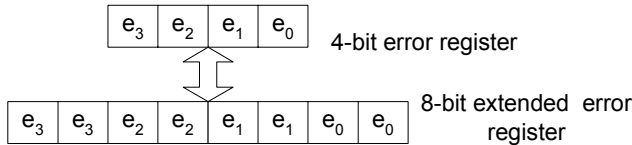

Fig.4. Bit-expansion/compression of the error register.

Each error signal bit is repeated twice in the 8-bit extended error register. The 16-bit buffer register includes a start sequence (0101) and a stop sequence (1010). The 16-bit buffer value is transferred to a circular shift register, the content of which is transmitted serially through the opto-coupler OC_2. The transmitter buffer value is updated once per switching period (which equals 16 system clock cycles), whenever the combination of ones and zeros at the beginning of the shift register indicates that the previous serial word has been sent. It can be observed that only 12 bits would be sufficient to transfer the 4-bit error value. Given the clock frequency of 16 times the switching period, there is room for transmission of additional signals, which could be used to implement protection features.

The total active chip area of the transmitter, the layout of which is shown in Fig. 3, is 0.15mm². The chip was designed in a standard 0.5μ CMOS process.

B. Serial receiver

A block diagram of the serial receiver is shown in Fig.5. The receiver takes a logic-level signal ser_in from the opto-coupler OC_2. The receiver output is the reconstructed 4-bit error signal. The serial data from the opto-coupler OC_2 is sampled at the system clock rate (at 16 times the switching frequency) and stored in the receiver shift register. When the start sequence (0101) is detected at the four most significant bits of the receiver shift register, the comparator creates an update compressor (UC) signal. The UC signal initiates the update of the compressed error register, which takes the 8-bit error from the receiver shift register and compresses it into the 4-bit value according to the scheme shown in Fig.4.

Experimental waveforms obtained with the serial transmitter and the receiver operating together are shown in Fig.6. Channel 1 (A1) shows a change of the input voltage from $V_{ref}-\Delta V_q$, which corresponds to the voltage of 3.2 V, to zero. Channel 2 (A2) shows the serial string ser_in at the input of the receiver. The digital channels 0, 1, 2 and 3 show the four decoded error bits at the output of the receiver block. In the experiment, the switching frequency is 400 KHz, and the system clock frequency is 16x0.4=6.4 MHz.
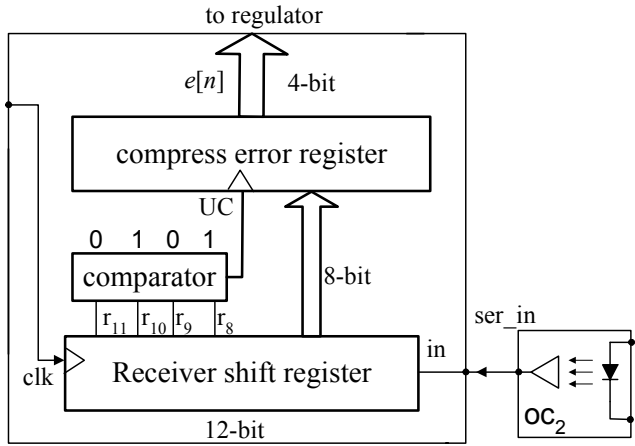
Fig.5. Block diagram of the serial data receiver.

From Fig.6 it can be seen that the serial data transmission introduces a delay of one switching period. The total delay from the moment when the output voltage change happens to the time when the error signal on the primary side is updated is less than two switching periods. This total delay includes the sampling delay of the A/D converter.
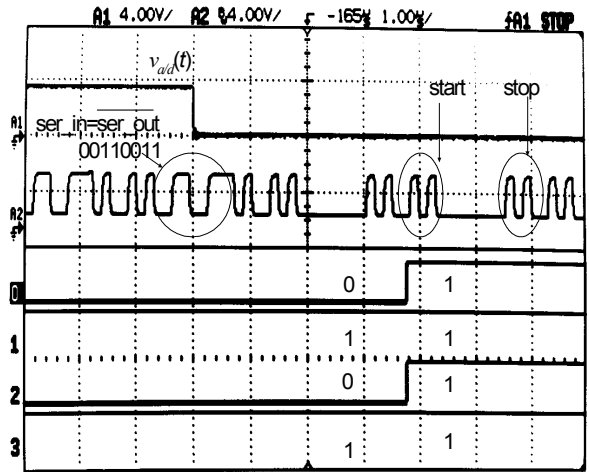

Fig.6. Experimental waveforms of the communication block for the input voltage change from V_{ref} - ΔV_q to zero. Top-to-bottom: Ch1- analog input voltage of the A/D converter; Ch2: serial data at the receiver input; digital channels [3:0]: decoded error signal $e[n]$ at the receiver output.

C. High-frequency, high-resolution digital pulse width modulator (DPWM) with programmable switching frequency

A high-resolution digital pulse-width modulator (DPWM) is needed to meet the minimum hardware requirements [3,4] in
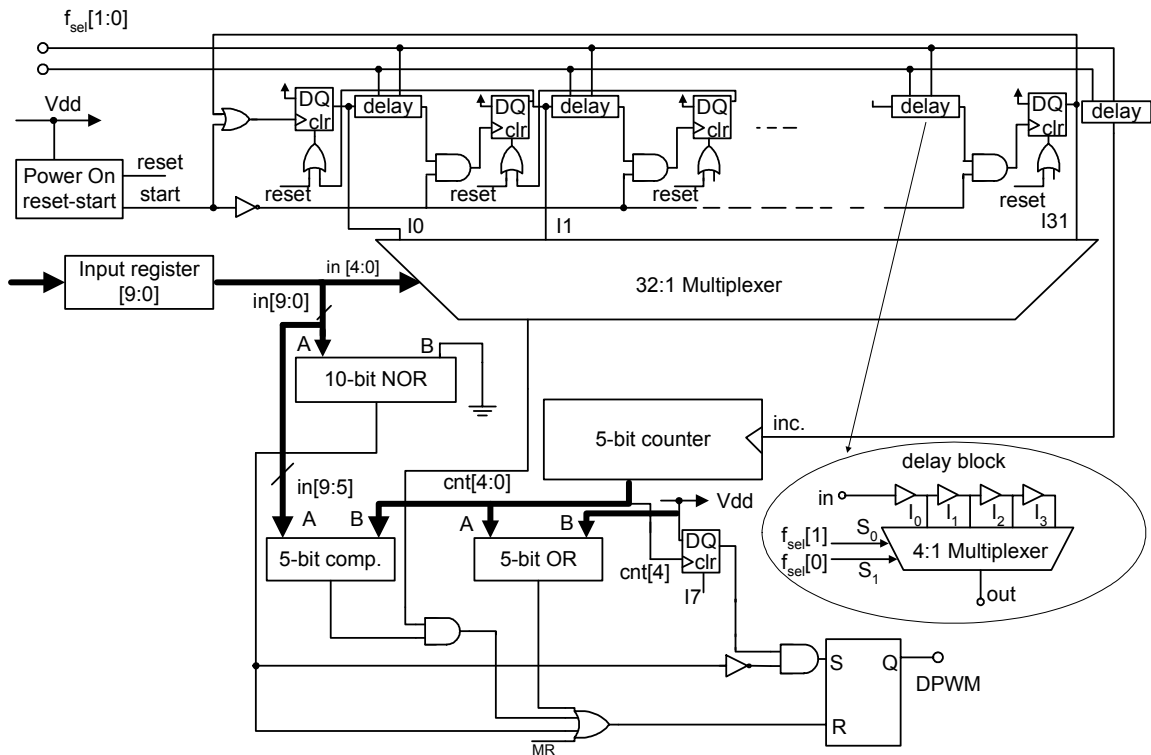

Fig.7. Block diagram of the 10-bit digital pulse width modulator (DPWM) with programmable switching frequency.

a range of isolated DC power supplies. If the DPWM resolution is lower, it may not be possible to meet the usual static voltage regulation specifications, or the system may exhibit undesirable limit-cycle oscillations. To design the 10-bit DPWM, the approach described in [1,2] was taken and modified to provide higher resolution and programmable switching frequency. A block diagram of the 10-bit DPWM integrated circuit used on the primary-side controller chip is given in Fig.7.

The DPWM includes a delay-line block, a 5-bit counter and control logic: five least significant bits of the 10-bit duty ratio value are taken by the delay-line (ring oscillator) structure consisting of 32 delay blocks, while the five most significant bits are taken by the 5-bit counter. The control logic is designed so that the DPWM produces the output duty ratio between 0 and 98%. Upon start-up or reset, the output duty ratio is forced to zero.

In order to provide programmable switching frequency, the delay blocks are constructed as shown in Fig.7. The number of cells that a signal propagates through (i.e. the delay of a block) is determined by a binary combination at the input of the delay-block multiplexer. Experimental DPWM characteristics for the fabricated prototype chip are given in Table I.

TABLE I: Characteristics of the 10-bit DPWM

Resolution	10-bit (1.3 ns at the maximum switching frequency)
Switching frequency	Four discrete values, 700 KHz maximum switching frequency
Maximum power consumption	2 mA at 700 KHz, 5 V power supply
Internal clock frequency	32 times higher than the switching frequency
On-chip area	0.16 mm^2 in 0.5 µm CMOS

D. Regulator

The regulator is based on look-up tables, following the approach described in [1-3]. To improve flexibility of the programmable regulator, three 14-bit, 16-word look-up tables are used. The on-chip area of this block is 0.12 mm^2.

A layout of the complete primary side integrated circuit is shown in Fig.8. The total area of the primary side chip, which includes the DPWM, the regulator, the receiver and a power-on-reset circuit, is 0.35 mm^2 in a standard 0.5µ CMOS process.
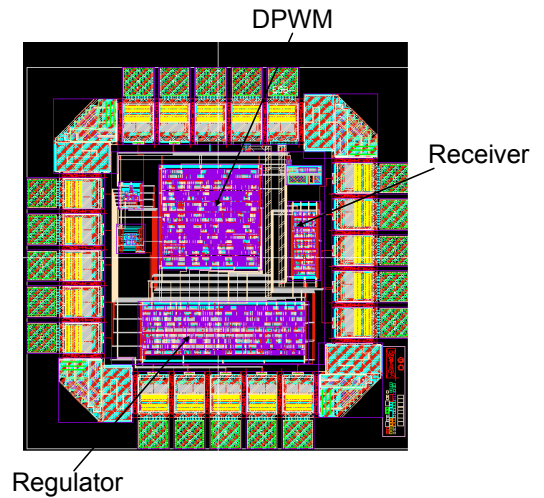

Fig.8. Layout of the primary side chip including the receiver, the regulator and the digital pulse-width modulator.

Both the primary-side chip and the secondary-side chip have been designed starting from a functional description in Verilog hardware-description language (HDL), and following standard digital ASIC design practices.
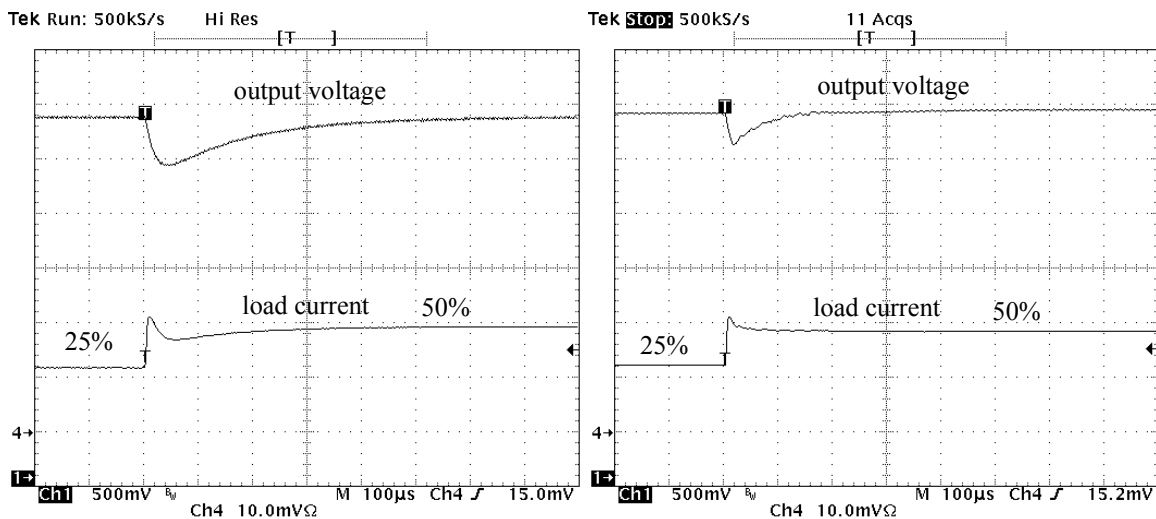

Fig.9. Load transient response (25 % to 50 %) for the converter with the original analog current-mode controller (left) and the converter with the digital controller chip set (right). Ch1: output voltage 500 mV/div, Ch4: load current 5A/div.
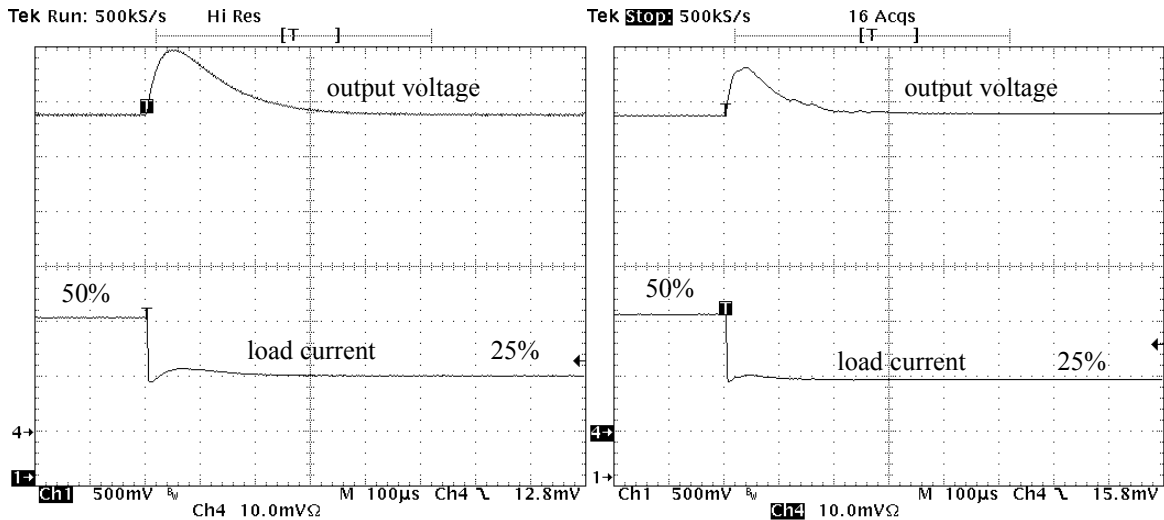
Fig.10. Load transient response (50 % to 25 %) for the converter with the original analog current-mode controller (left) and the converter with the digital controller chip set (right). Ch1: output voltage 500 mV/div, Ch4: load current 5A/div.
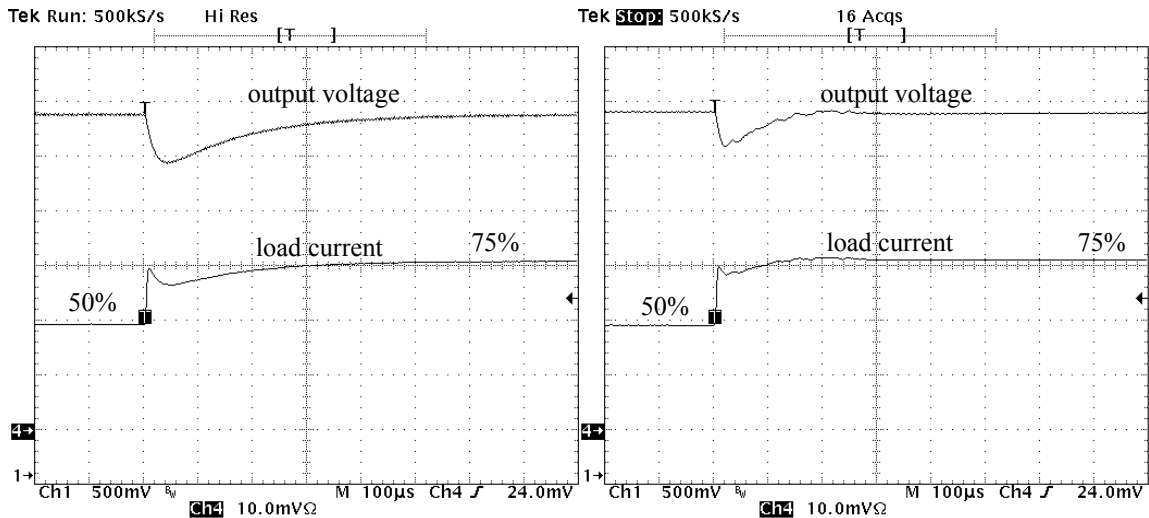

Fig.11. Load transient response (50 % to 75 %) for the converter with the original analog current-mode controller (left) and the converter with the digital controller chip set (right). Ch1: output voltage 500 mV/div, Ch4: load current 5A/div.

IV. EXPERIMENTAL RESULTS

The system of Figure 2 has been tested with a power stage from a commercial 3.3V, 20 A isolated DC power supply module [5]. This is a "half-brick" DC switching power supply that operates at 400 kHz switching frequency and uses an analog current-mode controller. In our test system, the analog controller was disconnected and replaced with the digital controller of Fig. 2. The discrete time control law implemented in the regulator was designed following the approach described in [3].

Figures 9 to 11 compare 25-50% and 50-75% load transient results obtained with the original analog current-mode controller against the results obtained with the digital controller chip set. In all cases, the converter operates at the same switching frequency of 400 KHz. It can be seen that the digital controller results in more than 2 times faster responses and about 2 times smaller deviations of the output voltage during the transients.

V. CONCLUSIONS

This paper describes a digital controller chip set for DC-DC converters with transformer isolation. The secondary-side controller includes an A/D converter that outputs a digital error signal, which is then transmitted as serial data through an opto-coupler that operates as a logic gate. The primary-side controller includes a serial data receiver that restores the digital error signal, a programmable digital regulator that implements a discrete-time control law, and a high-resolution

(10-bit) digital pulse-width modulator (DPWM) with programmable switching frequency (up to 700 KHz). In the digital controller realization, the loop performance is not affected by variations in opto-coupler or error-amplifier parameters, which allows for a less conservative design of the feedback loop.

To demonstrate a practical implementation of the proposed approach, an ASIC chip set, including the primary-side digital controller and the secondary-side transmitter, has been designed in a standard digital CMOS process starting from a functional description in Verilog hardware description language (HDL), and following standard digital ASIC design practices. The chip set has been tested as a replacement for an analog current-mode controller in a commercial 3.3 V, 20 A, 400 KHz DC power supply. Experimental waveforms show that the digital controller results in significantly improved transient responses compared to the responses obtained with the original analog controller, illustrating the point that digital controllers can be practical and advantageous alternatives to standard analog solutions in a range of power electronics applications.

ACKNOWLEDGMENT

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