Modeling of Quantization Effects in Digitally Controlled DC-DC Converters

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***Abstract*— In digitally controlled DC-DC converters with a single voltage feedback loop, the two quantizers, namely the A/D converter and the digital pulse-width modulator (DPWM), can cause undesirable limit-cycle oscillations. In this paper, static and dynamic models that include the quantization effects are derived and used to explain the origins of limit-cycle oscillations. In the static model, existence of DC solution, which is a necessary no-limit-cycle condition, is examined using a graphical method. A concept of amplitude and offset dependent gain is introduced to extend the describing function method and derive the dynamic system model. From the static and dynamic models, no-limit-cycle conditions associated with A/D, DPWM and compensator design criteria are derived. The conclusions are illustrated by simulation and experimental examples.**

I. INTRODUCTION

Digitally controlled PWM converters have gained increased attention because of a number of potential advantages including lower sensitivity to parameter variations, programmability, reduction or elimination of external passive components, as well as possibilities to implement more advanced control, calibration or protection algorithms. It has been demonstrated that such advantages can be realized without compromising dynamic performance, simplicity or cost ([1], for example).

The increased interest in digital control motivates the research in related design-oriented analysis and modeling techniques. In particular, it is well known that a digitally controlled PWM converter, a block diagram of which is shown in Fig. 1, may exhibit undesirable limit-cycle oscillations because of the nonlinear elements, analog-to-digital (A/D) and digital-to-analog (digital PWM) quantizers, in the feedback loop [2, 3]. In general control theory, limit cycle has been studied extensively [4-7]. For PWM converters, some of the quantization effects and no-limit-cycle conditions have been addressed in [2]. The purpose of this paper is to introduce more complete static and dynamic models that take into account multiple nonlinearities in the loop (A/D and DPWM quantizers), leading to a new set of no-limit-cycle conditions as well as A/D, DPWM and compensator design guidelines. In the static model, discussed in Section II, a graphical method is used to examine existence of a DC solution, which is a necessary no-limit cycle condition. In Section III, we extend the describing function [8] of a quantizer with a new concept of amplitude and offset dependent gains of the quantizers. A dynamic model including the effective quantizer gains is presented in Section IV. Based on the approach described in [9], the dynamic system model is used to predict the frequency and amplitude of a near-sinusoidal limit-cycle oscillation if it does occur. No-limit-cycle conditions are derived in Section V. Simulation and experimental results are presented in Section VI to illustrate the results from Sections II-V. Finally, for the cases where the assumptions of the describing function method are not met, Section VII gives a conservative bound for the limit-cycle oscillation amplitude, while Section VIII summarizes the conclusions.

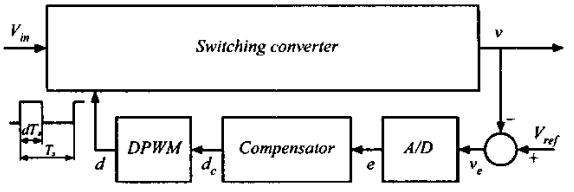

Fig. 1. Digitally controlled DC-DC switching power converter.

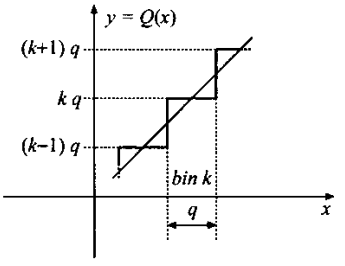

Fig. 2. Quantizer characteristic.

II. STATIC MODEL WITH A/D AND DPWM QUANTIZERS

In the system of Fig. 1, we assume that quantization effects in the digital compensator computation can be neglected, *i.e.*, that sufficiently long words are used to compute the duty cycle command d_c. Under this assumption, the digitally controlled converter of Fig. 1 includes two quantizers: the A/D converter and the DPWM, which serves as a D/A converter. The digital error signal e at the A/D output is obtained by quantization of the analog error voltage $v_e = V_{ref} - v$, while the duty cycle d at the DPWM output is obtained by quantization of the duty cycle command d_c.

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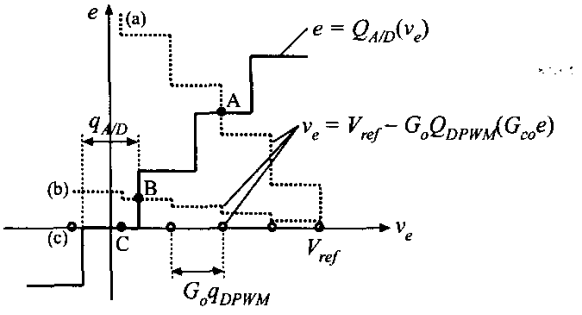

Fig. 3. Graphical solution of the static model for the digitally controlled converter of Fig. 1, for three DC compensator gains G_{co}: (a) small G_{co} (b) large G_{co}, and (c) $G_{co} \to \infty$.

The characteristic of a quantizer having a continuously varying input x and an output $y = Q(x)$ is illustrated in Fig. 2. The range of x is divided into bins of width q, where q is the "quantization level," or the value of the quantizer's least significant bit (LSB). For x in the k^{th} bin, the output y equals the k^{th} discrete output value ($y = kq$). Based on this quantizer definition, we note that a quantizer with very high resolution ($q \to 0$) behaves as a linear block having a gain of 1.

To examine quantization effects in the system of Fig. 1, it is first necessary to develop a static model and to establish conditions for existence of a DC solution. This task has been accomplished in [2, 3]. In this section we give an additional explanation and graphical interpretation of the main results.

The system DC solution can be obtained graphically as the intersection of the A/D quantization characteristic,

$$e = Q_{A/D}(v_e), \tag{1}$$

and the system static characteristic through the DPWM,

$$\begin{aligned} v_e &= V_{ref} - v = V_{ref} - G_o d \\ &= V_{ref} - G_o Q_{DPWM}(d_c) = V_{ref} - G_o Q_{DPWM}(G_{co}e), \end{aligned} \tag{2}$$

where G_o is the DC control-to-output gain of the converter, and G_{co} is the DC gain of the compensator, $d_c = G_{co}e$. Since the quantizer output are discrete values, an intersection of the two curves that resides at the transition from one output level to another output level means that there is no DC solution to the system. The graphical solution is illustrated in Fig. 3 for three cases of the compensator gain:

(a) if the compensator gain is relatively small, a DC solution may or may not exist. As an example, Fig. 3(a) shows a stable DC solution at point A;

(b) for sufficiently large DC compensator gain,

$$G_{c0} > \frac{V_{ref} - 0.5q_{A/D}}{G_0 q_{A/D}}, \tag{3}$$

the intersection is a point B on the 0-to-1 LSB transition of the A/D characteristic. We conclude that in this case a stable DC solution does not exist and the system always exhibits limit-cycle oscillations;

(c) for infinitely large DC gain, *i.e.*, when an integral compensator is employed, the curve corresponding to (2) reduces to discrete points on the v_e axis. A DC solution of the system exists when at least one of these points resides in the zero error bin of A/D characteristic, such as the point C in Fig. 3(c). Existence of a DC solution is guaranteed provided that the DPWM resolution is sufficiently high, *i.e.*, provided that:

$$G_o q_{DPWM} < q_{A/D}, \tag{4}$$

where q_{DPWM} and $q_{A/D}$ are the LSB values of the DPWM and the A/D converter, respectively. This last conclusion is consistent with the basic no-limit-cycle conditions formulated in [2,3]. In the rest of the paper, we assume that an integral compensator is employed and that the static no-limit-cycle condition (5) is satisfied.

III. Describing Functions of the Quantizers

The describing function method [8] is an approximate analysis method for nonlinear systems, where a nonlinear element is replaced by an amplitude (and/or frequency) dependent transfer function. Successful applications of the describing function method rely on the assumption that the signals at the quantizer inputs are approximately sinusoidal. In this section we address the derivation of the describing functions for the two quantizers, the A/D converter and the DPWM.

Consider a quantizer having the characteristic $y = Q(x)$ illustrated in Fig. 2, and suppose that the input signal is sinusoidal:

$$x(t) = a\cos(\omega t), \tag{5}$$

The Fourier series expansion of the output $y(t)$ is:

$$y(t) = a_0 + a_1\cos(\omega t) + \ldots + a_k\cos(k\omega t) + \ldots, \tag{6}$$

The describing function $N(a)$ of the quantizer is [8]:

$$N(a) = \frac{a_1}{a}. \tag{7}$$

In all cases considered here, the describing function is independent of frequency. Therefore, we can say that the

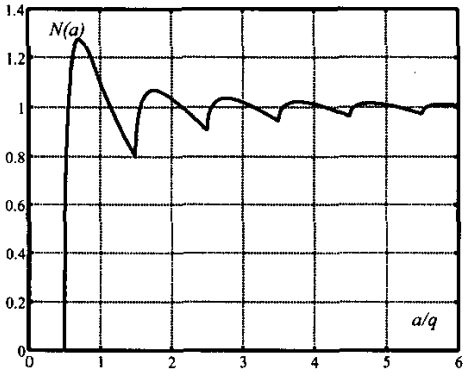

Fig. 4. Describing function of a quantizer when the DC offset is $\varepsilon = 0$, *i.e.*, the DC value of the input sinusoidal signal matches the midpoint of a quantization bin.

describing function $N(a)$ in (7) represents the effective *amplitude-dependent gain* of the quantizer.

Figure 4 shows the textbook result for the describing function $N(a)$ of a quantizer. Notice that the maximum effective gain of $4/\pi = 1.27$ is obtained for $a = q/\sqrt{2}$, and that $N(a)$ approaches 1 for $a >> q$.

We have found that the textbook definition based on (5)-(7) is not sufficient to develop a complete dynamic model for the system of Fig. 1. A key new concept introduced here is that the describing function of a quantizer in Fig. 1 depends not only on the amplitude a of the assumed sinusoidal input signal, but also on the input signal DC offset ε with respect to the mid-point of a quantization bin. Assuming that

$$x(t) = \varepsilon + a\cos(\omega t), \tag{8}$$

the Fourier series expansion of the output $y(t)$ has the same form as in (6), and the amplitude *and offset* dependent describing function $N(a, \varepsilon)$ is again defined by (7).

It is important to note that the amplitude and offset dependent gain of a quantizer can be significantly greater than 1 as the offset ε approaches $q/2$. In the worst case, $\varepsilon = q/2$, the input sinusoidal signal is centered at the transition point of the quantizer. Figure 5 shows an example of the input and output waveforms in this situation, for a quantizer with $q = 1$. Since the input signal with an arbitrarily small amplitude can produce the output with a non-zero amplitude, the quantizer with the input signal having the offset $\varepsilon = q/2$ can exhibit an *infinitely large gain*. Figure 6 shows the describing functions $N(a, \varepsilon)$ for several different values of the offset ε.

Let us consider the A/D converter. Because of the assumed integral action (*i.e.* infinite DC gain) of the compensator, the steady-state DC value of the A/D output must be equal to zero. Therefore, if a sinusoidal limit-cycle oscillation exists at the A/D input, this oscillation must have a zero DC offset, $\varepsilon_{A/D} = 0$. We conclude that the traditional zero-offset describing function can be used to model the A/D converter. The offset ε_{DPWM} at the input of the DPWM quantizer, however, *can be arbitrary*, and we have to include the possibility of the worst-case offset $\varepsilon_{DPWM} = q_{DPWM}/2$ in the model. The observation that the DPWM can contribute an effective gain much larger than 1 has important consequences in the construction of the system dynamic model and derivation of additional no-limit-cycle conditions.

IV. Dynamic Model and Existence of Sinusoidal Limit-Cycle Oscillations

Denote the converter power stage transfer function as $G_{vd}(s)$, and the continuous-time equivalent of the compensator transfer function as $G_c(s)$. Figure 7 shows a dynamic model for the system of Fig. 1 where the two quantizers are replaced by the amplitude and offset dependent effective gains. Using the model of Fig. 7, and the describing functions of Section III, existence, frequency and amplitude of a sinusoidal limit-cycle oscillation can be obtained using the approach described in [5].

Let $T_L(s)$ be the linear part of the loop gain, which does not include the quantizers,

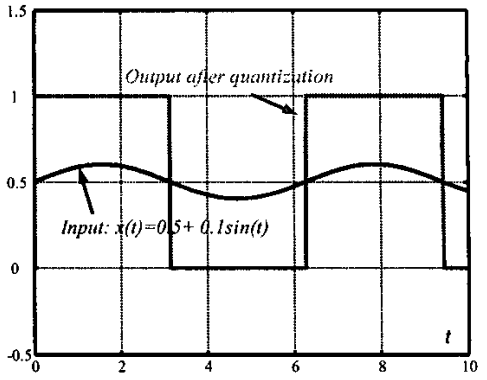

Fig. 5. Small amplitude sinusoidal signal becomes square wave signal with much bigger amplitude when the DC offset ε of the input sinusoidal signal matches the transition point ($0.5q$) between two quantization bins.

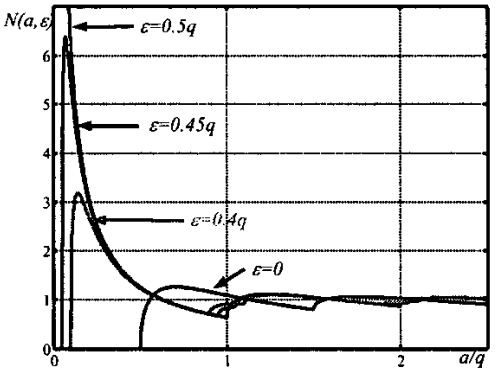

Fig. 6. Describing function of a quantizer for several different values of the offset ε.

$$T_L(s) = G_c(s)G_{vd}(s) \tag{9}$$

As discussed in Section III, the describing functions of the quantizers in Fig. 1 are independent of frequency, and do not introduce a phase shift between the input sinusoidal signal and the fundamental of the output signal. Therefore, from linear system theory, if a limit-cycle oscillation exists, the oscillation frequency f_x is such that:

$$\angle T_L(j\omega_x) = -180° \tag{10}$$

Suppose that the signal v_e at the input of the A/D is a.

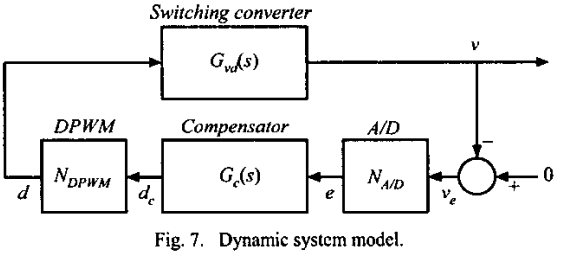

Fig. 7. Dynamic system model.

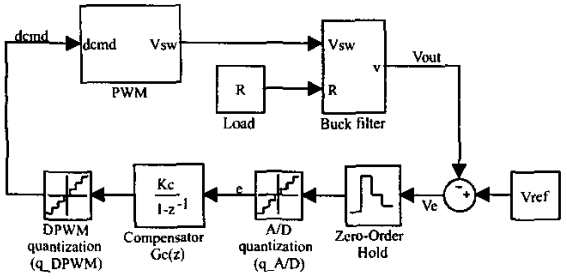

Fig. 8. *Simulink* model.

Then, *at the frequency* f_x, the magnitude of the amplitude/offset-dependent system loop gain $T(a,\varepsilon_{DPWM})$ can be found as follows:

$$\begin{aligned} T(a,\varepsilon_{DPWM}) &= \frac{v}{d}\cdot\frac{d}{d_c}\cdot\frac{d_c}{e}\cdot\frac{e}{v_e} \\ &= \left\|G_{vd}(j\omega_x)\right\| \\ &\cdot N_{DPWM}\left(\left\|G_c(j\omega_x)\right\| N_{A/D}(a,0)a,\varepsilon_{DPWM}\right) \\ &\cdot\left\|G_c(j\omega_x)\right\| \\ &\cdot N_{A/D}(a,0). \end{aligned} \tag{11}$$

If there exists an amplitude a_x and an offset ε_x such that

$$T(a_x, \varepsilon_x) = 1 \tag{12}$$

and

$$\left.\frac{\partial T(a,\varepsilon_x)}{\partial a}\right|_{a=a_x} < 0 \tag{13}$$

a near-sinusoidal limit-cycle oscillation of amplitude a_x and frequency f_x will occur in the system. Equations (10) and (12) are the standard oscillation conditions, while (13) is related to the stability of the oscillation. If, for example, the amplitude a drops below a_x, (13) implies that the loop-gain magnitude increases above 1, which implies that a will increase towards the equilibrium $a = a_x$.

V. No-Limit-Cycle Conditions and Design Guidelines

The models of Section II, III and IV can be used to formulate no-limit-cycle conditions and design guidelines related to the selection of the A/D and DPWM resolutions and the compensator design.

A. Static condition

A necessary no-limit-cycle condition is that a DC solution exists. According to the discussion in Section II, a DC solution is guaranteed to exist provided that an integral compensator is employed, and that the DPWM resolution is sufficiently high,

$$G_o q_{DPWM} < \alpha\, q_{A/D}, \tag{14}$$

where G_o is the DC duty-cycle-to-output gain and α can be as high as 1. In practice, to ensure a design margin, a smaller α is recommended ($\alpha = 0.5$ has been suggested in [2]).

B. Dynamic condition

A dynamic no-limit-cycle condition follows from the discussion in Sections III and IV. Let f_x be a frequency where (10) is satisfied, *i.e.*, a frequency where the phase response of the linear part of the system loop gain equals $-180°$. The *dynamic no-limit-cycle condition is:*

$$T(a,\varepsilon_{DPWM}) < 1, \tag{15}$$

for all $a > q_{A/D}/2$ and $0 \le \varepsilon_{DPWM} \le q_{DPWM}/2$, where a is the amplitude of the signal v_e at the A/D input, and $T(a, \varepsilon_{DPWM})$ is the magnitude of the amplitude/offset-dependent system loop gain computed from (11).

The condition (15) is related to the gain margin of the linear part of the system. For large signal amplitude $a >> q_{A/D}$, the system loop gain magnitude (11) gives the gain margin GM_L of the linear part of the system:

$$GM_L[\text{dB}] = -20\log\left\{T(a,\varepsilon_{DPWM})\big|_{a>>q_{A/D}}\right\}. \tag{16}$$

Note that the condition (15) requires that the linear part of the system is stable, *i.e.*, that the gain margin GM_L is positive. In addition, the condition (15) captures gain effects of the quantizers in terms of the amplitude a and the offset ε_{DPWM}.

The general dynamic no-limit-cycle condition (15) leads to two simple no-limit-cycle conditions in terms of the A/D and DPWM resolutions, and the converter and controller responses.

*B.*1 The worst-case (infinite) DPWM gain, which occurs for $\varepsilon_{DPWM} = q_{DPWM}/2$, is canceled by the zero gain of the A/D for signal amplitudes $a < q_{A/D}/2$:

$$\frac{4}{\pi}\left\|G_{vd}(j\omega_x)\right\| q_{DPWM} < q_{A/D} \tag{17}$$

Very large effective DPWM gain is a result of a very small amplitude signal at the DPWM input around the worst-case offset $\varepsilon_{DPWM} = q_{DPWM}/2$. In this case, the DPWM output is a square wave of amplitude q_{DPWM}, and $(2/\pi)q_{DPWM}$ is the amplitude of the corresponding fundamental at f_x. The dynamic condition *B*.1 (Eq. (17)) is the condition that the resulting amplitude a at the A/D input is smaller than $q_{A/D}/2$.

B.2 The gain margin GM_L of the linear part of the system is sufficiently high:

$$GM_L > 20\log\left(\frac{4}{\pi}\right)^2 = 4.2\,\text{dB}. \tag{18}$$

If a signal at the DPWM output oscillates between only two adjacent quantization levels, the no-limit-cycle condition *B*.1 applies. If the DPWM output steps over three or more levels, the effective DPWM gain cannot be greater than $4/\pi$, for any ε_{DPWM}. Similarly, the effective A/D gain cannot be greater than $4/\pi$, as discussed in Section III. Therefore, under the assumption that the signal at the DPWM output spans over more than two quantization levels, the combined DPWM and A/D gain cannot exceed $(4/\pi)^2 = 1.62$, which gives the no-limit-cycle condition *B*.2 (Eq. (18)).

Together, the conditions *B*.1 and *B*.2 imply the general dynamic no-limit-cycle condition (15). These conditions have not been reported earlier.

Note that the conditions *A* and *B*.1 clearly indicate the need for a high-resolution DPWM, while the conditions *A* and *B*.2 have direct implications on the compensator design – the compensator must include an integral action (as reported earlier in [2]), and must result in sufficiently large gain margin of the linear part. The condition *B*.1 originates from the fact that the DPWM can provide large effective gain, but the realization of the high gain depends on the DC offset and the amplitude of the signal at the DPWM input, which do not always occur. As a result, not satisfying the no-limit-cycle condition *B*.1 does not necessarily lead to a persistent limit cycle oscillation as long as there is a DC solution to the system.

The relative importance of the no-limit-cycle conditions established in this section depends on the particular application. In all cases, to avoid limit-cycle oscillations, the static condition *A* (Eq. (14)) must be satisfied. In applications with a relatively fast controller, the frequency f_x in (10) is relatively high, and the condition *B*.1 (Eq. (17)) is likely to be satisfied whenever the static condition *A* is met. In this case, in addition to the condition *A*, the condition *B*.2 must be taken into account. However, this is not the case in applications with a relatively slow integral compensator, where the condition *B*.1 can be very important, as illustrated in the next section.

VI. Simulation and Experimental Results

In this section, we present several examples to illustrate the results of Sections II-V.

A. Simulation example: no-limit-cycle condition B.2

Simulink model of a digitally controlled buck converter used in the simulation examples is shown in Fig. 8. The converter parameters are: $L = 10$ μH, $C = 10$ μF, $R = 1\ \Omega$, $V_{in} = 5$ V, $V_{ref} = 2.5$ V, $f_s = 1$ MHz. An integral discrete-time compensator is applied,

$$G_c(z) = \frac{K_c}{1 - z^{-1}}. \tag{19}$$

The integral compensator provides a phase lag of 90°. Therefore, the frequency f_x where (10) is met is

$$f_x = f_o = \frac{1}{2\pi\sqrt{LC}} = 15.9\ \text{kHz}. \tag{20}$$

With $K_c = 0.016$, the gain margin of the linear part is very small, but the system without quantizers is stable. When an A/D quantizer with $q_{A/D} = 0.2$ V is added, the system violates the condition *B*.2, and a limit cycle oscillation occurs, even when q_{DPWM} is still very small. Signal waveforms v_e at the A/D input and e at the A/D output are shown in Fig. 9. The A/D input signal amplitude is around $0.75q_{A/D}$, which corresponds to the effective A/D gain of approximately 1.2 in Fig. 4. The oscillation frequency obtained by simulation is very close to f_x.

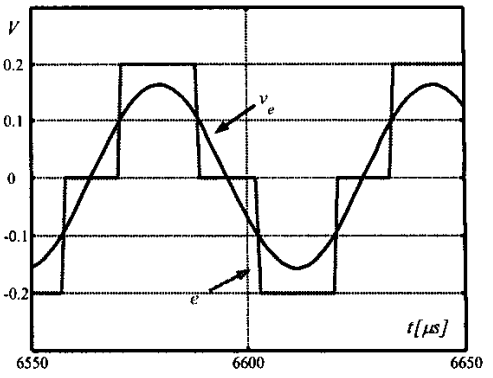

Fig. 9. Steady-state waveforms v_e at the A/D input and e at the A/D output in the example of Section VI.*A*.

B. Simulation example: no-limit-cycle condition B.1

In this example, the Simulink model of Fig. 8 is applied with the following parameters for the buck converter: $L = 10$ μH, $C = 10$μF, $R = 5\Omega$, $V_{in} = 5$ V, $V_{ref} = 2.505$ V, $f_s = 1$ MHz. The integral discrete-time compensator (19) is used, with $K_c = 0.0002$. The A/D quantizer has $q_{A/D} = 0.02$ V, and the DPWM quantizer has $q_{DPWM} = 0.002$. The frequency f_x is again given by (20). The gain margin of the linear part is $GM_L = 26$ dB. This system satisfies all no-limit-cycle conditions in [2]. Figure 10 shows that a limit-cycle oscillation occurs as a result of violation of the condition *B*.1: the DPWM input and output waveforms clearly illustrate the large effective gain of the DPWM. If the DPWM quantization level is reduced to $q_{DPWM} = 0.0005$, which satisfies the condition *B*.1, the limit cycle oscillation disappears. It is of interest to examine the plots of the magnitude loop gain $T(a, \varepsilon_{DPWM})$ computed from (11) as a function of the signal amplitude a, for the worst-case offset $\varepsilon_{DPWM} = q_{DPWM}/2$. The results are shown in Fig. 11 for $q_{DPWM} = 0.002$, and for $q_{DPWM} = 0.0005$. For $q_{DPWM} = 0.002$, there is an amplitude $a = a_x = 0.032$ V such that (12) and (13) are met. This oscillation amplitude predicted by the dynamic model of Section IV is very close to the v_e signal amplitude obtained by simulation as shown in Fig. 10. For $q_{DPWM} = 0.0005$, $T(a, \varepsilon_{DPWM}) < 1$ for all a, the no-limit cycle condition (15) is met, and no limit cycle oscillations occur.

C. Experiment: no-limit-cycle condition B.1

An experiment similar to the simulation example of Section *B* is performed using the experimental digitally controlled buck converter shown in Fig. 12 [11]. The buck converter parameters are $L = 10$ μH, $C = 10$ μF, $V_{in} = 3.313$ V, $V_{ref} = 1.3$ V, $f_s = 1$ MHz. Note that the A/D converter consists of only two comparators. The A/D converter characteristic is shown in Fig. 13(a), together with the corresponding describing function in Fig. 13(b). Instead of the fast PID compensator described in [11], the controller is programmed to operate as a slow integral compensator (19), with $K_c = 1.26 \times 10^{-3}$. The 6-bit feed-forward DPWM with

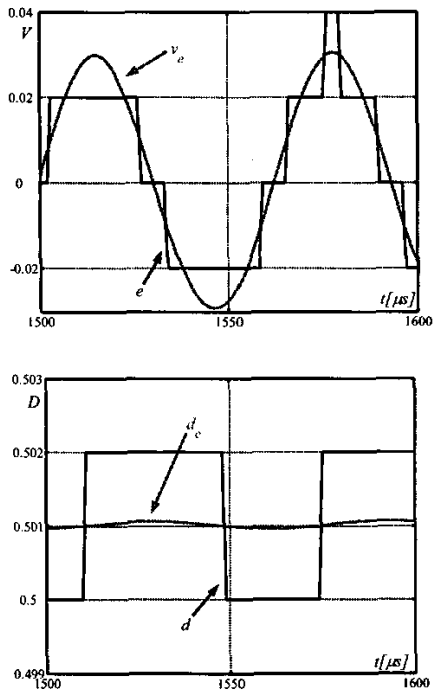

Fig. 10. Top: waveforms v_e and e before and after A/D quantization. Bottom: duty-cycle command d_c at the DPWM input, and the quantized duty-cycle command d in the example of Section VI.*B*.

additional 3 bits added by duty-cycle dithering results in $V_{in}\, q_{DPWM} \approx 5$ mV. The A/D quantization level is $q_{A/D} \approx 50$ mV. Because of the high switching frequency, the duty-cycle dithering contributes a very small additional ripple in the output voltage, well within the zero-error bin of the A/D converter. As in the simulation examples of Sections *A* and *B*, the frequency f_x given by (20) is 15.9 kHz.

Since $\|G_{vd}(j\omega_x)\| \approx V_{in}Q$, where $Q \approx R\sqrt{C/L}$ (neglecting losses), the gain margin of the linear part of the system depends on the load resistance R. For example, for a load of $R = 1\ \Omega$, $GM_L \approx 27.6$ dB. We tested a range of load transient responses. Figure 14 shows the waveforms for the case when the load current changes periodically from 160mA to 390mA, which corresponds to a load resistance change from 8 Ω to 3.3 Ω, respectively. For $R = 8\ \Omega$, the no-limit-cycle condition *B*.1 is not satisfied, and near-sinusoidal limit cycle oscillations at the frequency of approximately f_x can be observed in the output voltage and the A/D signals x and y. For $R = 3.3\ \Omega$, Q is reduced and the no-limit-cycle condition *B*.1 is satisfied. For this load, no limit cycle oscillations occur, as illustrated by the waveforms of Fig. 14.

VII. NON-SINUSOIDAL LIMIT CYCLING

The dynamic model of Sections III and IV, and the no-limit-cycle conditions of Section V.*B* are based on the assumption of near-sinusoidal limit cycle oscillation. Under this assumption, if a limit cycle exists, the oscillation

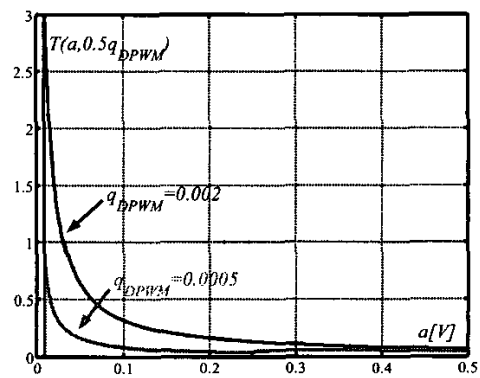

Fig. 11. Magnitude loop gain $T(a, \varepsilon_{DPWM})$ at f_x for two DPWM quantization levels q_{DPWM} in the example of Section VI.*B*.

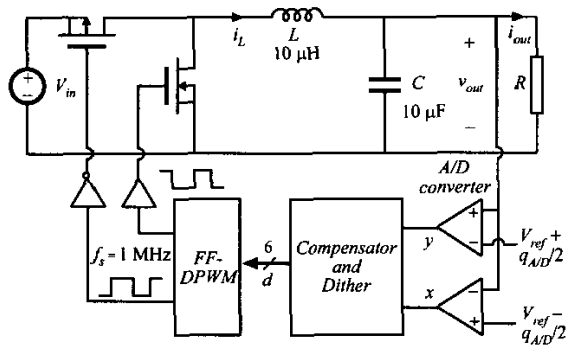

Fig. 12. Experimental digitally-controlled 1 MHz buck converter [11].

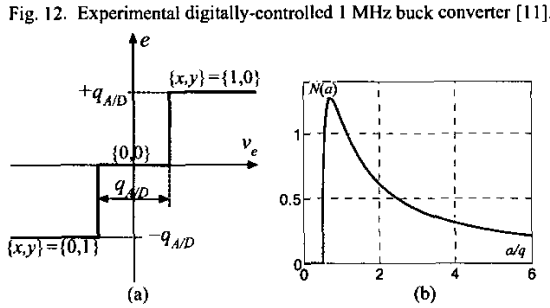

Fig. 13. Characteristic (a) and the describing function (b) of the A/D converter in Fig. 12.

amplitude and frequency can be inferred from the model in Section IV, with illustrative examples shown in Section V. It is important to note that even when all conditions of Section V are satisfied, non-sinusoidal limit-cycle oscillations may still occur, especially if α in (14) is close to 1, or if the gain margin is close to the limit in (18). In such cases, the DPWM output may swing between two adjacent levels, but with a more complicated oscillation pattern. It is then of interest to find a bound on the limit cycle oscillation amplitude in the output voltage. For an arbitrary signal pattern consisting of two adjacent DPWM levels, a bound for the signal amplitude at the output can be found from linear system theory as the induced L_∞ norm, which can be computed as the L_1 norm of the system impulse

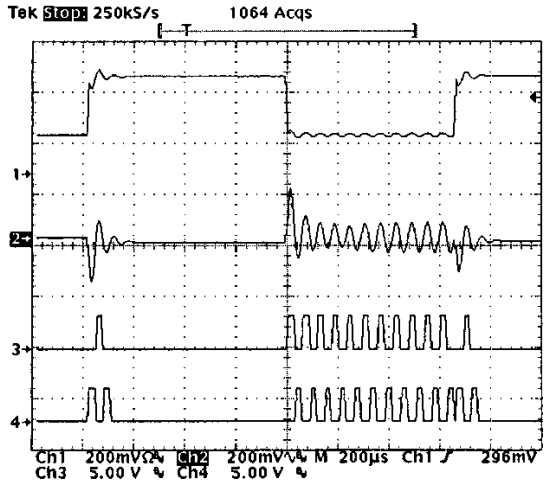

Fig. 14. Experimental waveforms in the example of Section VI.C; Ch1: load current i_{out} [200mA/div], Ch2: ac-coupled output voltage v_{out}, Ch3: A/D comparator output y, Ch4: A/D comparator output x.

response [10]. As an example, for a buck converter having the control-to-output transfer function:

$$G_{vd}(s) = \frac{V_{in}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{21}$$

the impulse response of which is $g(t)$, we have the following bound:

$$\|G_{vd}\|_{\infty\to\infty} = \|g\|_1 = \int_0^\infty |g(t)|dt < \frac{8Q^2 V_{in}}{4Q^2-1} \frac{1}{1-e^{-\frac{\pi}{\sqrt{4Q^2-1}}}} \tag{22}$$

Assuming, as has been observed in simulations and experiments, that the DPWM output signal has the amplitude equal to q_{DPWM}, we have a *conservative* bound for the amplitude of the limit-cycle oscillation at the output:

$$\begin{aligned} \max(V_{\text{limit\_cycle}}) &< \|G_{vd}\|_{\infty\to\infty} q_{DPWM} \\ &< \frac{8Q^2}{4Q^2-1} \frac{1}{1-e^{-\frac{\pi}{\sqrt{4Q^2-1}}}} V_{in} q_{DPWM} \end{aligned} \tag{23}$$

In practice, the result (23) can be used to find the worst-case effect of the oscillation on the output voltage, regardless of the origin of the oscillation. It should be noted that (23) is a conservative result. We note again the importance of a high-resolution DPWM having small quantization level q_{DPWM} for practical realization of digitally controlled switching power converters. A comprehensive survey of high-frequency, high-resolution DPWM realizations can be found in [12].

VIII. Conclusions

This paper presents static and dynamic models of digitally controlled PWM converters including quantization effects. The models include two quantizers, an A/D converter and a digital PWM (DPWM). In the static model, a graphical method is used to conclude that the existence of a DC solution, which is a necessary no-limit-cycle condition, can be guaranteed if the compensator includes integral action and if the DPWM resolution is sufficiently high. When the DC loop gain is large but not infinite, no DC solution exists and a limit cycle oscillation will happen. A dynamic model including quantization effects is derived using the describing function method. A concept of amplitude and offset dependent gain is introduced to complete the quantizer models. Under the assumption of sinusoidal signals, the dynamic system model can be used to predict the oscillation frequency and amplitude, if a limit cycle exists, and to establish no-limit-cycle conditions in terms of the A/D resolution, DPWM resolution, and the gain margin. For cases when the sinusoidal signal approximation is not met, we have found bounds for the amplitude of oscillations if a limit cycle exists.

The no-limit-cycle conditions and the amplitude bounds results point to the importance of high-resolution DPWM designs in practical realizations of digitally controlled switching power converters.

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