Stability of the Fast Voltage Control Loop in Power Factor Correctors

Aleksandar Prodić
Department of Electrical & Computer Engineering
University of Toronto
Toronto, ON M5S 3G4, Canada
Email: prodic@power.ele.utoronto.ca

Dragan Maksimović
Colorado Power Electronics Center
ECE Department
University of Colorado at Boulder
Boulder, CO 803092-0425, USA
Email: maksimov@colorado.edu

***Abstract*—This paper introduces a new method for stability analysis and design of a fast voltage loop in rectifiers with power factor correction (PFC). The method is based on the circle criterion, which unifies tools for nonlinear system analysis with frequency domain analysis tools used in linear systems. The controller design procedure is demonstrated and experimentally verified on two experimental systems that are built around a 300W digitally-controlled boost-based PFC. In the first system, the expansion of the voltage loop bandwidth is allowed by introduction of a self-tuning comb filter (STCF) for the output voltage ripple elimination. In the second experimental set-up, the fast voltage loop is enabled through utilization of a "dead-zone" in analog-to-digital conversion.**

I. INTRODUCTION

A conventional power factor correction (PFC) rectifier based on a high-frequency switching power converter consists of a power stage controlled by two interconnected feedback loops, a wide bandwidth current loop and a slow voltage loop. The purpose of the current loop is to make the input port of the PFC behave as an emulated resistor. This is accomplished by forcing the input current of the PFC to follow the wave-shape of the input voltage source. The voltage loop's task is to keep the output voltage regulated by changing the ratio between the input voltage and the current, *i.e.*, by changing the emulated resistance R_e. An equivalent circuit of the PFC is shown in Fig. 1 [1]. The power stage with the wide bandwidth current loop is modeled as an emulated lossless resistor R_e and a controlled power source. The power delivered by the source can be expressed as [1]:

$$p_{ac}(t)=\frac{2\cdot V_{g,rms}^2\sin^2(\omega t)}{R_e}=V_{g,rms}^2\left(1-\cos(2\omega t)\right), \qquad (1)$$

where $V_{g,rms}$ is the rms value of the input line voltage. Since this power has a dc component and a component at twice the line frequency, there is an output voltage ripple at twice the line frequency (and harmonics) across the output filter capacitor C. The voltage loop cannot attempt to remove this ripple because this would cause the emulated resistance to change at the frequency higher than the line frequency, and consequently would result in a significant distortion of the input current waveform [1, 2].

The most common solution is to minimize the voltage ripple's influence by closing the voltage control loop at a frequency significantly lower than the ripple frequency (usually 10-20 Hz). The main shortcoming of this approach is a slow response to disturbances in the circuit, which may result in additional stresses on the components and requires over-design of the PFC and a downstream dc-to-dc converter.

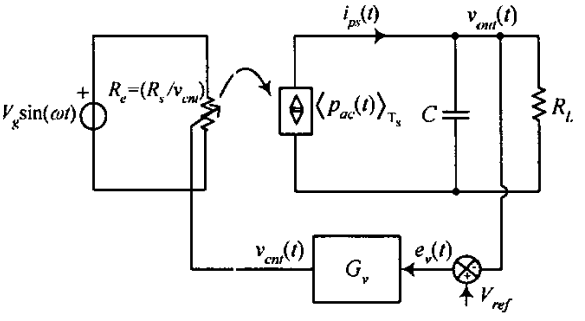


Fig.1 Large signal model of a PFC circuit

In order to eliminate the ripple's influence and enable faster voltage control loop, various methods have been proposed [3-11], including ripple cancellation [3-6], regulation band circuit [3-5, 7], digital filtering of the voltage ripple [10], or utilization of a "dead zone" in analog-to-digital conversion [11]. A problem associated with the fast voltage loop design is that the nonlinear time-varying nature of the system does not allow application of traditional stability analysis and compensator design techniques. A method for fast voltage loop design was presented in [6], but only for the specific ripple-feedback cancellation scheme proposed in the same paper.

In this paper, we present a new, more general method for the stability analysis and design of a fast voltage loop controller, which can be applied with many previously developed techniques for elimination of the ripple's influence in the voltage loop. The proposed method, based on the circle criterion [12], can be used to confirm the system stability under all operating conditions.

The paper is organized as follows: the problem of nonlinear, time-varying nature of the fast voltage loop is addressed in Section II. In Section III, an introduction to the circle criterion is given. Two design examples which shown how the circle criterion can be applied for the stability analysis of the fast voltage loop are given in Section IV. In Section V, experimental results illustrating the fast voltage loop operation are presented.

0-7803-8399-0/04/$20.00 ©2004 IEEE.

II. TIME-VARYING NONLINEAR NATURE OF THE FAST VOLTAGE LOOP

The large-signal PFC model shown in Fig. 1 is a time-varying nonlinear system. The output voltage has nonlinear dependence on the instantaneous power from the power source, which varies at twice the line frequency. In addition, the instantaneous power depends on the magnitude of the line voltage and on the ratio R_s/v_{cnt}, where R_s is the gain of the sensor for the input current measurement, and v_{cnt} is the signal at the output of the voltage loop compensator G_v. The conventional modeling method used in the design of a slow voltage loop is based on averaging the voltage loop waveforms over the line period, and then on linearization of the resulting large-signal averaged model [1]. This method cannot be applied here. Since the voltage loop bandwidth is much wider, time-varying components at twice the line frequency and beyond cannot be neglected. The approach proposed in this paper to address the fast voltage loop design in the system of Fig. 1 is based on the circle theorem [12], which is briefly described in the next section.

III. CIRCLE CRITERION

The *circle theorem* [12] results in a method for analysis of nonlinear time-varying systems, and gives a sufficient condition for the closed loop system stability. This theorem provides a link between the tools for nonlinear system analysis and the transfer function concepts used in the linear control theory. In this section, we summarize the results that we use in the method proposed in this paper. The system under consideration is shown in Fig. 2. It consists of a linear-time invariant element, with transfer function $H(j\omega)$, and a time-varying nonlinear block N.

The stability of this closed loop system is assessed through three main steps. First, the nonlinear element is characterized with a sector $\{\alpha,\beta\}$, which bounds the graph that characterizes N in the input-output plane. Next, based on the sector's size in the input-output plane, the complex plane is divided into two parts: a critical region (a circle or a half-plane), and the remaining region ("stable section"). Finally, the frequency response of the linear part in the complex plane is plotted (as a Nyquist diagram). The system is stable if the Nyquist diagram stays away from the critical region.

A. Sector $\{\alpha,\beta\}$ and the product sector

In this part, the sector $\{\alpha,\beta\}$ and the product sector, which is important for the stability analysis of the fast voltage loop with multiple nonlinearities, are introduced.

Restrictions set on the nonlinear element and important definitions for the analysis that will be presented in the following sections are listed below:

- N is assumed to be inside a sector $\{\alpha,\beta\}$, which means that $N(x)$ satisfies the inequality $\alpha x < N(x) < \beta x$, where x is the input and $N(x)$ is the output of the nonlinear element. In other words, N is inside the sector $\{\alpha,\beta\}$ if its graph lies in the segment of the input-output plane bounded by two lines, with slopes α and β, respectively.
- Additionally, it is assumed that N is incrementally inside the sector $\{\alpha,\beta\}$, where β is a positive number. This means that slope (incremental gain) of N is also limited by the gains α and β,

$$\alpha \le \frac{[N(x)-N(y)]}{x-y} \le \beta . \qquad (2)$$

- For the case when a nonlinear system consists of several nonlinearties connected in series, the sector $\{\alpha,\beta\}$ of the system can be defined as the product sector of the sectors that bound the system's nonlinearities [12]. The product sector of the sectors $\{\alpha_1,\beta_1\}$ and $\{\alpha_2,\beta_2\}$ is the sector $\{\alpha,\beta\}=\{\alpha_1,\beta_1\}\times\{\alpha_2,\beta_2\}$ defined by the interval of real numbers:

$$[\alpha,\beta]=\{xy,\ x\in[\alpha_1,\beta_1] \text{ and } y\in[\alpha_2,\beta_2]\}, \qquad (3)$$

i.e., the product sector can be described as a point-wise product of the corresponding intervals, $\{\alpha,\beta\} = \{\alpha_1\alpha_2, \beta_1\beta_2\}$.

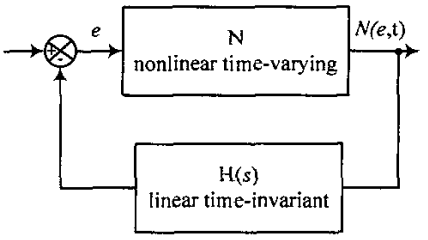


Fig.2 Block diagram of a closed loop system, consisting of a time-varying nonlinear block N and a linear time-invariant block H.

B. Critical region

The slopes α and β of a sector $\{\alpha,\beta\}$, define the critical region in the complex plane.

In the complex plane, for $\alpha > 0$ the critical region is a disc whose center is halfway between the points $-1/\alpha$ and $-1/\beta$, and whose diameter is greater than the distance between these two points. For the case when α equals 0, the critical region becomes a half-plane bounded by the vertical line that crosses the point $-1/\beta$.

The critical region divides the complex plane into two sections, stable and unstable. These two regions combined with the Nyquist plot of the linear part of the system $H(j\omega)$ can be used for the stability assessment.

C. Stability assessment based on the circle criterion

According to the circle criterion [12], the closed loop system of Fig. 2 is bounded-input bounded-output stable if the nonlinearity is inside the sector $\{\alpha,\beta\}$, and if the frequency response of the linear part $H(j\omega)$ avoids the critical region in the complex plane, *i.e.*, if the Nyquist plot of $H(j\omega)$ does not enter or encircle the critical region (circle or half plane).

IV. Stability Analysis and Controller Design Based on the Circle Criterion

In this section we show how the circle criterion can be used for the assessment of the voltage loop's stability and for the design of a linear compensator that provides a fast dynamic response of the voltage loop. In order to show the versatility of the proposed controller design method, the procedure is demonstrated on two examples. In the first example, the expansion of the voltage loop bandwidth of a digitally controlled universal PFC rectifier is enabled using a self-tuning digital comb filter (STCF) [10]. In the second example, the expansion is made possible though utilization of a dead-zone in analog-to-digital conversion [11].

In both cases, the design procedure consists of three main steps. First a separation of the system into nonlinear and linear parts is performed, then the critical sector and the corresponding critical region are defined, and finally through the compensator design, the frequency response of the linear part is shaped to avoid the critical region and to provide a fast response of the system.

A. Fast voltage loop with STCF

A large signal model of the system under consideration is shown in Fig. 3. A self-tuning comb filter, which eliminates the ripple components at twice the line frequency and the harmonics, is inserted in the voltage loop. The magnitude and phase characteristics of the STCF are also shown in Fig. 3.

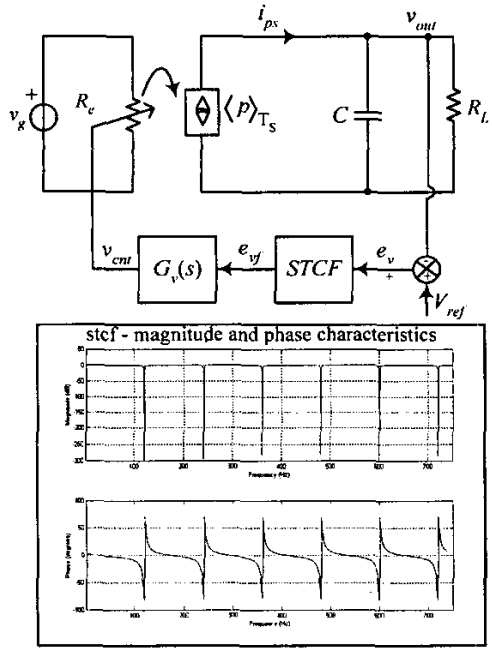


Fig.3 Voltage loop of a PFC with STCF for ripple elimination [10]; Top: functional block diagram; Bottom: frequency response of the STCF.

Based on the output voltage ripple, the filter automatically tunes frequencies with maximal attenuation (notches) to match the frequency of the output voltage ripple. As a result, a ripple-free signal is e_{vf} is obtained at the input of the voltage loop compensator $G_v(s)$.

1) Separation of the system

In order to analyze this system and obtain a structure similar to the one shown in Fig. 2, the system of Fig. 3 is redrawn and separated into linear and nonlinear parts, as shown in Fig. 4.

The nonlinear part is obtained by replacing the power source of the input port with a voltage-controlled current source:

$$\langle i_{PS}(t) \rangle_{T_S} = \frac{\langle p(t) \rangle_{T_S}}{V_{out}}$$

$$\langle i_{PS}(t) \rangle_{T_S} = \frac{V_g^2 \sin^2(\omega t)}{R_e V_{out}} = \frac{V_g^2 \sin^2(\omega t)}{R_S V_{out}} \cdot v_{cnt}(t) \,. \qquad (4)$$

where it is assumed that the DC value of the output voltage V_{out} is much larger than the ripple component. It is also assumed that the instantaneous power delivered by the input port is equal to the value $\langle p(t) \rangle_{Ts}$ obtained by averaging over a switching period [1].

The linear part of the system consists of a parallel connection of the output load and the output filter capacitor, the STCF filter for ripple elimination, the voltage loop compensator G_v.

2) Determination of the Critical Sector

A critical sector that describes the nonlinear part of the system (the current source i_{ps}) is defined by two nonlinearities: a time-varying gain $sin^2(\omega t)$ and a nonlinearity caused by the variable magnitude of the input signal V_g, which for universal-input PFC rectifiers can span a range of more than 3 to 1. The critical sector for the first nonlinearity $\{\alpha_1,\beta_1\}$ is only limited by the value of $sin^2(\omega t)$, which varies between 0 and 1. Hence, the sector $\{\alpha_1,\beta_1\}$ is $\{0,1\}$. The boundaries of the second critical sector are defined by the minimum and the maximum *rms* voltage

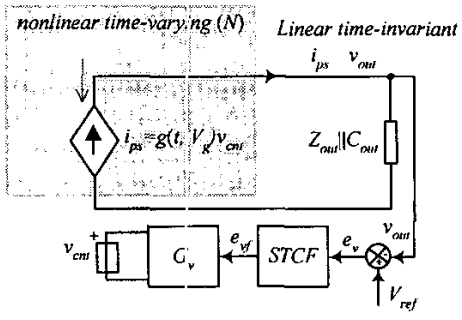


Fig.4 Separation of the PFC's voltage loop with STCF into nonlinear and linear parts

values in universal-input PFC rectifiers (V_{gmin} = 80 V_{rms} and V_{gmax} = 260 Vrms). Therefore, the second critical sector is

$$\{\alpha_2,\beta_2\}=\left\{\frac{2V_{g\min}^{\ 2}}{R_sV_{out}},\frac{2V_{g\max}^{\ 2}}{R_sV_{out}}\right\}. \quad (5)$$

In accordance with the results given in Section III, the system can be described with the product sector $\{\alpha,\beta\}$:

$$\{\alpha,\beta\}=\{\alpha_1,\beta_1\}\times\{\alpha_2,\beta_2\}=\left\{0,\frac{2V_{g\max}^{\ 2}}{R_sV_{out}}\right\}. \quad (6)$$

Also, from the results given in Section III, it can be seen that the critical sector forms a half-plane, bounded on the left-hand side by the vertical line passing through the point $(-(R_sV_{out}/(2V_{gmax}^2)), 0)$, as shown in Fig. 5.

3) Stability Assessment and Voltage Loop Compensator Design

The design of the compensator is performed in the complex plane of Fig. 5. In this plane, with the critical region determined in Step 2, the Nyquist plot of the linear part is constructed.

The compensator design is performed by having in mind two goals: first to avoid the critical region, and second to provide a fast response by keeping the "instantaneous loop gain" larger than one, during the largest portion of the line voltage period.

The transfer function of the linear part is defined as

$$H(j\omega)=G_v(j\omega)H_{CF}(j\omega), \quad (7)$$

where $H_{CF}(j\omega)$ is the continuous time equivalent of the discrete-time transfer function of the digital comb filter,

$$H_{CF}(z)=\frac{1-z^{-M}}{1-z^{-1}}\frac{1-(r\cdot z)^{-1}}{1-(r\cdot z)^{-M}}. \quad (8)$$

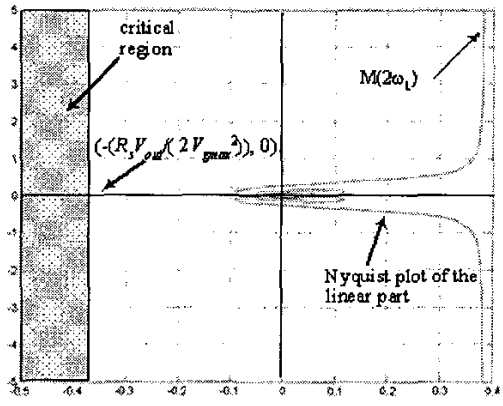
The continuous time equivalent of (8) is obtained by substituting z with $e^{j\omega}$, where $\omega = 2\pi f/f_s$, and f_s is the sampling frequency of the STCF.

The voltage loop compensator was designed by creating a digital equivalent of the continuous time compensator using digital redesign [13],

$$G_v(j\omega)=\frac{K_P}{j\omega}\left(1+\frac{j\omega}{\omega_z}\right). \quad (9)$$

The transformation of the analog compensator into its digital form is obtained using the pole-zero matching method [13].

The gain K_p, and the frequency of the compensator's zero



Fi

Fig.5 Nyquist plot of the linear part of the system in Fig. 4, together with the critical region.

$f_z = \omega_z/2\pi$ are adjusted to provide stable operation and fast transient response of the voltage loop.

As shown in Fig. 5, the stability is provided by placing the Nyquist plot of $H(j\omega)$ to the right from the vertical line $-R_sV_{out}/(2V_{gmax}^2)$, while the fast response is achieved by adjusting the magnitude of the frequency response at twice the line frequency $M(2\omega_L)$ to be greater than $(R_sV_{out}/(2\sqrt{2}V_{gmin}^2))^{-1}$. As a result, the "instantaneous loop gain" is greater than one during the largest portion of the line period, even in the case when the PFC operates at the lowest line voltage of 80 V_{rms}.

B. Fast voltage loop design for a "dead-zone" controller

In this section, we show how the design method based on the circle theorem can be used for the design and analysis of a fast voltage loop using the "dead-zone" controller described in [11]. In this digital technique, which is similar to analog methods based on a regulation band circuit [7], the output ripple elimination is accomplished through the utilization of a non-sensitive ("dead") zone in the analog to digital conversion.

In this system, a block diagram of which is shown in Fig. 6, the output voltage ripple is eliminated by setting the A-to-D quantization step V_q to be larger than the amplitude of the ripple.

The use of the A-to-D with lower resolution in this application introduces an additional gain into the feedback loop, which can be approximately characterized with the describing function [14] as shown in Fig. 7. The describing function shows that the effective gain of the analog to digital converter depends on the amplitude of the input signal. The gain varies between 0 and $4/\pi$.

Since the placement of the A-to-D in this nonlinear system cannot be changed, in order to obtain a structure similar to the one shown in Fig. 2, a worst-case design approach can be adopted. The A-to-D can be replaced with a block that has a constant (maximum) gain of $4/\pi$, and the system can be separated into linear and nonlinear parts shown in Fig.8.

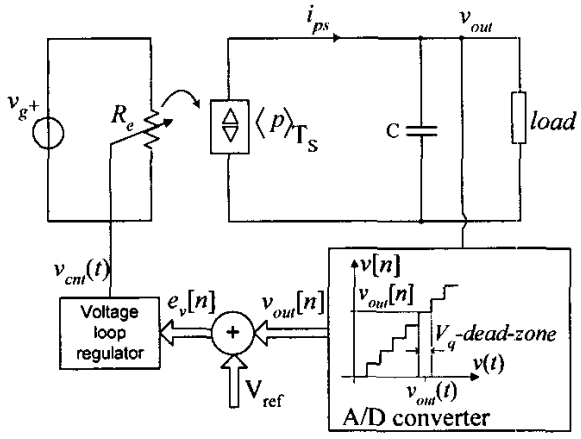


Fig.6 Block diagram of the PFC with the "dead-zone" wide bandwidth voltage loop controller [11].

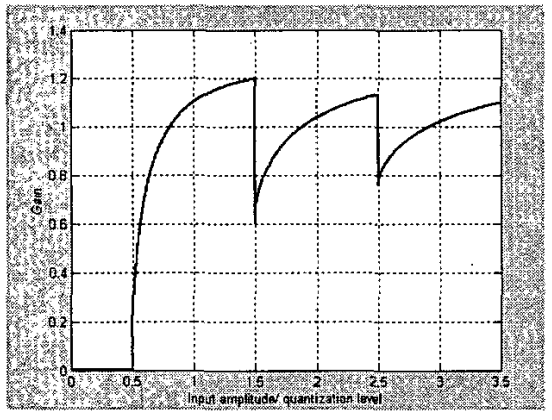


Fig.7 Describing function of the analog-to-digital converter.

After the system separation is performed, the determination of the critical region and the design of a fast controller can be performed in the same way as in the example of Section IV.A. The critical region, as well as the form of the voltage loop compensator (9), are the same. In comparison with the previous case, only the coefficients of the compensator need to be changed in accordance with the change of the characteristics of the linear part of the system. Again, in order to provide stable operation and fast dynamic response, the coefficients of the controller are adjusted to provide a frequency response of the system that avoids the critical region and provides loop gain larger than one during the largest portion of the line voltage.

V. Experimental System and Results

Both controllers described in Section IV have been tested on a 300 W boost-based completely digitally controlled PFC system, a block diagram of which is shown in Fig. 9. The system is controlled using an Analog Devices ADMC-401

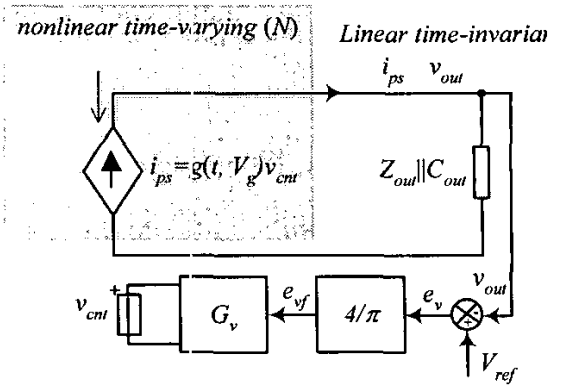


Fig.8 Separation of the voltage loop of the system in Fig. 6 into nonlinear and linear parts

DSP evaluation board and it operates at 200 kHz switching frequency.

In the first experimental set-up the self-tuning comb filter was implemented in the voltage loop, and a fast voltage loop controller is designed following the procedure described in Section IV.A. Then, the characteristics of the system are tested through load transient experiments.

The experimental results are shown in Fig. 10. It can be seen that the method provides stable operation and fast response of the voltage loop to load transients.

In the second experimental set-up, requiring only a simple change of the DSP's code, the STCF is excluded from the voltage loop, and a dead-zone controller described in [11] is implemented. The load transient experimental results of this experiment are shown in Fig. 11. The experimental results again show fast transient response and stabile operation of the experimental system.

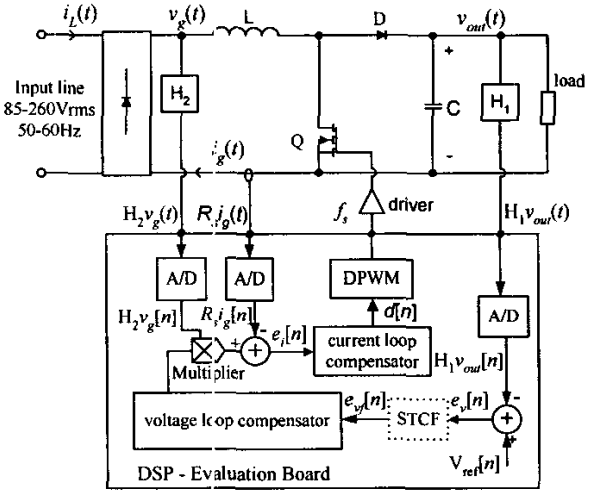


Fig.9 Experimental digitally-controlled 300 W boost PFC.

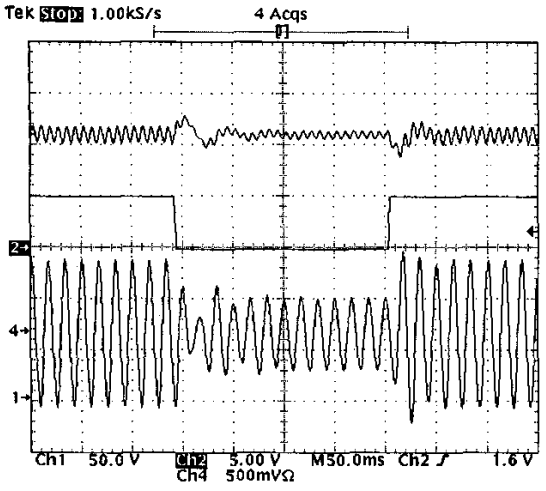


Fig.10 Load transient response of the fast voltage loop with STCF: Ch-1(top) output voltage; (Ch-2) load change between 100 watts and 200 watts; (Ch-4) input current.

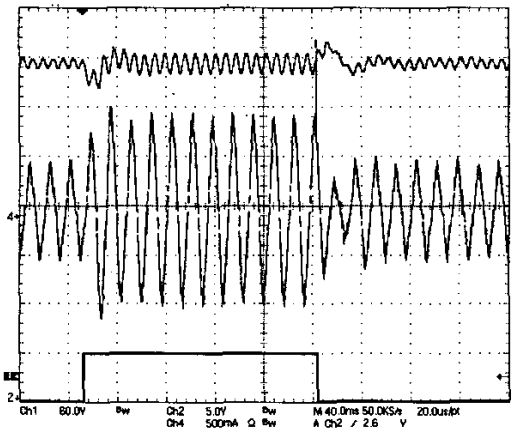


Fig.11 Load transient response of the fast voltage loop with the dead-zone controller: Ch-1(top) output voltage; (Ch-2) load change between 100 watts and 200 watts; (Ch-4) input current.

VI. CONCLUSION

A new method for stability analysis of a fast voltage loop controller in PFC application is presented and a set of guidelines for the design and implementation of a fast voltage loop compensator are given. The method, which follows directly from the circle theorem [12], is simple to use and is capable of guaranteeing the system stability under all operating conditions.

The proposed stability analysis and voltage loop design guidelines can be used with many different techniques for elimination of the influence of the output voltage ripple on the voltage loop.

The versatility of the method is demonstrated through two examples that employ different techniques for ripple elimination: a comb filter [10], or a dead-zone in analog-to-digital conversion [11]. In both cases, the experimental results show fast and stable operation of the voltage loop and verify validity of the proposed method.

REFERENCES

[1] Robert W. Erickson and Dragan Maksimović, *Fundamentals of Power Electronics*, Second Edition, Kluwer 2000.

[2] R.W. Erickson, M. Madigan, and S. Singer, "Design of a Simple High Power Factor Rectifier Based on the Flyback Converter," *IEEE APEC* 1990, pp. 792-801.

[3] G.Spiazzi, P.Mattavelli, L.Rossetto "Methods to Improve Dynamic Response of Power Factor Preregulators: An Overview" *European Power Electronics Conf. (EPE)*, 1995, Vol.3, pp.754-759.

[4] G. Spiazzi, P. Mattavelli, L. Rossetto, "Power Factor Preregulator With Improved Dynamic Response," *IEEE Power Electronics Specialists Conference*, 1995 pp. 150-156

[5] J.B. Williams, "Design of Feedback Loop in Unity Power Factor AC to DC Converter," *IEEE PESC* 1989, pp. 959-967.

[6] M.O. Eissa, S.B. Leeb, G.C. Verghese, and A.M. Stanković, "Fast Controller for a Unity-Power-Factor PWM Rectifier," *IEEE Transactions on Power Electronics*, Vol.11, No.1, January 1996, pp.1-6.

[7] J. Lazar , S. Ćuk,"Feedback loop analysis for AC/DC rectifiers operating in discontinuous conduction mode," *IEEE Applied Power Electronics Conference*, 1996. pp. 797 -806 vol.2.

[8] S. Wall and R. Jackson, "Fast Controller Design For Single-Phase Power-Factor Correction System," *IEEE Transactions on Industrial Electronics*, Vol.44, Issue 5, October 1997, pp 654-660.

[9] S. Buso, P. Mattavelli, L. Rossetto, G. Spiazzi, "Simple Digital Control for Improving Dynamic Performance of Power Factor Preregulators," *IEEE Trans. on Power Electronics*, Vol.13, 1998, pp.814-823.

[10] A. Prodić, J. Chen, R.W. Erickson and D. Maksimović: "Self-Tuning Digitally Controlled PFC Having Fast Dynamic Response", *IEEE Transactions on Power Electronics*, January 2003.

[11] A. Prodić, D. Maksimović, and R.W. Erickson, "Dead-Zone Digital Controller for Improved Dynamic Response of Power Factor Preregulators," *IEEE APEC* 2003, pp. 382-388.

[12] G. Zames, "On the Input-Output of Time-Varying Nonlinear Feedback Systems Part II: Conditions Involving Circles in the Frequency Plane and Sector Nonlinearities," *IEEE Transactions on Automatic Control*, July 1966, pp. 465-476.

[13] G.F. Franklin, J.D. Powell, and M. Workman, *Digital Control of Dynamic Systems*, 3rd edition, Addison Wesley 1997.

[14] J.H. Taylor, *Describing Functions*, article of *Electrical Engineering Encyclopedia*, Wiley 1990.