High-Frequency Digital Controller for DC-DC Converters Based on Multi-Bit Σ-Δ Pulse-Width Modulation

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Abstract-**This paper introduces a novel digital controller for low-power dc-dc switching converters that allows operation at very high constant switching frequencies and can be implemented with a simple hardware. The key components of the controller are new digital pulse-width modulator (DPWM), which is based on multi-bit sigma-delta (Σ-Δ) concept, and a dual-sampling mode PID compensator. Depending on the conditions in the converter circuit, the output voltage is either sampled at a frequency lower than the switching frequency or at the switching rate. The undersampling, which is used in steady-state, minimizes power consumption of the controller. During transients, to achieve fast dynamic response, the controller samples at the switching rate.**

Operation of the controller is verified with an experimental FPGA system and an integrated circuit (IC), which utilizes the Σ-Δ DPWM architecture, is designed. Pulse-with modulated signals produced by the new IC at frequency of 115 MHz are obtained and closed loop operation with a 2 W buck dc-dc that switches at 2 MHz is demonstrated.

I. Introduction

Digital control of low-power switch-mode power supplies (SMPS) can result in significant improvements of the supplies characteristics. It has been shown that the digital control offers advantages, such as simple introduction of advanced control and power management techniques [1-5], use of automatic design tools for fast implementation, low sensitivity to external influences [6,7], and realization with a small number of external passive components [2-9]. Although the advantages are known, in low-power portable devices, such as mobile phones and PDA-s, high-frequency analog controlled SMPS are mainly used. At high switching frequencies the analog controllers exhibit considerably lower power consumption, and consequently provide significantly better overall efficiency of the SMPS.

The inefficient operation of digitally controlled SMPS is mostly due to high power consumption of digital pulse-width modulators (DPWM) [3-5,8-10]. The consumed power is usually proportional to the product of the switching frequency and the resolution of the DPWM. This product limits the maximum frequency at which DPWM controllers can be effectively used.

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On the other hand, controllers that do not require pulse-width modulators are usually not preferred in low-power portable applications. They mostly operate at non-constant switching frequencies and introduce wide-bandwidth noise that affects operation of the supplied devices.

Recent publications [3,4,8-10] have demonstrated low-power high-resolution DPWM controllers that can operate at switching frequencies between 400 kHz and 1 MHz. Those digital systems are still slower than several high-frequency commercial analog solutions [11,12]. Also, they probably will not be able to control upcoming low-power SMPS, which are expected to operate at frequencies significantly higher than 1 MHz [13]. The DPWM architecture that supports operation at frequencies up to 15 MHz [5] cannot be used either. It is primarily designed for higher power applications and is not suitable for mobile phones and similar low-power devices.

The main goal of this paper is to introduce a new digital controller for SMPS that allows power efficient operation at constant switching frequencies significantly higher than 1 MHz.

Figure 1 shows block diagram of the new controller that can be implemented with a simple hardware. It combines novel functional blocks, a multi-bit sigma-delta digital pulse-width modulator (Σ-Δ DPWM) and a dual-sampling compensator.

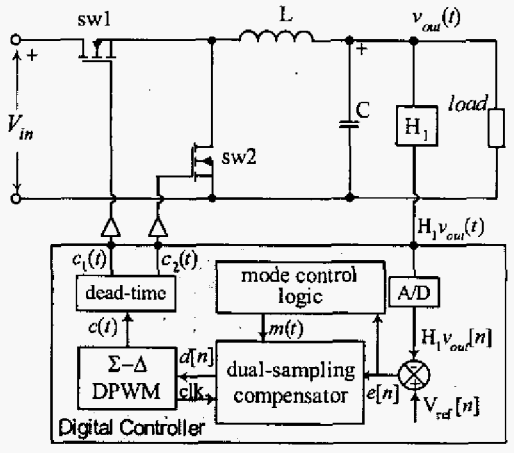

Fig.1. A buck converter regulated with Σ-Δ DPWM controller.

The paper is organized as follows. In Section II the high-frequency low-power Σ-Δ DPWM is described. Section III explains the dual-sampling compensator. The prototype system and experimental results are presented in Section IV. Section V summarizes the main results of this paper.

II. DPWM BASED ON MULTI-BIT SIGMA-DELTA CONVERSION (Σ-Δ DPWM)

New multi-bit sigma-delta architecture eliminates the need for power dissipative high-frequency high-resolution DPWM-s and consequently allows efficient operation at high switching frequencies.

The Σ-Δ DPWM shown in Fig.2 is based on the well-known sigma-delta modulation concept [17]. It consists of a *high-frequency low-resolution DPWM*, a delay block, and two adders. For the case shown in Fig.2, the low-resolution DPWM is a 3-bit unit that changes duty ratio of the pulse-width modulated signal $c(t)$ between eight possible discrete values: 0, 0.125, 0.25, 0.375, 0.5, 0.675, 0.75, and 0.875. The duty ratio is varied over several switching periods to result *in an average value that has high-resolution* (high effective resolution). The high resolution is necessary for the tight output voltage regulation and for the elimination of undesirable quantization effects [14-16]. The value of the duty ratio is set by the high-resolution digital control command $d[n]$ and the averaging process is performed by the switching converter itself (see Fig.1). The effective averaging is possible as long as the corner frequency of the converter $f_c=1/(2\pi\sqrt{LC})$ [18] is significantly lower than $f_{av}=1/T_{av}$, where T_{av} is the averaging period.

Table I shows a sequence of Σ-Δ DPWM's state values and the average value of the duty ratio D. It is assumed that the initial state of all variables is zero and that 9-bit command $d[n]$ is equal to 0.3 (decimal). It can be seen that D closely approaches $d[n]$ over just several switching cycles.

The fast convergence toward the high-resolution value, i.e. short averaging period, is provided with the internal loop of the Σ-Δ DPWM, whose model is shown in Fig.3. The pole at zero (i.e. at $z=1$) forces the average value of $e_D[n]$, the difference between high-resolution $d[n]$ and the low-resolution command of 3-bit DPWM $d_{LR}[n]$, to be zero and effectively increases the resolution of the internal DPWM.

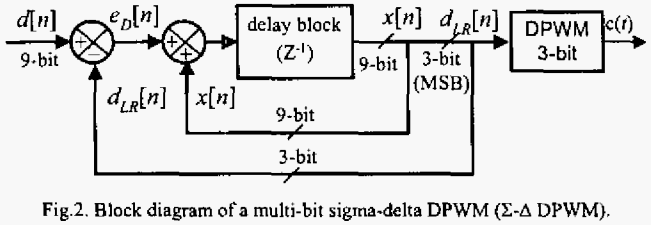

Fig.2. Block diagram of a multi-bit sigma-delta DPWM (Σ-Δ DPWM).

Table I – A signal sequence of the Σ-Δ DPWM

n	d[n]	$e_D[n]$	x[n+1]	x[n]	$d_{LR}[n]$	duty ratio of c(t)	Average D $D=\sum_{i=1}^{n}\frac{d_{tr}[i]}{n}$
1	0.3	0.3	0.3	0	0	0	0
2	0.3	0.3	0.6	0.3	0.25	0.25	0.125
3	0.3	0.05	0.35	0.6	0.5	0.5	0.25
4	0.3	-0.2	0.4	0.35	0.25	0.25	0.25
5	0.3	0.05	0.45	0.4	0.375	0.375	0.275
6	0.3	-0.075	0.375	0.45	0.375	0.375	0.2916
7	0.3	-0.075	0.3	0.375	0.375	0.375	0.303
8	0.3	-0.075	0.225	0.3	0.25	0.25	0.296

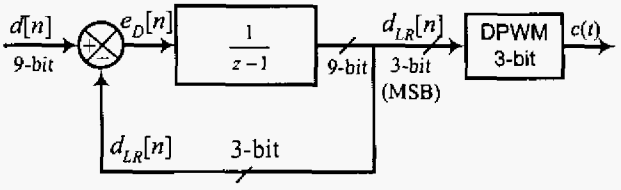

Fig.3. Dynamic model of the Σ-Δ DPWM.

A. Effective resolution of Σ-Δ DPWM

To find the effective resolution of the Σ-Δ DPWM we used general analysis of the sigma-delta concept, which is based on the signal-to-noise ratio (SNR) comparison [17]. The analysis shows that Σ-Δ modulation improves the resolution of the internal DPWM by 1.5 bits with every switching period added to the averaging sequence.

This means that the effective resolution of the Σ-Δ DPWM, D_{eff}, is approximately equal to

$$D_{eff} = D_{LR} + 1.5(N_{AV} - 1) \text{ bits} \qquad (1)$$

where, D_{LR} is the number of bits of the low-resolution DPWM, and N_{AV} is the number of switching periods taken into averaging sequence.

From (1) it can be seen that, in the system of Fig.2, the effective resolution of 9 bits can achieved by averaging the output of the 3-bit DPWM over 5 switching periods.

B. Dynamic model

The discrete transfer function of the Σ-Δ DPWM, $H_{\Sigma\text{-}\Delta}(z)$ can be derived from the model of Fig.3 and written as:

$$H_{\Sigma\text{-}\Delta}(z) = \frac{C(z)}{D(z)} = \frac{C(z)}{D_{tr}(z)} \cdot \frac{D_{tr}(z)}{D(z)} = z^{-1} H_{dpwm}(z) \qquad (2)$$

where, $H_{dwpm}(z)$ is the transfer function of the low resolution DPWM. It can be seen that the Σ-Δ DPWM causes delay of one switching cycle and consequently introduces additional phase shift into the system.

The negative influence of this delay can be minimized using dual-sampling compensation presented in the following section.

III. Dual Sampling/Clocking Mode Compensator

This section describes a new digital compensator suitable for the use with the Σ-Δ DPWM as well as with other low-power high-frequency DPWM architectures. The compensator utilizes dual-sampling scheme, which results in low power consumption of the controller and in fast transient response to disturbances in the switching converter circuit.

Figure 4 shows block diagram of the compensator for the case when the effective 10-bit resolution is obtained using a 4-bit low-resolution DPWM. The attenuated output voltage of the switching converter $Hv_{out}(t)$ (Fig.1) is transformed into its digital equivalent $Hv_{out}[n]$ with a *windowed A/D* [2], and then compared to the reference value $V_{ref}[n]$. The windowed A/D produces one of only nine possible discrete values of the errors signal $e[n]$ (from -4 to +4). A compensator based on look-up tables [8] (LUT Compensator) processes the error and, depending on conditions in the circuit, creates $d_{dy}[n]$ and $d_{ss}[n]$, the control signals for the Σ-Δ DPWM. The error is also monitored with the *hysteretic logic & clock divider* block and based on its value the mode of the controller operation is set.

A. Steady-state mode

As long as the error $e[n]$ is small, in the range of -2 to +2, the compensator operates in steady-state mode with low power consumption. In this mode the frequency of the clock signal clk 1, which synchronizes operation of system, is lower than the switching frequency and the output voltage is sampled every sixth cycle. Accordingly, the high resolution control value $d_{s-s}[n]$ is updated every sixth cycle and high effective resolution of the Σ-Δ DPWM is achieved.

The undersampling also minimizes phase shift caused by the delays of all elements of the control loop, including the one switching cycle delay introduced by the Σ-Δ DPWM (2). This is because the phase shift, which is proportional to the ratio of the delay and the sampling period [19], decreases when the sampling period increases.

B. Dynamic mode

To improve limited dynamic response of the steady-state operation, *dynamic mode* is introduced.

Compensator switches into dynamic mode asynchronously. At the moment when the input voltage of the A/D is high or low enough to cause absolute error $e[n]$ larger than 2 the mode bit is set high and the compensator instantaneously enters into the dynamic mode.

In the dynamic mode, using the multiplexer, the hysteretic logic bridges the internal feedback of the Σ-Δ DPWM. It also changes the clock rate of the system, and alters the control law of the LUT. In this mode, the fast DPWM inside the Σ-Δ DPWM is fed by a low resolution control value d_{dy}[n], which is updated every switching cycle.

The controller stays in the dynamic mode until the absolute value of the error drops bellow 2. Then, it switches back to the steady state.

IV. Experimental System and Results

To test the presented concepts a prototype system around a low-cost FPGA evaluation board was built and an IC based on the new Σ-Δ DPWM architecture was designed

A. FPGA Implementation

Operation of the new controller is experimentally verified with a prototype system based on an FPGA development board. First a Σ-Δ DPWM, based on the block-diagram of Fig.2 was constructed and then the closed loop operation was tested.

In the implementation of the Σ-Δ DPWM as the low-resolution DPWM, a ring oscillator based [10] 3-bit DPWM was used. The delay cells of the ring oscillator were constructed of D-flip-flops, which typical propagation time is 2.5 ns.

Figure 5 shows pulse-width modulated waveforms when the control command $d[n]$ (see Fig.2) changes between two 9-bit values.

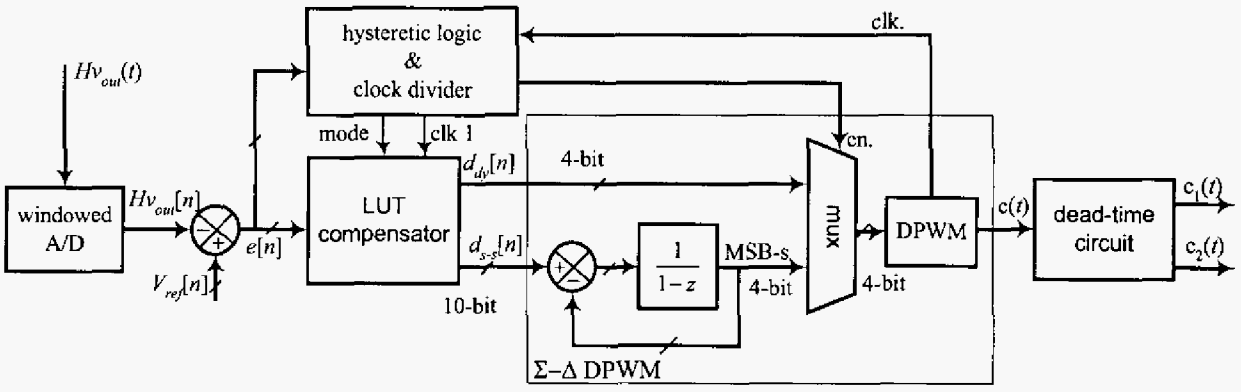

Fig.4. Dual-sampling mode digital compensator.

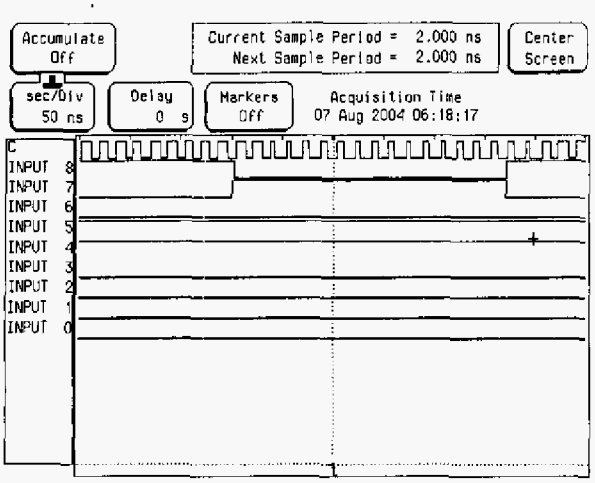

Fig.5. Pulse width modulated waveforms at 60 MHz produced by Σ-Δ DPWM (logic analyzer snapshot). *c*- pulse width modulated output signal; inputs 0 to 8 create binary control value *d*[*n*].

Pulse-width modulated signals at very high constant frequency of 60 MHz are demonstrated. It can be seen that even in FPGA implementation the Σ-Δ DPWM allows operation at extremely high switching frequencies.

A.1. Closed loop operation

The construction of the closed loop system is based on the block diagrams shown in Figures 1 and 4. To limit the switching losses we designed a buck converter to operate at switching frequency of 2 MHz, and accordingly decreased the frequency of the Σ-Δ DPWM. To decrease the frequency, a 4-bit DPWM based on ring oscillator was implemented and each of the delay cells was replaced with a block of four D-flip-flops connected in series.

The buck converter is designed to operate with regulated output of 3.3 V when the input voltage varies between 4 and 10 V. The maximum output current is 1 A.

Figure 6 shows operation in the steady-state mode. It can be seen how the Σ-Δ DPWM controller varies the duty ratio (i.e. t_{on} times) over successive switching periods to maintain well-regulated output voltage.

Results of the measurement of the load transient response for the output load changes between 0.1 A and 1 A are shown in Fig.7. Upon the transient the dynamic mode is activated with the high value of the control signal *mode* (see Fig.4) and the controller quickly reduces the overshoot caused by the load change. In the second phase, when the output voltage approaches regulated value, the *mode* signal goes low, and the controller returns to the steady-state, which has improved voltage regulation. It can be seen that dual sampling technique results both in good output voltage regulation and fast dynamic response.

B. Σ-Δ DPWM Integrated Circuit (IC)

To estimate the area needed for on-chip implementation and power consumption of theΣ-Δ DPWM, as well as, the range of achievable switching frequencies, an integrated circuit based on 0.35 μm, 3.3 V, technology is designed and simulated.

The layout of the IC is shown in Fig.8. It includes a 10-bit Σ-Δ DPWM and a dead-time circuit (Fig.4) and occupies only 0.057 mm^2 off silicon area.

The low-resolution DPWM core of the Σ-Δ DPWM is based on a 4-bit ring oscillator. The complete IC is designed from standard digital cells, using automatic synthesis tools. The results of analog simulation of the IC, are shown in Figures 8 to 10, and summarized in Table II.

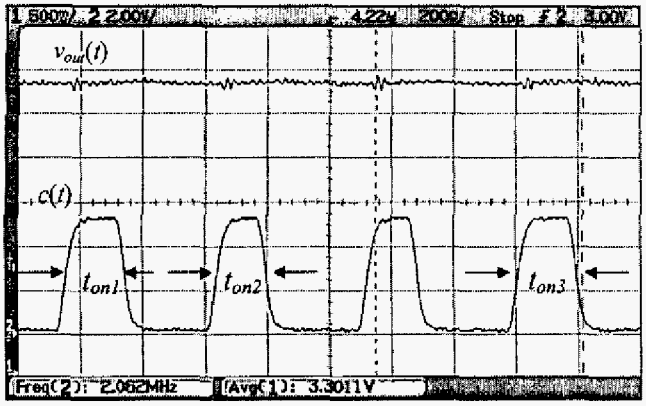

Fig. 6. Steady-state closed-loop operation of the Σ-Δ DPWM controller at 2.06 MHz switching frequency for V_{in}=8 V. Ch.1: Output voltage $v_{out}(t)$ (500mV/div); Ch.2: Pulse width modulated control signal $c(t)$. Time scale is 200ns/div.

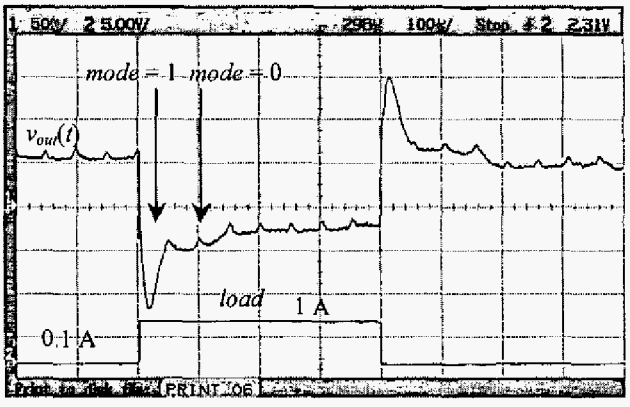

Fig. 7. Transient response for the load change between 0.1 and 1A. Ch.1: Output voltage $v_{out}(t)$ (50 mV/div – ac scale); Ch.2: load transient. Time scale is 100 μs/div.

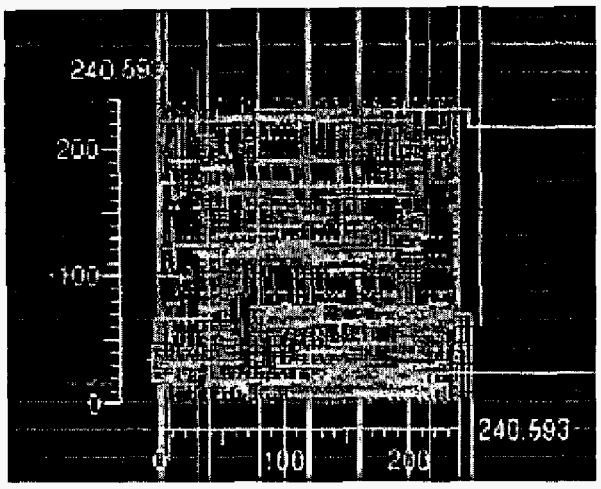

Fig. 8. Layout of the Σ-Δ DPWM designed in 0.35 μm technology (chip dimensions are 0.24 x 0.24 mm^2).

Figures 9 and 10 show pulse-width modulated waveforms of the IC operating at ultra-high switching frequency of 115 MHz. The simulation results predict that when fabricated, this IC will have current consumption of 9 mA at 115 MHz.

Simulations at other frequencies show that the average current consumption of the chip is only 80 μA/ MHz. This value is comparable to state of the art analog solutions.

Table II: Characteristics of the Σ-Δ DPWM IC

Parameter	Value
Switching Frequency	up to 115 MHz
Power Consumption	less than 80 μA/MHz
On-chip are	0.057 mm^2

V. Conclusions

This paper describes a low-power digital controller for dc-dc SMPS operating at constant switching frequencies significantly higher than 1 MHz. The main controller blocks are a novel digital pulse-width modulator, which is based on multi-bit sigma-delta conversion (Σ-Δ DPWM), and a new dual-sampling mode compensator. The Σ-Δ DPWM can be implemented with a simple low-power hardware and as such is suitable for on-chip implementation. The dual-sampling compensation allows further reduction in power consumption without penalties in dynamic performance and output voltage regulation.

Experimental FPGA-based implementation verifies advantages of the new architecture. Pulse-width modulated signals at frequency of 60 MHz are produced and closed loop operation of dc-dc converter operating at 2 MHz is demonstrated. Based on the Σ-Δ DPWM an integrated circuit is designed, the IC produces pulse-width modulated waveforms at 115 MHz and consumes very low power and on-chip area.

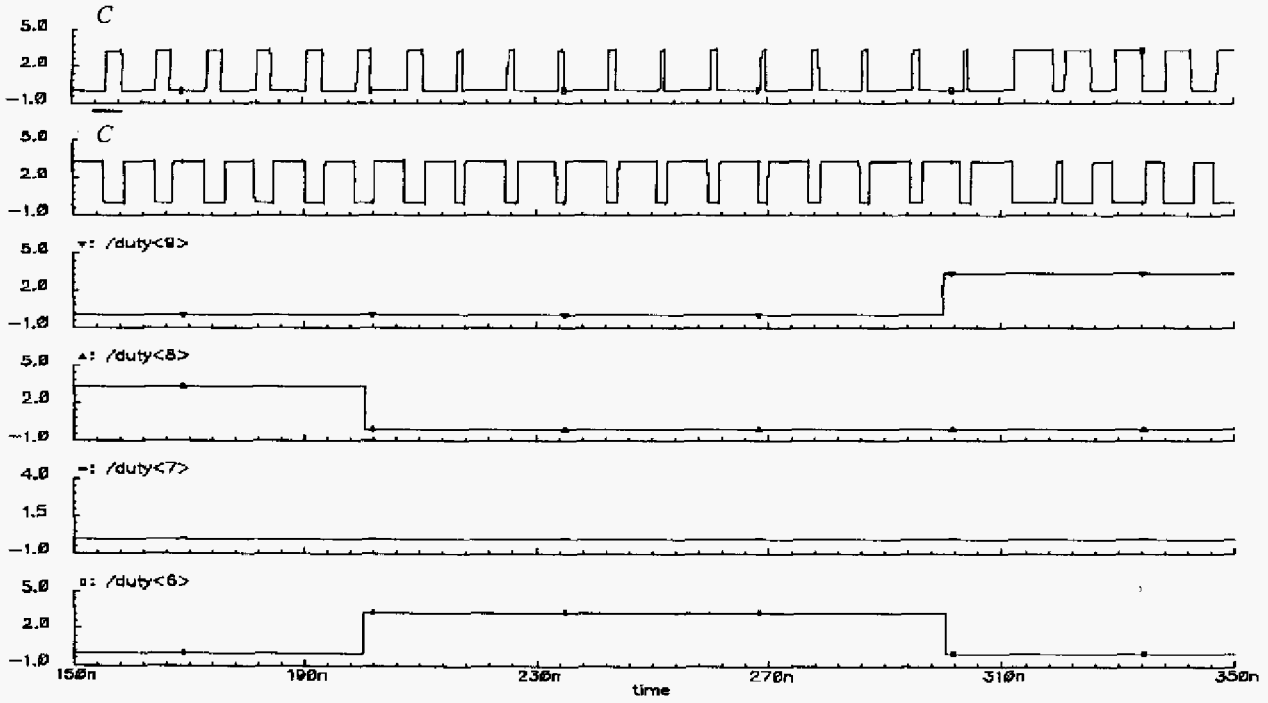

Fig.9. Simulation results: pulse-width modulated waveforms at 115 MHz produced by the Σ-Δ DPWM IC. C and $\bar{C}$ are the outputs of the dead-time circuit (Fig.4); Duty 6 to 9 are 4 most significant bits of the 10-bit input control value $d[n]$.

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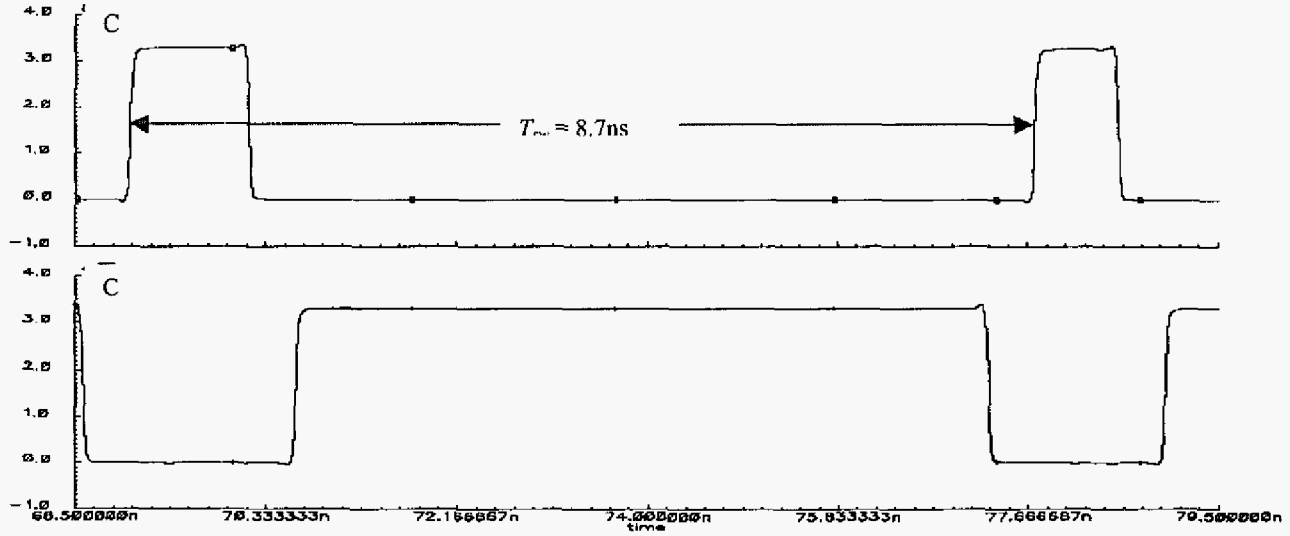

Fig.10. Simulation results: pulse-width modulated waveforms at 115 MHz produced by the Σ-Δ DPWM IC. C and $\bar{C}$ are the outputs of the dead-time circuit. T_{sw} is the period of the DPWM.