All-Digital DPWM/DPFM Controller for Low-Power DC-DC Converters

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***Abstract*— A digital controller for dc-dc switching converters used in battery-powered handheld devices is introduced. The controller can operate in two modes and encompasses novel designs of a digital pulse-width modulator (DPWM) and an all-digital pulse-frequency modulator (DPFM). The DPWM has a high resolution and can operate at very-high constant switching frequency (tens of MHz). The DPFM features very-low power consumption, programmable on-time and control over switching frequency range. An experimental FPGA prototype and an application-specific IC that employ new controller architecture are built around 3.3 V, 3W, 6 MHz buck power stage and successful operation of the digital controller in both modes is verified. The low power consumption has been also verified on a chip implemented in a standard CMOS 0.18um process.**

I. INTRODUCTION

Digital control of low-power switching converters allows numerous benefits including the ability to use digital design tools, flexibility in transferring to different implementation technology, and low sensitivity on external influences [1-6].

However, in battery-powered handheld devices, such as cell phones, digital still cameras (DSC), and personal data assistants (PDAs), analog controlled dc-dc switching converters are predominantly used. Among the main obstacles for successful digital implementation are lower switching frequency, compared to analog solutions, and the absence of low-power digital architectures that can support pulse-frequency modulation (PFM). The PFM results in significant efficiency improvement when the output loads of SMPS are light. In handheld devices, to extend the battery life, the PFM is usually used when the supplied devices perform simple processing tasks or operate in stand-by mode.

In recent publications several low-power solutions that either support only digital pulse-width modulation control or combine a digital-pulse width modulator (DPWM) and an analog PFM have been presented [7-10]. With the exception of the DPWM demonstrated in [11] most of the presented solutions operate at much lower frequencies than the analog controllers. On the other hand, digital pulse-frequency modulators (DPWM) demonstrated in [12] have not been utilized in low power switching converters. To create a pulse-frequency modulated signal, often characterized with short on and long off time intervals, these realizations use high frequency clocks and employ power-inefficient counters, which make them unsuitable for low-power applications.

In this paper we introduce a novel all-digital DPWM/DPFM controller that can be used in low-power SMPS and easily transferred from one implementation technology to another. The controller, shown in Fig 1, utilizes novel architectures of DPFM and DPWM. The DPWM operates at switching frequencies comparable to the fastest analog solutions today [13,14] and can be implemented with a low-power digital hardware. The DPFM is based on a new "racing ring" architecture that also provides very low power consumption and operation without an external clock. In addition, the DPFM utilizes advantages of digital control and offers new features not commonly seen in analog implementations. It offers digital control of the on-time (maximum transistor current) and control of the range of switching frequency operation, which can be used to eliminate undesirable frequency components that can influence supplied device.

Depending on the value of the external mode signal $m(t)$, the system of Fig.1 operates either as a digital pulse-width or pulse-frequency modulator. In pulse-width modulation mode it operates in a similar manner as the system presented in [8].

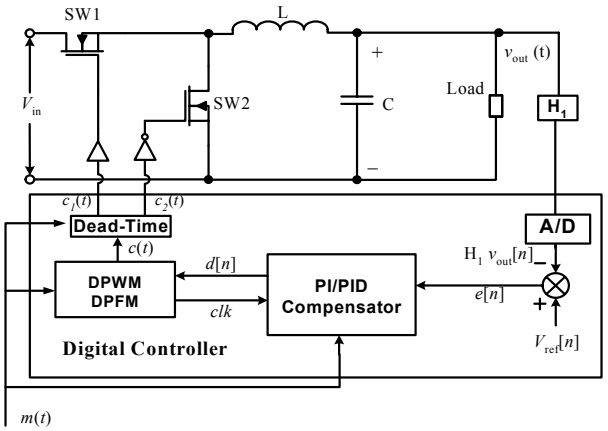

Fig. 1. Buck converter regulated by all-digital DPWM/DPFM Controller

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Based on the value of the error signal a look-up table based PID compensator creates a control signal for DPWM. When operating in pulse-frequency mode a simpler PI compensator law is used. In this case the compensator creates a control signal for DPFM, which is proportional to the switching frequency.

In the next section, the architecture and operation of the DPWM are explained. In Section III, we describe the programmable DPFM. Section IV presents the experimental results obtained with an FPGA-based controller that employs this new controller architecture. In this section we also show results obtained from an application specific IC utilizing this control method.

II. High-Frequency Digital Pulse-Width Modulator Based on Segmented Ring

The new DPWM shown in Fig.2 is a modification of segmented DPWM architecture [15] that does not require an external clock to operate. The architecture also resembles the DPWM architecture based on a ring oscillator [16], with the difference here being that the size of this structure, for 8-bit implementation, is reduced to 1/15 of the original.

The ring-based segmented architecture shown in Fig. 2 is an 8-bit DPWM. It consists of two 16:1multiplexers and two sets of delay lines connected as a ring. The first delay line consists of 16 fast delay elements in series. Each intermediate node is passed onto a 16:1 multiplexer (MUX-A), whose select signal are the 4 least significant bits (LSB) of the digital input $d[n]$ (see Fig.2). MUX-A is responsible for the fine resolution of the DPWM, as it is controlled by the 4 LSBs of $d[n]$. The second delay line consists of 15 slow delay elements in series. These delays are 16 times slower than the fast delay elements. The outputs of slow delays are connected to a second 16:1 multiplexer (MUX-B). The select signal for the MUX-B are the 4MSBs of $d[n]$ connected in reverse order, such that the MSB of $d[n]$ is tied to the LSB of MUX-B. In this way, the 4MSB of $d[n]$ define the start point of the pulse-width modulated signal, that sets the SR latch. The 4LSBs of $d[n]$, connected to the select input of MUX-A, are not reversed and define the end point of the fraction of switching period during which the PWM signal is high. This connection always ensures that the signal stop point is defined by 4LSB and hence an accurate duty ratio adjustment is achieved.

For example, when the input $d[n]$ is a high binary input, 1101 1000, which corresponds to a duty ratio value of 0.84375, the PWM waveform is created as follows. As the signal is propagating through the delay cells, it sets the SR latch at MUX-B I14. Then it goes through 14 slow cells (because the MUX-B input is 1101), moves through eight fast cells and resets the latch at MUX-A input I8 (because the MUX-A input is 1000). When the input value $d[n]$ is small, 0001 0001, the ring oscillator signal sets the SR latch at MUX-B I1, moves through just one slow and one fast cell and resets the latch after that. As a result, a small duty ratio value is obtained. It can be seen that the DPWM can be implemented with very small hardware. It takes only 1/15 of the resources needed for the implementation of a conventional 8-bit ring-oscillator based DPWM that employs a large 256:1 multiplexer.

A. DPWM Linearization Problem

As described in [15] segmented DPWM structures suffer from nonlinearity problems. The mismatch between fast and slow delay cells in some cases can cause the characteristic of the DPWM to become nonmonotonic and cause instability of the system, due to effective positive feedback.

In mixed-signal IC implementation both this problem and stabilization of the switching frequency can be solved using simple DPWM linearization block demonstrated in [16,17]. In that solution a replica of fast delay line and custom made programmable delay cells are used. The delay of 16 fast delay cells is matched to be exactly the same as the delay of a slow cell.

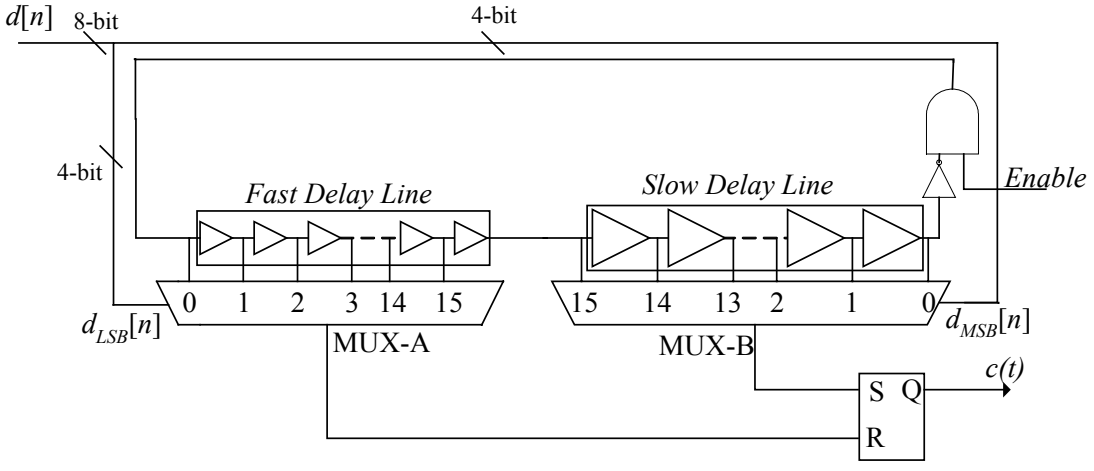

Fig. 2. Ring-based segmented DPWM

III. RACING RING BASED PROGRAMMABLE DIGITAL PULSE-FREQUENCY MODULATOR

One of the main challenges in designing a low-power digital pulse-frequency modulator (DPFM) is the creation of long time intervals using vey fast digital logic. Since the switching periods of SMPS operating in DPFM are several orders of magnitude larger than the propagation times of modern digital circuits, direct implementation of solutions used in DPWM architectures is impractical. Conventional ring oscillators would require thousands of delay cells and huge on-chip area. On the other hand, counter-based DPFM architectures [12] consume significant amount of power and silicon area, especially if a large range of frequencies are required. In portable applications, these methods are rendered useless due to their high power consumption.

The novel signal-race based DPFM architecture is shown in Fig. 3. It allows creation of very long time intervals using fast digital logic and can be implemented with low power hardware. The DPFM operation is based on the race of two signals around a ring oscillator where one signal starts first and the second signal, which propagates a little bit faster, starts a little bit later. Once the faster signal catches the first one the race is over. The period of the DPFM signal is defined by the time difference between the start of the first signal and the end of the race. In this case the duration of the race, i.e. switching period, is proportional to the time spacing between the two start signals and inversely proportional to the speed difference of the two signals, i.e. time delay of digital logic. The architecture of Fig.3 has three major functional blocks, the DPWM described in the previous section, the *End of Race* detector (EoR), and a ring oscillator that comprises of SR latches and programmable delay cells. In this case, the DPWM operates with a "broken ring" and is triggered externally, i.e. operates in the same manner as conventional segmented DPWM [15]. The DPWM creates a short pulse, whose rising and falling edges determine the time-spaced racing signals (on-time of DPFM signal).

Initial states of all the SR latches are zero. When the DPWM generator produces the positive edge, the first SR latch will be set to high. In turn, the output of the first SR latch will set the second SR latch. This is illustrated in Fig. 3 as a positive edge propagating on the upper track. When the DPWM generator produces the negative edge, the first latch will be reset to zero after being previously set by the positive edge. The output of the first latch will reset the output of the second latch. This is shown as a negative edge going down the reset line. Hence the positive and negative edge will start to chase each other around the SR latch ring, because the delay of the set delay block on the set line is made to be slightly bigger than the delay of the not gate. The delay of the DPFM is again controlled by the DPWM. Once these pulses catch up to each other, all the outputs of the SR latch will become zero, indicating that the race has ended. Each time the end of race condition is detected by the EoR block, a new signal for the DPWM is created and the race starts again. It should be noted that this control scheme provides regulation of both the switching frequency and the on-time.

IV. EXPERIMENTAL RESULTS

Based on the diagrams shown in Figures 1 to 3, an experimental system was built around an FPGA system. As a power stage, a buck converter is used and the controller is realized with a Xilinx Spartan-3 FPGA board.

As shown in Fig.1, in both modes, the switching converter is regulated with the same controller, consisting of a windowed analog-to-digital converter (ADC), digital compensator and the combined DPWM/DPFM described in previous section. No external clock is needed as in both cases the clock frequency of the system is the same as the switching frequency, resulting in very low power consumption in DPFM and fast control in DPWM. Mode selection is performed with the external mode signal.

A. DPWM Operation

Figures 4 and 5 demonstrate DPWM operation of the controller. Figure 4 show steady-state operation. It can be seen that the converter operates at a very-high constant switching frequency of 6.2 MHz, which is comparable to cutting edge analog integrated solutions. Figure 5

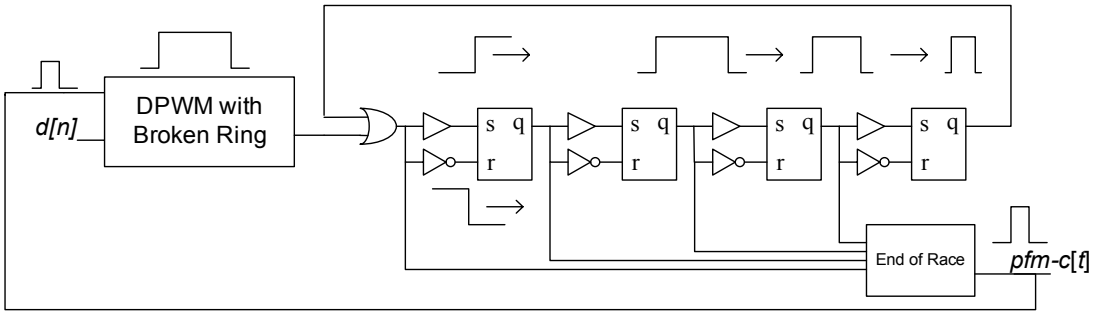

Fig. 3. All-digital DPFM

demonstrates that the controller also exhibits fast transient response.

B. DPFM Operation

DPFM operation is illustrated with Figs. 6 and 7. Figure 6 demonstrates operation of DPFM in open loop. It shows how the digital control signal, $d[n]$ affects the pulse-frequency modulated output. It can be seen that the change of $d[n]$ immediately influences the frequency of the pulse-frequency modulated signal. Operation of the DPFM in closed loop is shown in Fig. 7. From the control signal $d[n]$ and output voltage $v(t)$ it can be seen that the controller is able to provide good regulation of the output voltage by changing the frequency of operation.

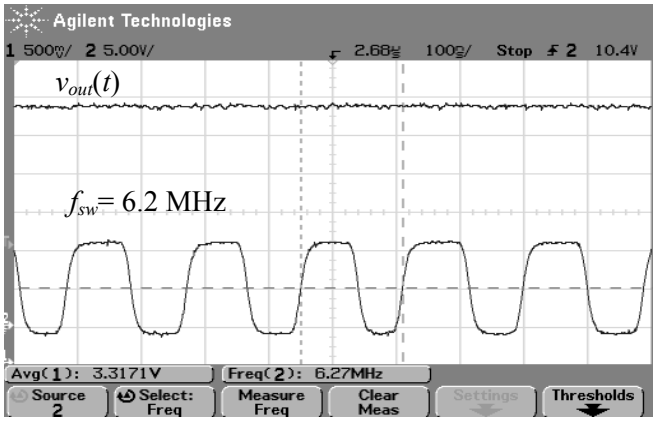

Fig. 4: DPWM operating at 6.2 MHz. Ch.1: regulated output voltage v(t); Ch.2: Gate drive signal

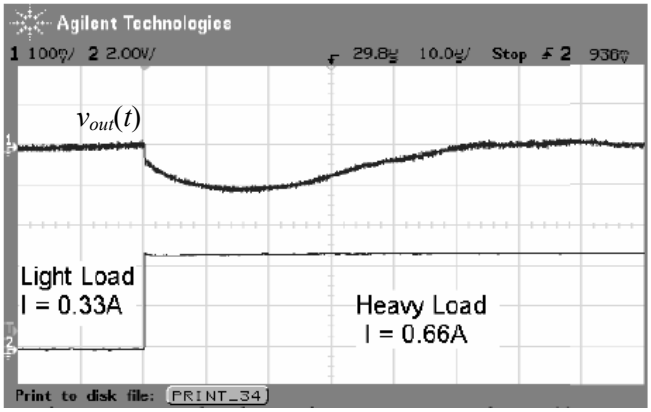

Fig. 5: DPWM load transient response. Ch.1: v(t); Ch.2: load transient control signal.

C. On-Chip Implementation

In addition to the FPGA implementation, the DPWM and the DPFM have also been implemented on a CMOS 0.18um, as a part of more complex low-power management IC described in [16,17]. The layouts of the DPWM and DPFM are shown in Fig. 8 and their characteristics are given in Table I. As it can be seen the novel architecture allows operation at very-high switching frequencies and has very small power consumption, comparable to state of the art analog PFM solutions.

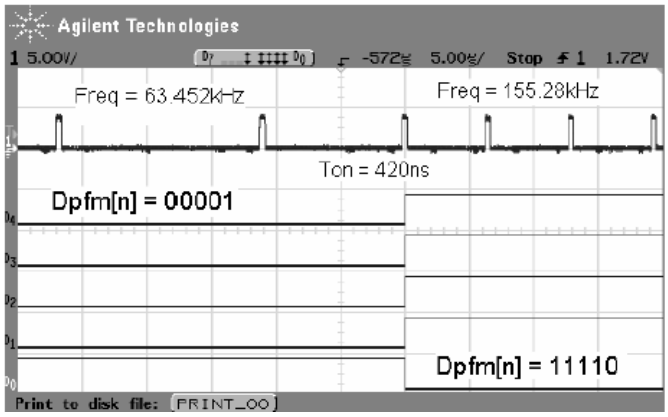

Fig. 6. DPFM operating in open loop. Ch.1: c(t) DPFM signal. D0-D4: digital control word d[n]

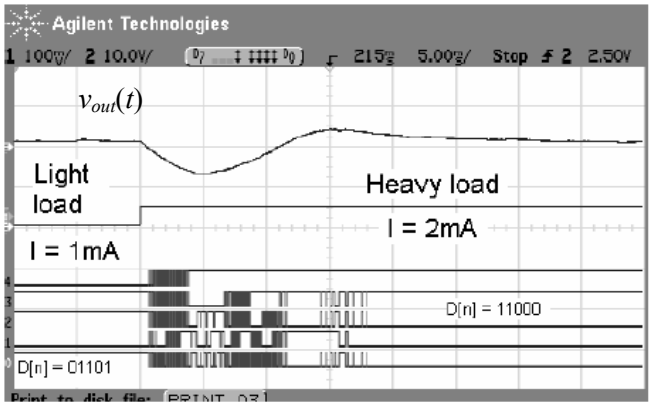

Fig. 7. Closed loop DPFM operation. Ch.1: $v_{out}(t)$; D0-D4: Digital control word d[n]

TABLE I- PARAMETERS OF ON-CHIP IMPLEMENTED DPWM AND DPFM

	Area	Frequency range	Current cons.
DPFM	0.01950 mm^2	20 kHz to 250 kHz	3 μA
DPWM	0.007710 mm^2	1 MHz to 20 MHz	5 μA/MHz

V. CONCLUSION

This paper introduces a novel digital architecture of a DPWM/DPFM controller for low-power dc-dc switching converters. The controller is all-digital, and its design can be easily transferred from one implementation technology to another. It also meets the requirements of very high frequency of operation in DPWM mode and very low power consumption in the DPFM required for low-power portable and handheld devices. Experimental FPGA prototype demonstrates operations at a very high constant switching

frequency of 6.2 MHz, as well as effective voltage regulation in DPFM operation. Furthermore, on-chip implementation of this architecture verifies ultra-low power consumption, comparable to state of the art analog solutions.

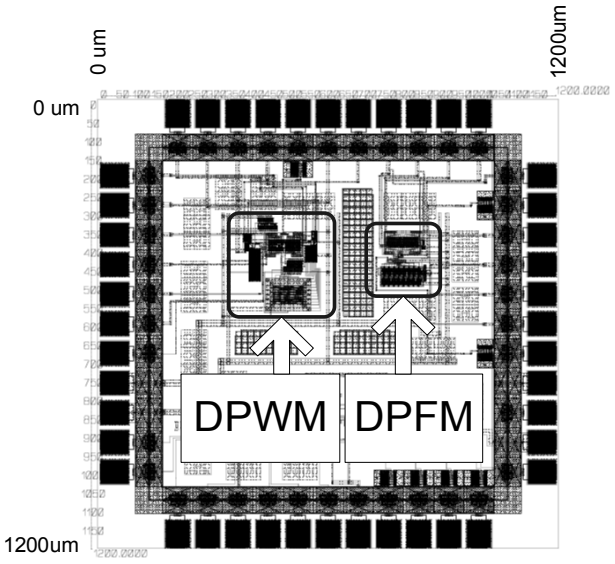

Fig. 8. Layouts of DPWM and DPFM implemented in a standard CMOS 0.18um process

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