A Low-Power Mixed-Signal Current-Mode DC-DC Converter Using a One-Bit $\Delta\Sigma$ DAC

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***Abstract*— This work describes a novel dual-mode mixed-signal peak current-mode controller for high-frequency DC-DC converters. The simple controller provides peak-current protection, inherent low audio susceptibility, and is suitable for portable applications. The voltage feedback loop is implemented using a windowed ADC and a digital PI compensator based on lookup tables. The analog current command used in traditional current-mode controllers is generated by a 2nd order one-bit $\Delta\Sigma$ DAC. The dual-mode controller automatically adjusts the DAC sampling frequency based on the digital error signal magnitude. The novel mixed-signal control strategy is experimentally verified on an 5V-to-1.5V 1 MHz buck converter prototype that exhibits a settling time of under 50 μs.**

I. Introduction

Digital controllers have emerged as promising candidates for DC-DC converter ICs in portable applications. The advantages of digital control include inherent noise immunity, on-the-fly configuration, potential for advanced nonlinear control, compatibility with low voltage deep sub-micron processes, design re-use, low parts count and automated place-and-route. Despite these advantages, digital controllers have not been widely adopted in low power applications, mainly due to concerns over high power consumption and frequency bottlenecks. Low power, area efficient, high frequency voltage-mode controllers with digital pulse-width modulators (DPWM) have been demonstrated in recent years to address these issues [1]–[5]. Peak current program mode (CPM) is widely used in analog implementations to provide inherent current protection, simple/robust compensation and reduced audio susceptibility. Existing current-mode solutions [6] [7] rely on complex digital signal processing to achieve Superior transient response, at expense of high power consumption. The most attractive digital current mode solution to date [8] relies on a low-power, low resolution A/D to sample the low-side transistor current. In this approach, both the current and voltage feedback loops are implemented digitally to implement average current mode control. The current-loop compensator includes a low-pass filter to estimate the steady-state duty cycle. While this relatively complex approach may be promising in certain applications, it does not offer inherent peak current protection. Without current protection, the integrated power stage must typically be over-designed to sustain peak currents far beyond the rated current during transients and additional start-up circuits that limit inrush current are needed. The main goal of this paper is to demonstrate a simple high frequency peak current-mode controller suitable for low-power converters used in battery-powered products.

II. Mixed-Signal digital CPM Concept

A simplified digital peak current-mode controller whose operation is similar to analog CPM is shown in Figure 1. The output voltage is sampled and subtracted from the digital reference $V_{ref}[n]$, producing an error signal $e[n]$. A DAC converts the digital current command from the compensator, $i_c[n]$, into an analog voltage, $v_c(t)$ that is compared to the sensed high-side transistor current [7]. The comparator resets the RS latch when $v_s(t) = K_s R_s i_s(t)$ exceeds $v_c(t)$, as in conventional CPM control. The analog comparator simplifies the design by eliminating the need for a fast current ADC used in [8], resulting in an efficient hybrid analog/digital approach.

The high current spike that occurs during the high-side transistor turn-on can cause the comparator to prematurely reset the latch. A simple modification to the RS latch provides positive edge blanking during the noisy leading edge of the current sense amplifier output as shown in Figure 2. A blanking clock, $\text{clk}_{\text{blank}}$ is used to disable the latch reset during t_{blank}. An additional modification is used to limit the duty cycle to 50 % since slope compensation is not employed in this work. The converter efficiency could be improved by using lossless current sensing schemes such as senseFET [9].

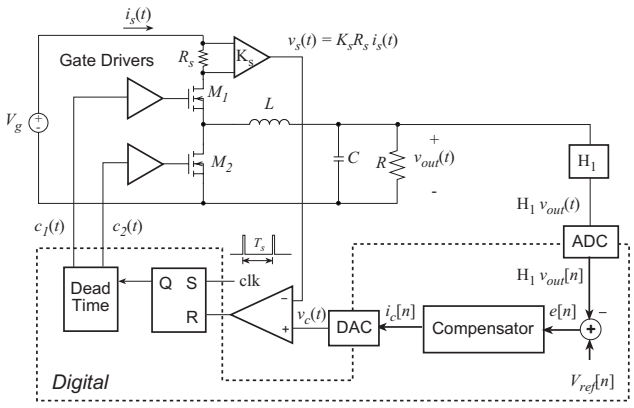

Fig. 1. Simplified architecture of the digital CPM converter. The proposed control scheme is also compatible with lossless current sensing techniques such as senseFET for improved efficiency.

This work was supported by NSERC and U of T Open Fellowship.

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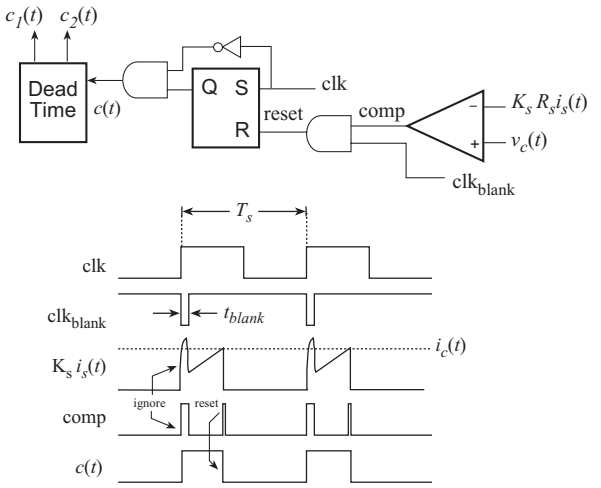

Fig. 2. Additional circuitry used to achieve 50% duty cycle limit and positive edge blanking.

III. Peak Current Programming using a 2nd order One-Bit ΔΣ DAC

In voltage-mode controllers, the digital pulse-width modulator (DPWM) must have sufficient resolution to avoid limit cycles [10]. Similar arguments apply to the resolution of the DAC that generates the current command, $v_c(t)$. The standard topology of a one-bit ΔΣ DAC is shown in Figure 3(a). The digital representation of the current command, $i_c[n]$ is fed into a noise-shaping modulator whose output is a bit-stream. The analog signal is extracted from the bit stream using a low-pass filter (LPF) having a cutoff frequency of f_c. A one-bit DAC is used to avoid the linearity degradation due to mismatches present in multi-bit ΔΣ DACs.

A. Effective Resolution of ΔΣ DAC

The 2nd order ΔΣ modulator and first order RC low-pass filter are shown in Figure 3(b). The delay elements are implemented as registers clocked by clk_{DAC} which has a frequency of f_{DAC}. The modulator can be implemented using only two registers and two adders. The gain of two is achieved using a simple bit-shift operation. The one-bit ΔΣ DAC offers high-resolution, low power (no quiescent current) and potential for compact on-chip implementation. The modulator noise-to-output transfer function is given by (1):

$$H(z) = (1 - z^{-1})^2 \tag{1}$$

The in-band noise present at the output of the modulator is analyzed in [11] and given by (2):

$$n_0 = e_{rms} \frac{\pi^N}{\sqrt{2N+1}} OSR^{N+1/2} \tag{2}$$

where N is the modulator order and e_{rms} is the rms quantization noise. For a second order modulator, it can be shown from (2) that the noise falls by 9 dB and hence the effective resolution increases by 1.5 bits for every doubling of the OSR [11]. In the context of the CPM controller, the OSR is defined as the modulator clock frequency divided by the update rate of $i_c[n]$. A high OSR is achieved during steady state, when the rate of change of the compensator output $i_c[n]$ is small compared to modulator clock frequency, allowing $v_c(t)$ and $v_{out}(t)$ to settle with very high accuracy. This oversampling concept has also been demonstrated in a voltage mode controller [12], where the traditional high-resolution delay-line based DPWM [13] is replaced by a combination of a low-resolution DPWM and a multi-bit ΔΣ modulator.

B. ΔΣ DAC Reconstruction Filter

The order of reconstruction filter in ΔΣ DACs is usually chosen to be at least one greater than the modulator order [14]. Using a 2nd or 3rd order butterworth LPF greatly reduces the quantization noise present at the DAC output for a given f_c, as shown in Figure 4. Despite the increased voltage ripple, a first-order RC filter is chosen for this work due to its simple passive implementation and power efficiency. This is considered a reasonable choice since the 2nd order output LC filter provides further low-pass filtering between $v_c(t)$ and $v_{out}(t)$. The LPF cutoff frequency must be kept sufficiently low such that the resulting voltage ripple on C_c does not cause $v_{out}(t)$ to fluctuate beyond the ADC zero error bin. On the other hand, it is desirable to keep f_c and f_{DAC} as high as possible in order to achieve a maximum voltage loop bandwidth and fast transient response. The simulated step response of the DAC is shown in Figure 5 for different values of f_c. The trade-off between voltage ripple due to quantization noise and transient response is clearly evident. In certain applications such as VRMs, where the power consumption of the DAC is negligible compared to the load power, the simplest solution is to use the highest possible frequency for f_{DAC}. This allows f_c to be placed high enough to have no effect on the control loop and achieve the fastest transient response. This illustrates the classical bandwidth/power consumption trade-off that is also present in analog controllers. For example, the bandwidth of a traditional analog voltage error amplifier is proportional to $g_m \propto \sqrt{I_D}$ and $g_m \propto I_C$ in CMOS and bipolar technologies respectively. In this design, the DAC dynamic power consumption is proportional to f_{DAC}. The limitation of this trade-off is overcome by using a dual-mode controller as described in Section IV.

IV. Dual-mode Controller for Improved Power-Bandwidth Trade-off

This section describes the novel CPM controller that provides inherent current limit and tight output voltage regulation without current limit cycling [15] [16]. In addition, complex digital signal processing is not required, making the controller suitable for low power applications. The block diagram of the CPM controller is shown in Figure 6. In the dual-mode controller concept, a different controller architecture is used in transient and steady-state operation [12]. The attenuated output voltage, $H_1 v_{out}(t)$, is sampled by a windowed ADC [15] and the result, $H_1 v_{out}[n]$, is subtracted from the digital reference, $V_{ref}[n]$. The windowed ADC produces only nine possible values of the error signal, $e[n]$ from -4 to +4, which greatly reduces the hardware requirements.

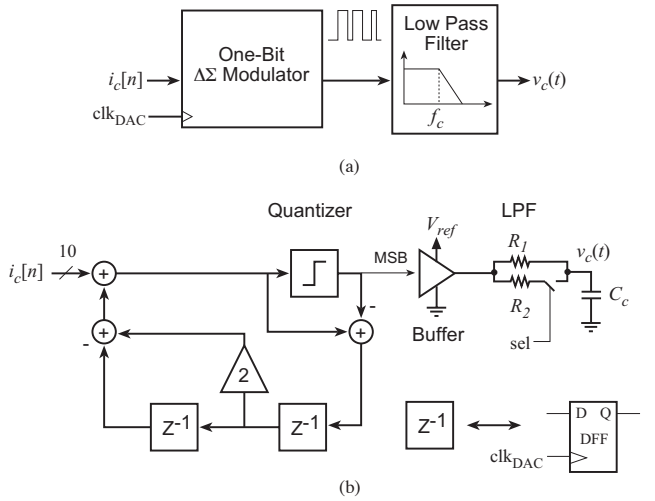

Fig. 3. (a) One-bit $\Delta\Sigma$ DAC structure and (b) 2nd order digital modulator with first order adaptive low-pass filter.

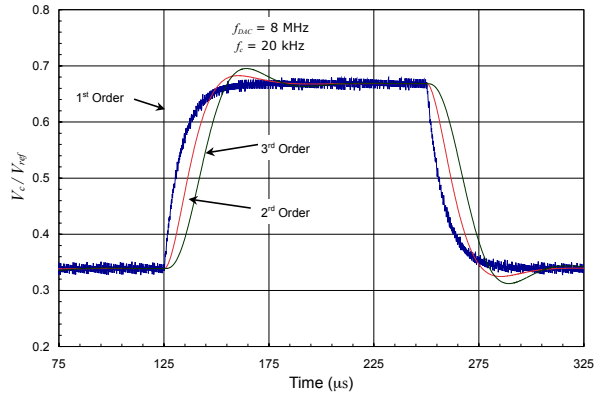

Fig. 4. Simulated step response showing the normalized $\Delta\Sigma$ DAC output voltage with 1st (RC), 2nd and 3rd order butterworth low pass filters.

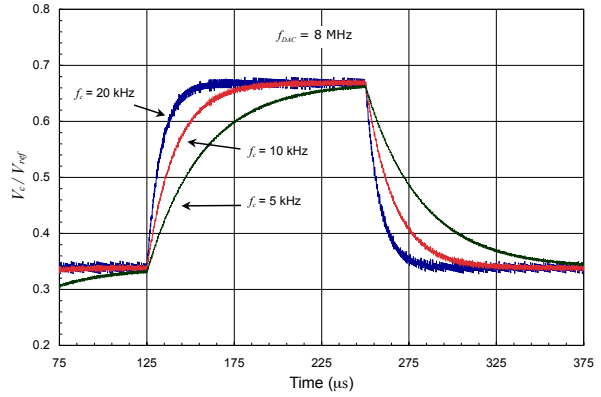

Fig. 5. Simulated step response showing the normalized $\Delta\Sigma$ DAC output voltage for three LPF corner frequencies to illustrate the trade-off between voltage ripple and transient response.

A. Controller Structure

The controller dynamics are adjusted by the mode selector based on the magnitude of $e[n]$, as given in Table I. In

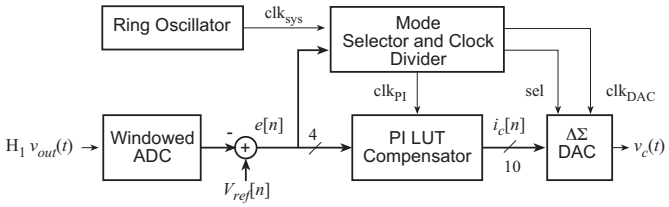

Fig. 6. Dual-mode controller architecture.

steady-state, when the error is small, the $\Delta\Sigma$ OSR and filter components are selected to provide tight regulation and low power consumption. During a load transient, when $|e[n] > 2$ the compensator is clocked every switching cycle, and the $\Delta\Sigma$ OSR is set based on the worst-case assumption that the compensator changes the duty cycle every period of clk_{PI}. The $\Delta\Sigma$ modulator clock frequency is doubled to allow a higher LPF cutoff frequency and more aggressive LUT compensator gains. This results in fast settling without compromising the steady-state power consumption. The sel pin is used to switch between $f_{c1} = 1/(2\pi R_1 C_c)$ in steady-state mode and $f_{c2} > f_{c1} = 1/(2\pi(R_1||R_2)C_c)$ in transient mode.

TABLE I
CONTROLLER CLOCK FREQUENCIES DURING DUAL MODE OPERATION

Mode	$\|e[n]\|$	clk_{PI}	clk_{DAC}	f_c	OSR
0 (steady-state)	≤ 2	$f_s/4$	$8f_s$	$1/(2\pi R_1 C_c)$	>32
1 (transient)	> 2	f_s	$16f_s$	$1/(2\pi R_1 \|\| R_2 C_c)$	>16

B. Compensator Design

Unlike voltage-mode control, the buck converter control-to-output transfer function in CPM is dominated by a single, load-dependent, low frequency pole at $f_p = 1/(2\pi RC)$ [17], which makes PI compensation suitable. The voltage loop compensator is based on lookup tables and implements the PI difference equation given by (3):

$$i_c[n] = i_c[n-1] + Ae[n] - Be[n-1] \tag{3}$$

The controller architecture is shown in Figure 7. The LPF pole at f_c reduces the achievable controller bandwidth unless it is moved beyond f_p. For a given ripple on $v_c(t)$, the minimum f_c is proportional to the $\Delta\Sigma$ compensator clock frequency, f_{DAC}. In steady-state, a slow compensator is used and the dynamics are not influenced by the filter pole, while during transients this pole is pushed at higher frequencies through the change of filter constant. The trade-off between the DAC power consumption and bandwidth is effectively managed by the dual-mode controller. Programmable current limiting is achieved simply by adding a digital saturation block at the compensator output. The peak current limit i_{peak} for a digital saturation value of i_{sat} is given by (4):

$$i_{peak} = \frac{i_{sat}}{2^M} \cdot \frac{V_{ref}}{K_s R_s} \tag{4}$$

where M is the DAC input bus width, V_{ref} is voltage swing on the modulator output and $K_s R_s$ are the current sensing

parameters. In addition, the steady-state current command can be used to determine whether the converter should switch to a more efficient mode, such as PFM. A digital comparator can used to compare $i_c[n]$ with pre-programmed thresholds. This is a distinct advantage over voltage-mode controllers, where the load current is not known. In one digital controller [18] an estimator technique is used to extract the load current information from the input/output voltage and the duty cycle.

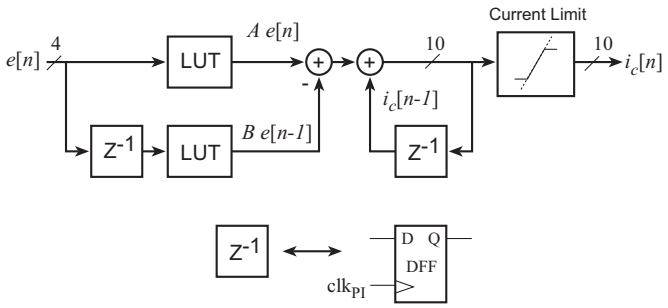

Fig. 7. PI compensator with programmable saturation for current limiting.

V. Experimental System and Results

An experimental 5V to 1.5V DC-DC converter with L = 2.5 μH, C = 36 μF, f_s = 1 MHz was constructed. The digital controller is implemented in a mainstream 256 macrocell 0.18μm CMOS CPLD. The response of the DAC fed by a 10-bit counter is shown in Figure 8. As expected, the $\Delta\Sigma$ modulator has good linearity over the range of interest but the linearity is degraded for large inputs. The steady-state waveforms for $v_c(t)$, $K_s i_s(t)$ and the reset pulse are shown in Figure 9. The transient response for a 0.46 A to 1.1 A load transient is shown in Figure 10. The controller switches to transient mode (mode =1) as soon as $|e[n]| > 2$. The DAC filter resistance is automatically reduced and the modulator clock frequency is doubled to allow a rapid settling of $v_c(t)$ and hence $v_{out}(t)$. A fast settling time of 50μs is achieved. The controller rapidly increases $v_c(t)$ in transient mode before switching back to steady-state mode for $e[n] \leq 2$. Effective cycle-by-cycle current limiting is always maintained. The switching frequency is only limited by PCB's current sense amplifier bandwidth and the high switching losses. The full prototype specifications are listed in Table II.

TABLE II
Prototype Specifications

Specification	Value	Units
Input Voltage	5	V
Output Voltage	1.5	V
Nominal Load	0.5	A
Output Capacitor	36	μF
Filter Inductance	2.5	μH
Switching Frequency	1	MHz
$\Delta\Sigma$ Modulator	2nd	order
Steady State / Transient DAC Frequency	8/16	MHz
ADC Error Bin	31.3	mV
Settling Time	< 50	μs

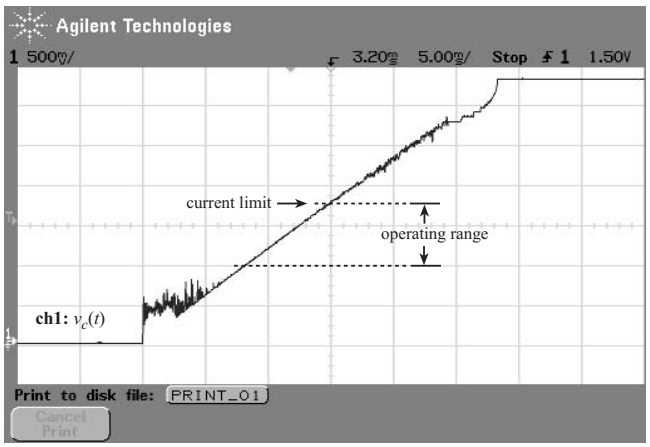

Fig. 8. DAC output voltage when the modulator is fed by a low-frequency 10-bit counter.

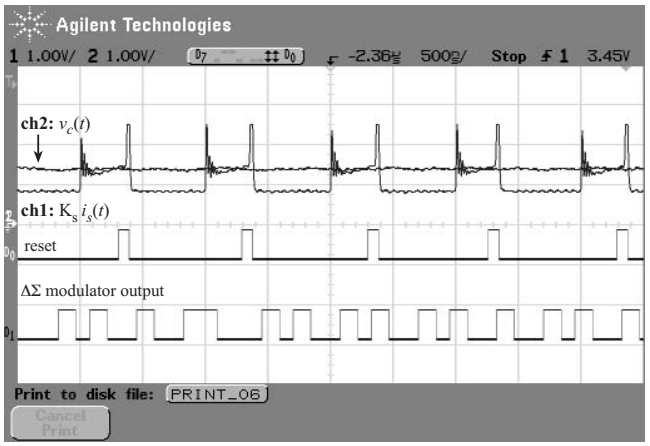

Fig. 9. The amplified current ramp is compared to the DAC output. The leading edge spike is blanked, resulting in a correct reset signal.

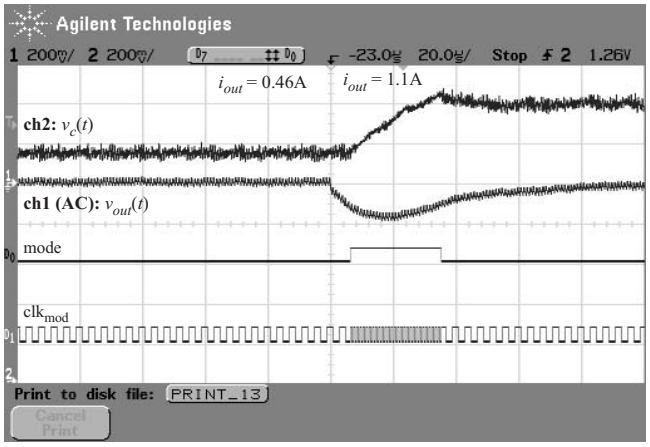

Fig. 10. Transient response for a 0.46A to 1.1A load current step (at t=0). The controller switches into transient mode to achieve a fast settling in under 50μs.

VI. Conclusion

A novel dual-mode mixed-signal peak-current controller for high frequency DC-DC switching converters was presented. The analog current command present in traditional CPM controllers is generated by a 2^{nd} order one-bit $\Delta\Sigma$ DAC fed by a digital LUT-based PI compensator. The novel digital control strategy is successfully verified on an experimental 5V to 1V DC-DC converter prototype. The prototype has a high switching frequency of 1 MHz, which is competitive with analog CPM solutions.All the advantages of analog implementation such as peak current protection, low audio susceptibility and high frequency operation are maintained. In addition, the potential advantages of digital control including noise immunity, on-the-fly configuration, design re-use, low parts count and automated place-and-route are gained.

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