Limit-Cycle Based Auto-Tuning System for Digitally Controlled Low-Power SMPS

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***Abstract*- This paper presents a new method and system for the parameter extraction and dynamic auto-tuning of low power digitally controlled dc-dc switch-mode power supplies (SMPS). During a short-lasting test phase, SMPS parameters, such as output capacitance and load, are estimated by examining the amplitude and frequency of intentionally introduced limit cycle oscillations. Then, accordingly, the digital compensator of SMPS is automatically tuned to improve the output regulation and dynamic performance. The effectiveness of the method is demonstrated on an experimental 200 kHz, 12V-to-5 V, 10 W, digitally controlled buck converter.**

I. INTRODUCTION

Digital control offers features that can improve characteristics of low-power high frequency switch mode power supplies (SMPS). Flexibility, realization with a small number of passive components [1-5], low sensitivity on external influences [6-7] and fast design, which can easily be modified, and transferred from one implementation technology to another are just some of them. The digital control also allows simple implementation of advanced control and power management techniques that are not easily realizable in analog implementations. However, many advanced control techniques, widely employed in large-scale power systems, have not been used in low-power SMPS for battery-powered handheld devices and consumer electronics. This is mostly due to high computational demands those methods require for implementation. The methods can usually only be realized with digital hardware which complexity and power consumption exceeds that of all other system parts of low-power SMPS, resulting in poor overall system efficiency.

System identification and auto-tuning, i.e. on-line calibration, are among the most attractive control methods extensively used in large scale systems [8] and rarely utilized in low-power SMPS. In these methods system parameters are extracted from information available in feedback loop and, accordingly, the control law is adjusted to improve the system robustness, dynamic response, and regulation.

Recent publications [9, 10] show simplified methods for on-line calibration based on the use of pseudo random binary sequence (PRBS). In these methods, during the system identification, the SMPS operates in open loop and the identification is performed with a dedicated digital hardware. This hardware is still fairly complex for the use in very-low power applications.

In this paper we present a new closed-loop auto-tuning method and system that can be realized with a very simple hardware and used in low-power SMPS. The system, shown in Fig.1, utilizes information from intentionally introduced limit cycle oscillations for sensorless identification of output capacitance, load, and inductance values (i.e. system identification). Then, based on collected information, it performs dynamic compensator adjustment.

The method and system allow better utilization of the flexibility of digital control and introduction of new features in low-power SMPS. They can be used in the upcoming sophisticated power management systems for handheld devices [11], computers, and communication systems. Some immediate applications include decentralized "health monitoring" of SMPS [12], and minimization of stability problems in distributed power architectures (DPA) [9-13]. The auto-tuning could provide easier paralleling of multiple SMPS.

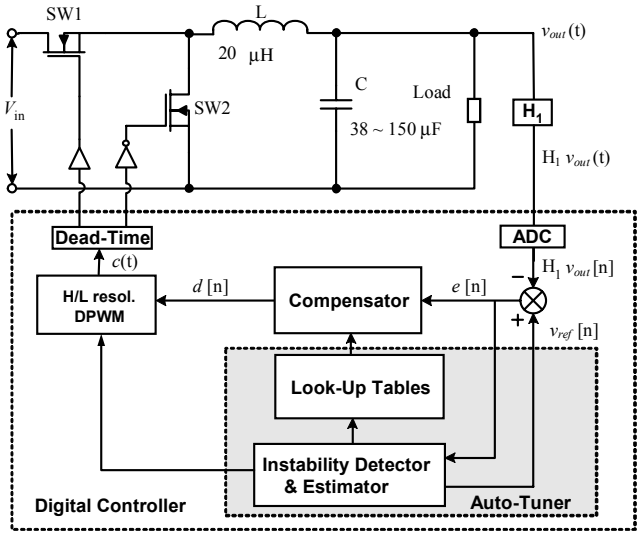

Fig. 1. Block diagram of an SMPS with limit-cycle based auto-tuning digital controller.

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Also, as it is shown later, the new method and system can improve dynamic response of SMPS and eliminate the need for digital compensator redesign each time the system configuration changes.

The paper is organized as follows: Section II briefly addresses the fundamentals of limit-cycle oscillations (LCO) and explains how the LCO can be used for the SMPS parameters extraction. The architecture and operation of the new auto-tuning system are described in Section III. Section IV shows experimental results obtained with a prototype that utilizes this auto-tuning method. A summary of the main results is given in section V.

II. Parameter Estimation from Limit-Cycle Oscillations

A specific property of digitally controlled SMPS, as the one of Fig.1, is that small self oscillations around the steady state could occur. The oscillations are caused by non-linear quantization effects in analog-to-digital converter (ADC) and digital pulse-width modulator (DPWM) [14, 15]. The DPWM produces a discrete set of duty ratio values, meaning that only a quantized set of steady-state voltages can be obtained. When the resolution of the DPWM is low, compared to that of the ADC, for some operating conditions quantized outputs cannot result in zero error $e[n]$ value. As a result, the feedback controller containing an integrator changes its output between two or more discrete duty ratio values, and oscillations known as limit cycling (LCO) occur. The problem of LCO in digitally controlled dc-dc SMPS and their elimination methods are extensively analyzed in [14, 15].

Although undesirable in the steady state, the limit cycle waveforms contain useful information about the system parameters. Figure 2 shows a typical LCO waveform. It is a non-symmetric signal characterized with maximum and minimum amplitudes (A_{max}, A_{min}), and period, T_{LC}. In a digitally controlled SMPS these three distinctive features depend on the values of power stage inductance, output capacitance and the load. They also depend on the input voltage of the power stage and digital compensator parameters. Since in digital controllers the parameters of the compensator are usually known, LCO features A_{max}, A_{min} and T_{LC} (or frequency f_{LC}) can be used for the estimation of any other three system parameters.

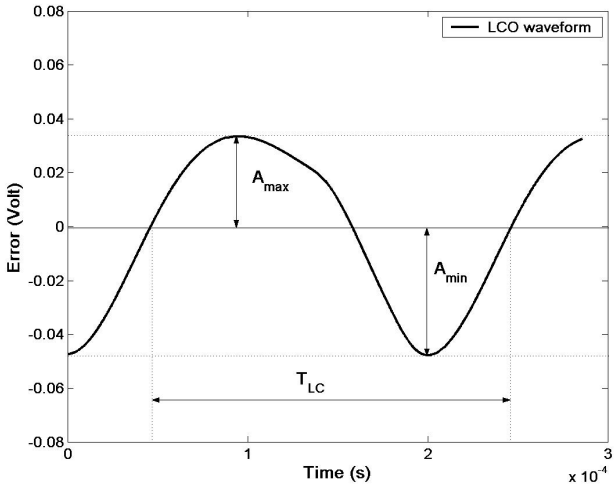


Fig. 2. A typical limit cycle oscillation (LCO) waveform.

It is especially helpful to obtain system parameters for compensator self-adjustment purpose when the system configuration often changes. The controller can then be adjusted accordingly using the knowledge of updated system parameters.

Although the system described in the following section of this paper is able to extract all three LCO parameters, for simplicity, only two of them are used. Peak-to-peak amplitude and frequency of LCO are observed to obtain values of the output capacitance C and the output load R.

The exact relation between system parameters and LCO features can be found using advanced control theory tools,

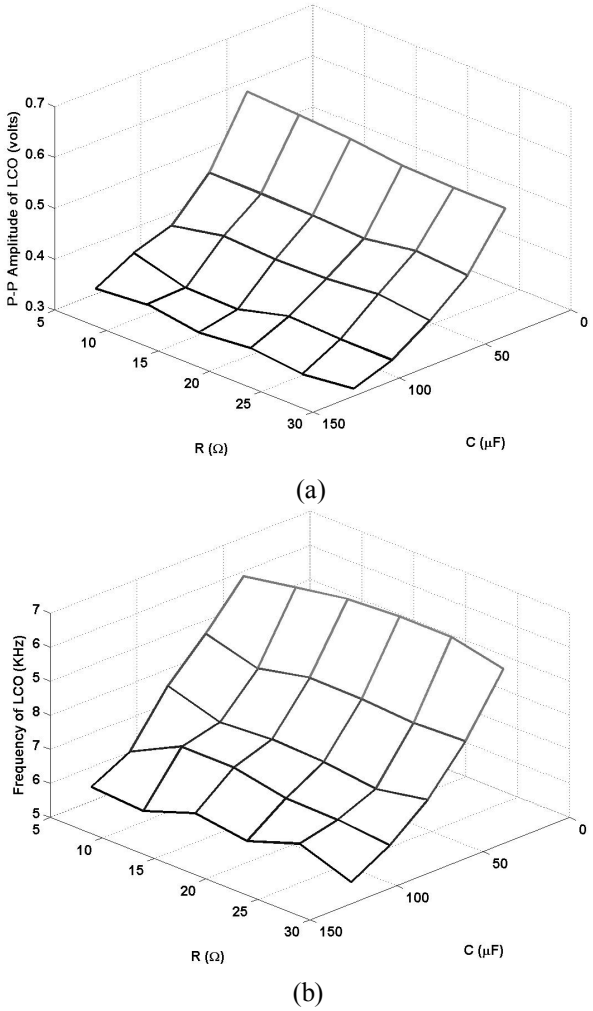


Fig. 3. Variations of LCO feature under different output capacitance and load conditions. (a) peak-peak amplitude, (b) frequency

developed for large-scale relay systems [16, 17]. However, due to high computation complexity these methods are not suitable for on-line implementation in low-power SMPS. A simpler approach, adopted here, is the use of prior system analysis as well as simulations and experimental verifications to establish the relations between the LCO features and SMPS parameters. In section V we will show that the prior assessment in a small number of operating points over a wide operating range provides sufficient information about system behavior and allows simple system realization.

Diagrams of Fig. 3 demonstrate results of only 30 experimental measurements. They show how for the system of Fig.1 the peak-to-peak amplitude and frequency of LCO vary with wide changes of the output capacitance and load. It can be seen that by examining the peak-to-peak amplitude and frequency of oscillations both the capacitance and load can be uniquely determined.

In the following section we describe an auto-tuning architecture that utilizes predetermined relations between the LCO features and SMPS parameters.

III. Auto-Tuning System Architecture and Operation

The auto-tuning system and adjustable controller shown in Fig. 4 operate as follows. The block named *instability detector* monitors the output voltage error $e[n]$ and senses disturbances in the SMPS. When a disturbance that can lead to instability occurs, to regain stability, the estimator decreases the compensator gain, and when the regulation is again achieved, the system switches into parameter extraction mode.

During the parameter extraction the resolution of the digital pulse-width modulator (DPWM) is intentionally decreased to initiate small limit-cycle oscillations. Simultaneously the values of limit cycle amplitudes A_{max}, A_{min} and frequency f_{LC} (see Fig.2) are identified.

In the following phase, based on the extracted A_{max}, A_{min}, i.e. peak-to-peak amplitude, and f_{LC}, the parameters of PID compensator are updated from the values pre-stored look-up tables (LUT) to accommodate changed system dynamics. Then, the high DPWM resolution is restored (limit cycle oscillations are eliminated) and auto-tuning process is completed.

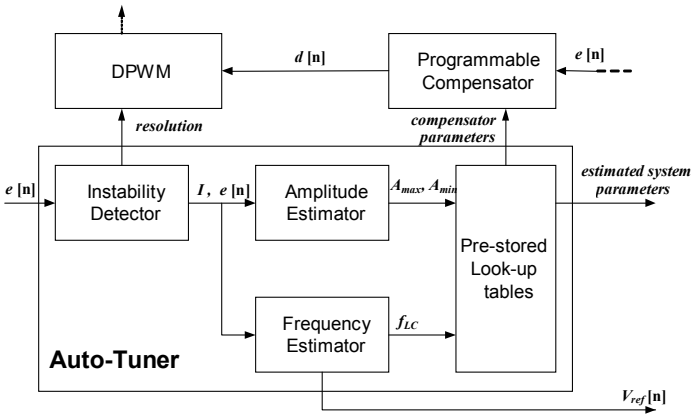


Fig. 4. Detailed Auto-Tuner block diagram

In the following subsections we give more detailed description of all functional blocks.

A. Instability Detector

The instability detector constantly monitors the output voltage error $e[n]$ and senses operating conditions that may lead to reduced system stability or instability. When such conditions are sensed the detector creates *start identification* signal, I, that initiates parameter extraction mode. In this case to realize detector we used implementation shown in [18]. Many other realizations, documented in [19, 20], are also possible.

B. Detection of A_{max} and A_{min}

The extraction of the maximum and minimum LCO magnitudes is performed through a simple detection of the sign change of the derivative of feedback error signal $e[n]$:

$$\Delta A[n] = e[n] - e[n-1] \tag{1}$$

The error $e[n-1]$ immediately preceding the change of the sign from positive to negative is considered to be maximum amplitude of LCO, A_{max}, while the error $e[n-1]$ preceding the opposite sign change is equal to A_{min}. Calculation of the derivative is performed at the rate of switching frequency. Since the power stage behaves as a low-pass filter, its switching frequency is significantly higher than the frequency of LCO and accurate calculation of the derivative is possible. Also, due to the low-pass nature of the power stage, in a single oscillation period, there will be only one local maximum and one minimum of the LCO. Peak-to-peak amplitude in one LCO period is calculated as the difference between two successive A_{max} and A_{min} values.

C. Frequency Extractor

Figure 5 shows a simplified diagram of the frequency extractor which is a part of the auto-tuner block of Fig. 4. The

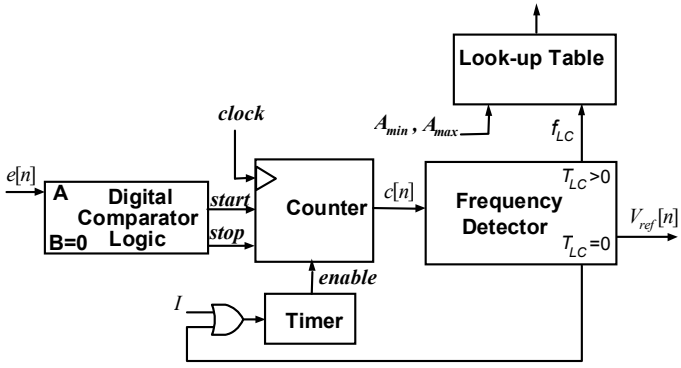


Fig. 5. Frequency extractor block diagram

frequency extractor measures the frequency of limit cycle oscillations upon the parameter extraction process is triggered with signal *I*. The signal starts a timer and a counter, which counts the number of switching periods between three zero-crossings of error signal $e[n]$, i.e. measures the period of limit-cycle oscillations.

The frequency extractor also ensures the existence of LCO during the identification phase. For some operating points, the quantized output voltage results in zero error value and the oscillations do not exist even though the resolution of the DPWM is low. In the frequency detector block of Fig. 5 this situation is detected as $T_{LC} = 0$. In that case LCO are initiated through a small change of voltage reference. Furthermore, in this implementation, the same block is used to make A_{max} and A_{min} approximately the same and create a symmetrical signal. This allows use of simpler tools for the analysis of the correlations between the limit cycle oscillations and system parameters. For example *describing functions* [15] which assume symmetry of the LCO signal can be used for the pre-calculation of the compensator parameters. As described in [16], the symmetric LCO gives a simpler solution to the mapping between the features and system parameters.

It should be noted that the frequency of LCO can also be estimated from duty ratio control value $d[n]$, which is always available in a digital control loop. Instead of measuring the output voltage error $e[n]$ variations in least significant bits (LSBs) of $d[n]$ can be observed. In that case a minor modification of the block shown in Fig. 5 would be required.

Once the frequency and peak-to-peak amplitude are determined these values can be mapped to the estimated R, C values and the system identification can be completed.

D. Pre-stored Look-up Tables

The measured peak-to-peak amplitude of LCO and their frequency are used as the inputs of look-up shown in Fig. 4. The outputs of the table are pre-stored coefficients for a multiplier-based PID compensator. The coefficients are pre-calculated based on corresponding R and C values using digital redesign as described in [21].

IV. Experimental System and Results

Based on diagrams shown in Fig.1 and 4 an experimental prototype was built. The power stage of the system is a 12V-to-5V, 10W buck converter operating at switching frequency of 200 kHz. All functional blocks of the digital controller but DPWM are realized using an Analog Devices, ADMC-401 DSP Board. An Altera 10K FPGA system is used for the implementation of a high-resolution high-frequency programmable DPWM, which is not available on the DSP board [2]. In steady-state the resolution of the DPWM is set to 8 bits, while, during the identification phase it is decreased to

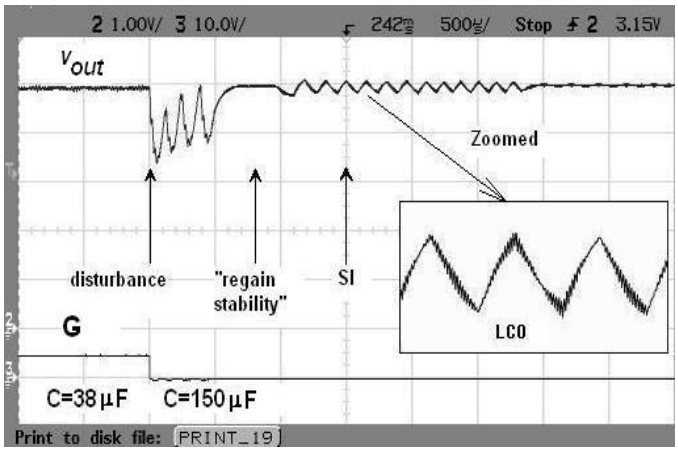


Fig. 6. Experimental results for the output capacitance change from 38 µF to 150µF. Ch2 (1 V/div): output voltage $v_{out}(t)$; Ch3: control signal for the capacitance change.

4 bits. Pre-stored PID coefficients are placed in three 30 word 10-bit look-up tables. It can be seen that the whole system can be implemented with a simpler hardware and a complete FPGA or on-chip implementation is also possible.

Figures 6 and 7 show experimental results obtained with our prototype.

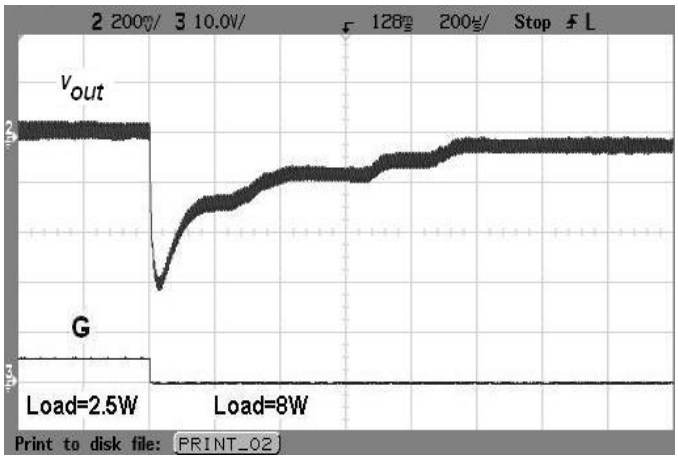
A. Experimental Results on System Behavior

Figure 6 demonstrates auto-tuning system behavior when the output capacitance changes from a value of 38 µF to 150 µF (indicated as disturbance in Fig.5)., This change leads to instability, which is recognized by an instability detector. In the next "regain stability" phase the gain of the PID regulator is decreased and the system stability is regained. Then, during the system identification (SI) phase the controller introduces limit-cycle oscillations by decreasing the DPWM resolution from 8 to 4 bits, and the parameter estimation is performed according to the procedure described in Section III. The last part of the waveform shows operation of the controller with updated PID regulator parameters and increased 8-bit DPWM resolution.

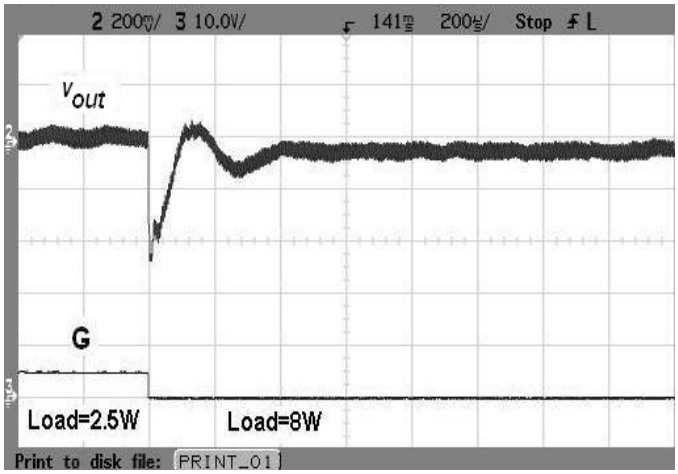
B. Experimental Results on Dynamic Response

Figure 7 shows comparison of two load transient responses. First is the response of slow PID regulator used during "regain stability" phase. This compensator provides stability for all operating conditions and would be used in a conventional system without auto-tuning. The second response is obtained with controller that employs limit-cycle based auto-tuning. It can be seen that the auto-tuning results in stable and significantly faster response.

The diagrams of Figs. 6 and 7 also demonstrate that the system is able to detect instability, "recognize" new set of parameters, and accordingly perform auto-tuning that results in improved dynamic response.



(a)



(b)

Fig. 7. Experimental results of load transient change 2.5W-to-8W. Ch2 (200 mV/div-ac): output v_{out} (t); Ch3: control signal for the load transient; (a) transient response with a slow "regain stability" PID controller; (b) transient response with auto-tuning system.

V. CONCLUSIONS

This paper describes a new digital system that allows introduction of auto-tuning in low-power dc-dc switching converters. We demonstrate how the limit-cycle oscillations of digitally-controlled converters can be utilized for practical system identification and auto-tuning. A simple prototype that employs the new method is shown as well as experimental results that verify effective system operation.

REFERENCES

[1] A.V. Petrchev, J. Xiao, and S.R. Sanders," Architecture and IC Implementation of a Digital VRM Controller," IEEE Transactions on Power Electronics, Special Issue on Digital Control, vol. 18, pp. 356 364, January 2003.

[2] B. Patella, A. Prodić, A. Zirger, D. Maksimović, "High-Frequency digital controller PWM controller IC for DC-DC converters," IEEE Transactions on Power Electronics, Special Issue on Digital Control, vol. 18, pp. 438 446, January 2003.

[3] E. O'Malley, K. Rinne, " A Programmable Digital Pulse Width Modulator Providing Versatile Pulse Patterns and Supporting Switching Frequencies Beyond 15 MHz," in Proc. IEEE APEC'04 Conf., 2004, pp. 53 59.

[4] A.P. Dancy, R. Amirtharajah, and A.P. Chandrakasan, "High-Efficiency Multiple-Output DC-DC Conversion For Low-Voltage Systems," IEEE Transactions on VLSI Systems, vol. 8, pp. 252 263, June 2000.

[5] J. Xiao, A. Peterchev, J. Zhang, S.R. Sanders, "An Ultra Low-Power Digitally-Controlled Buck Converter IC for Cellular Phone Applications," in Proc. IEEE APEC'04 Conf., 2004, pp. 383 391.

[6] A.V. Petrchev, S.R. Sanders, "Digital Loss-Minimizing Multimode Synchronous Buck Converter" in Proc. IEEE PESC'04 Conf., 2004, pp.20-25.

[7] A. Prodić, R.W. Erickson and D. Maksimović, "Digital Controller Chip Set For Isolated DC-DC Power Supplies," in Proc. IEEE APEC Conf., 2003, February 2003, pp. 866 872.

[8] K. Hirayama, Y. Tone, K. Takagi, H. Murakami, M. Shibata, H. Nagamura, and Y. Takagi, "Digital AVR application to power plants," IEEE Trans., Energy Conversion, Vol. 8, pp.602-609, Dec. 1993.

[9] M.F. Schlecht, "Distributed power architecture system stability requires compensation of DC-DC converter inputs," PCIM Mag., Vol.26. No.2, pp. 52-56, February 2000.

[10] B. Miao, R. Zane, and D. Maksimović, "Practical on-line identification of power converter dynamic response," in Proc., IEEE APEC 2005, pp. 57-62.

[11] D. Monticelli, "System approaches to power management" in Proc. IEEE APEC Conf., 2002, February 2002, pp. 3 7.

[12] R. White, "Emerging on-board power architectures," in Proc., IEEE APEC 2003, pp. 799-804, Feb. 2003.

[13] D. L. Logue and P.T. Krein, "Preventing instability in DC distribution systems by using power buffering," in Proc., IEEE PESC 2001, pp.33-37.

[14] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," IEEE Trans., Power Electron., Vol.18, pp. 301 - 308, Jan. 2003.

[15] Hao Peng, D. Maksimovic, A. Prodic and E. Alarcon, "Modeling of quantization effects in digitally controlled DC-DC converters," in Proc., IEEE PESC 2004, pp. 4312 – 4318.

[16] I. Kaya and D. P. Atherton, "Exact parameter estimation from. relay autotuning under static load disturbances," In Proc., IEEE American Control Conference 2001, pp.3274 – 3279.

[17] S. Majhi and D. P. Atherton, "Autotuning and controller design for processes with small time delays," IEE Proc., Control Theory and Applications, Vol. 146, pp. 415 – 425, Sept. 1999.

[18] B. Miao, R. Zane, and D. Maksimović, "Detection of instability and adaptive compensation of digitally controlled switched-mode power supplies," in Proc., IEEE APEC 2005, pp. 63-69.

[19] P. Ranjan and E. H. Abed, "Instability monitoring in boost converters by resonant perturbation and control," In Proc., IEEE American Control Conference, 2001, pp. 1727-1732.

[20] Taihyun Kim and E. H. Abed, "Closed-loop monitoring systems for detecting incipient instability," In Proc., IEEE Decision and Control Conference, 1998, pp. 3033-3039.

[21] A. Prodic and D. Maksimovic, "Design of a digital PID regulator based on look-up tables for control of high-frequency DC-DC converters," In Proc., IEEE COMPEL, 2002, pp. 18-22.