Self-Programmable PID Compensator for Digitally Controlled SMPS

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***Abstract*-This paper shows an auto-tuning system for digitally controlled switch-mode power supplies (SMPS) that automatically adjusts parameters of PID compensator based on pre-specified bandwidth requirements. The PID compensator parameters are determined from intentionally introduced limit cycle oscillations (LCOs) through two consecutive auto-tuning procedures. First, the placement of poles and zeros is defined from LCOs at the corner frequency of the power stage. Then, the gain of the PID compensator is found from the oscillations occurring at the desired crossover frequency of the system. The proposed auto-tuning procedure is verified through Matlab/Simulink simulations that show fast load transient response and short settling time.**

I. INTRODUCTION

In a recent publication [1] an LCO-based auto-tuning system has been demonstrated as an effective solution for the estimation of parameters of digitally controlled SMPS and consecutive compensator adjustments. It has been shown that limit-cycle oscillations contain useful information and that by examining their frequency and amplitude parameters of power stage (PS) such as the values of inductor, output capacitor and load, can be determined and consequently used for PID compensator adjustments. The method is based on a relatively complex pre-calculation of the relations between the LCO features and power stage parameter values, whose results are later stored in look-up tables to simplify implementation.

In this paper we show an extension of this concept, an auto-tuning method that does not require parameter estimation and therefore can be realized in a simpler manner. Controller coefficients and its gain are adjusted directly from the measured LCOs eliminating the need for pre-calculation of the corresponding control parameters. This self-programming digital PID compensator minimizes compensator design efforts and can be used with a various power stages having wide range of inductor, capacitor and load values. Practically, a system designer only need to set the cross-over frequency, e. t. bandwidth, of the loop gain and the remaining part of the compensator design is automatically performed. A similar tuning concept has been reported in [4] where relay feedback controllers are applied. However, the proposed LCO based tuning method takes advantages of inherent nonlinear characteristics and more information of the system. Moreover it is based on small oscillations (i.e. limit-cycle oscillations) which may already appear in dc-dc converters and whose amplitude is inherently limited to a few Least-Significant-Bits (LSBs) of the Analog to Digital (ADC) converter.

A different auto-tuning approach, based on non-parametric methods for the on-line assessment of system dynamics in dc-dc converter, has been proposed in [2,3]; the methods reported in [2,3] are very interesting for converter transfer functions identifications, but they requires open-loop operation during the identification process and slightly more complex signal processing.

A block diagram of the self-programmable system is shown in Fig.1. It comprises of a conventional digital pulse width modulator controller (analog-to-digital converter (ADC), digital pulse-width modulator (DPWM), and programmable compensator) and an auto-tuner. The tuner has an instability detector / mode selector block [1], which can be triggered periodically or externally, upon instability in the system is detected, and a LCO initiator for introduction of limit cycle during tuning process. The limit cycle oscillations are intentionally introduced during monitoring and auto tuning process, through a reduction of the DPWM resolution [1].

As it will be described in later sections in more details, all

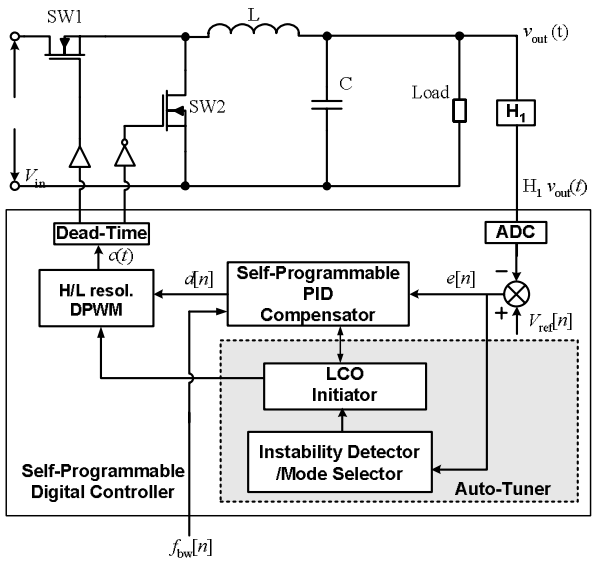

Fig. 1. Self-programmable SMPS system block diagram

of the blocks of the self-programmable controller can be

implemented with a very simple hardware allowing its use in low-power SMPS (power supplies for miniature portable devices, consumer electronics…). Traditionally, auto-tuning systems have not been utilized in low-power applications due to high complexity and cost of conventional solutions used in higher power systems.

The paper is organized as follows: the following section briefly addresses the relationship between LCO features and system transfer functions and it explains how LCOs are used for designing PID coefficients. The PID tuning and design procedure with bandwidth control is described in Section III. Section IV shows simulation results obtained with a Matlab/Simulink model that utilizes auto-tuning method.

II. Properties of Limit-Cycle Oscillations in Digitally Controlled SMPS

In a digitally controlled SMPS, whose model is shown in Fig.2, limit cycle oscillations can exist even when the system is conditionally stable and the output voltage is kept around desired reference V_{ref}. The LCOs are caused by nonlinear elements, ADC and DPWM, whose gains M_{DPWM} and M_{ADC} respectively, depend on input signal amplitudes.

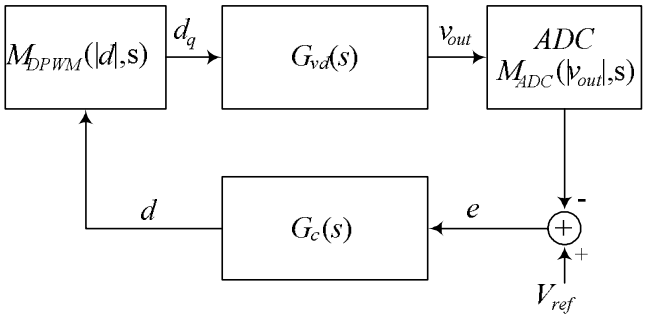

Fig. 2. Linear model of SMPS feedback loop

The LCOs occur at certain magnitudes of output voltage $|v_{out}|$ and control signal $|d|$, for which the system "loop gain"

$$T(s) = M_{dpwm}(|d|,s)G_{vd}(s)G_c(s)M_{ADC}(|v_{out}|,s) \quad (1)$$

has unit magnitude and phase of -180°, i.e. $T(s) = 1\angle$-180°. Given that LCO conditions strongly depend on $G_{vd}(s)$ and $G_c(s)$, the power stage control-to-output and compensator transfer functions respectively, by examining LCOs we can estimate some of their parameters. Even more, since in digitally controlled systems $G_c(s)$ is usually exactly known, estimation process can be simplified and, as will be shown in the following section, all main features of $G_{vd}(s)$ can be accurately determined. Consequently, an appropriate PID compensator can be automatically designed to satisfy predetermined bandwidth requirements.

III. Self-Programmable PID Compensator

Self-programmable PID compensator, whose simplified block diagram is shown in Fig.3, can operate in three different modes. When all three data switchers (*SW*1 to *SW*3) are in *regular* mode, it operates as a conventional controller. Digital

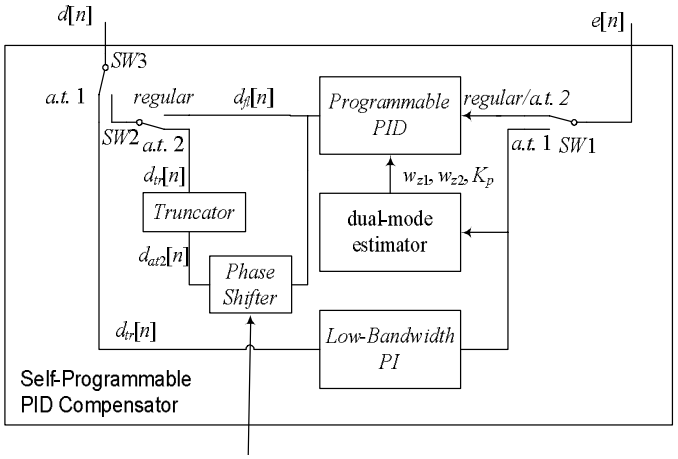

Fig. 3. Self-programmable PID compensator block diagram

equivalent of the analog output voltage $v_{out}[n]$ is compared to the reference $V_{ref}[n]$ and the resulting error signal is processed with PID compensator, whose coefficients are determined through auto-tuning process.

In addition, it has two auto-tuning modes, labeled as *a.t.*1 and *a.t.*2, defined with the corresponding positions of the data switchers.

In auto-tuning modes the resolution of the DPWM is intentionally reduced by sending truncated binary control signal $d_{tr}[n]$ to its input. As a result a strong nonlinearity causing LCO is introduced allowing dynamic adjustment of PID compensator parameters. In the first auto-tuning step PID compensator zeroes w_{z1} and w_{z2} are defined. Then, in the following step appropriate gain of the compensator, K_p, is determined to result in a desired bandwidth of the controller $f_{bw}[n]$ that can be set externally. In both steps the resolution of the ADC is kept sufficiently high, so that its nonlinear quantization effects are negligible compared to those of the DPWM.

The two-step auto-tuning process can be explained through the following example assuming that a buck-converter with control-to-output transfer function

$$G_{vd}(s) = \frac{V_g}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_o^2}} \cong \frac{V_{out}/D}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_o^2}} \quad (2)$$

is the power stage, where corner frequency ω_0 and Q factor are determined with the power stage components and its load [5]. The value D defines steady-state duty ratio value. In (2) and hereafter in the paper we will assume that the zero of the

ESR output capacitors is outside the control bandwidth, i.e. we consider the case of output capacitors with small ESRs.

During the first auto-tuning step *SW*1 and *SW*3 are set in position *a.t.*1 and the output voltage is regulated with a digital integrator, whose analog equivalent has the following form

$$G_{C1}(s) = K_I D\left(\frac{1}{s}\right) \tag{3}$$

The compensator's gain, K_I, is multiplied with D to eliminate the influence of the input voltage change effectively behaving as a feedforward element. The resulting loop gain in this mode is described with the following equation

$$T_{AT1}(s) = M_{dpwm}(|d|,s)G_{C1}(s)G_{vd}(s)M_{ADC} \tag{4}$$

and depicted in Fig.4. It can be seen that in this case phase shift of 180° always corresponds to the corner frequency of the power stage. As a result, the LCO can occur only at the corner frequency and their magnitude is proportional to Q factor, which strongly influences the gain of G_{vd}(s) at that frequency. Hence, by measuring amplitude and frequency of the limit cycle oscillations these two parameters can be directly determined. In the dual-mode estimator in Fig. 3

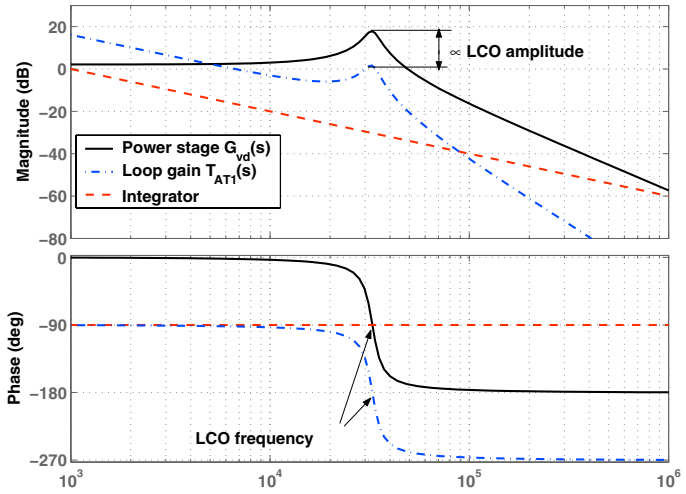

Fig. 4. Bode plots of systems during first step tuning

includes simple hardware for amplitude and frequency measurements [1] to determine the LCO parameters. Based on the measured results self-programmable PID compensator is adjusted in accordance with the following equation:

$$G_{C2}(s) = D \cdot K_{I2} \frac{s^2 + \frac{r}{Q}\omega_{LCO}s + \omega_{LCO}^2}{s} = D \cdot K_{I2} \frac{s^2 + \frac{k}{A_{LCO}}\omega_{LCO}s + \omega_{LCO}{}^2}{s} \tag{5}$$

where ω_{LCO} and A_{LCO} are the radial frequency and amplitude of LCO, respectively. In accordance with the procedure described in [6] the compensator zeroes are adjusted with factor k to minimize the influence of the second-order pole in $G_{vd}(s)$. Initially the gain K_{I2} is set at a low value and the self-tuning compensator is switched into the second auto-tuning mode.

As shown in Fig. 5, the resulting loop gain, T_{AT2}(s), in this mode reassembles behavior of a pole at origin and the whole system behaves as an integrator, i.e.

$$T_{AT2}(s) = M_{dpwm}(|d|,s))G_{C2}(s)G_{vd}(s)M_{ADC} \approx \frac{K_P}{s} \tag{6}$$

To complete compensator design and achieve desired bandwidth, the gain of compensator in (5) needs to be determined. The gain estimation is performed in two steps: 1) LCOs at the desired crossover frequency are introduced and 2) the value of K_I is determined from the measurements of the small signal gain of nonlinear element, i.e. DPWM.

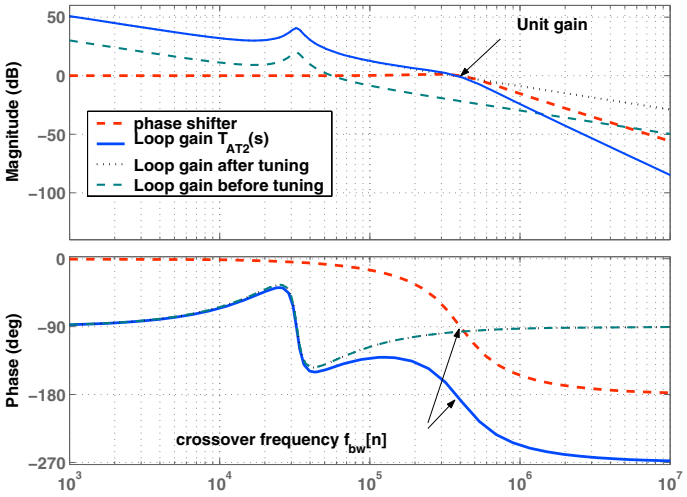

Fig. 5. Bode plots of systems during second step tuning

The idea is based on the fact that *at the amplitude and frequency of LCO the gain of nonlinear element, i.e. DPWM, is automatically adjusted to result in unit loop gain* $T_{AT2}(s)$. In other words, if the LCO occur at predefined crossover frequency, the gain of DPWM is exactly equal to the desired value of K_I when the nonlinear effect is eliminated and the controller operates in regular mode utilizing high-resolution DPWM.

The abovementioned two-step process is performed during the second auto-tuning step, when all switchers of Fig. 3 are in the position *a.t.*2. In this case, the PI compensator of the first step is replaced with the initially designed low-gain PID (5) and a programmable phase shift block is added. For example, in this case we use a second-order unity-gain low-pass filter with programmable cutoff frequency as our phase shifter. The

programmable phase shift introduces additional -90° at the desired frequency, $f_{bw}[n]$, to result in the total phase shift of 180° and LCO at the same frequency. After the LCOs are initiated the gain of DPWM (desired K_I) is determined through measurement of the ratio of variations of the truncated signal $d_{tr}[n]$ and its high resolution value (see Fig.3)

$$M_{dpwm} = K_I = \frac{\Delta d_{tr}[n]}{\Delta d_2[n]} \tag{7}$$

Finally, the self-programming PID is switched to regular mode and the initial low gain value is replaced with the one given in (7). Because the phase shifter is removed the resulted new closed-loop system will have a phase margin of 90 degree as shown in Fig. 5.

It should be noted that in actual system implementation the bandwidth of the controller can be compromised with the processing delays of the other elements of the system caused by finite processing and analog-to-digital conversion times. In addition, the delays of the uniformly sampled DPWM need to be included. Thus, there are several delays in the control loop and, correspondingly, the specification on the required phase margin (or bandwidth) needs to be adjusted accordingly. The proposed autotuning procedure can be easily extended to account for these delays by representing the control-loop transfer functions in the Z-domain, including the PWM modulator transfer function and the control and ADC delays [9]. However, under the assumptions that the time delay is much smaller compared to time constants of the desired system and controller bandwidth far from PS corner frequency, the proposed method may be applied to achieve acceptable dynamic responses.

IV. System Verification

Based on diagrams shown in Fig.1 a Matlab/Simlink model of a 200 kHz 12 V-5 V buck converter is built and the results

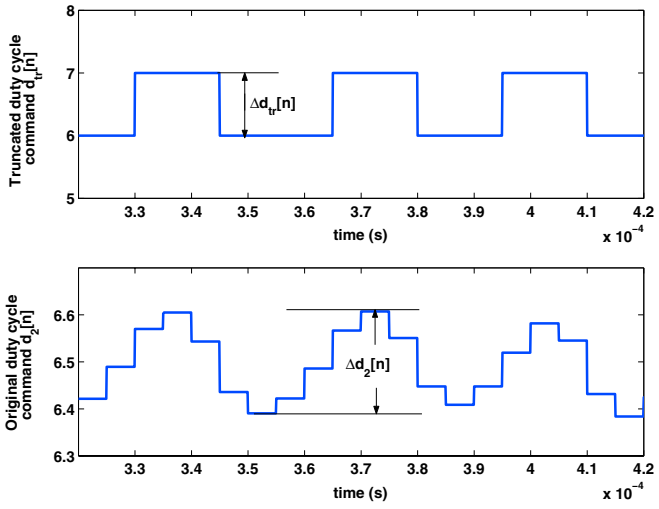

Fig. 6. Input (bottom) and output (top) of the nonlinear element (DPWM quantizer)

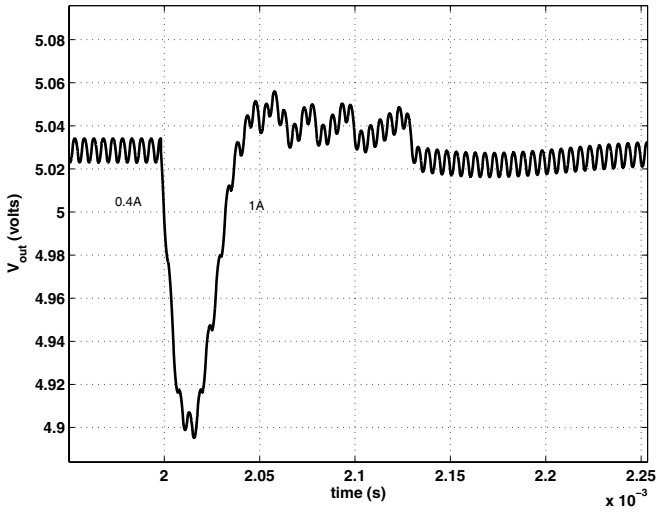

Fig. 7. Transient response of the auto-tuned system to a load current change from 0.4A to 1A

proving the proper operation of the system are obtained. The system parameters used in the simulations are: L=20μH, C=47μF, switching frequency f_{sw} =200 kHz and Controller bandwidth 60 kHz. Some results of first step auto-tuning have been explicitly reported in [1] and will not be included here. Results of the newly proposed second step auto tuning are shown in Fig. 6 to 7. The truncated DPWM signal $d_{tr}[n]$ and its high resolution input signal $d_2[n]$ are shown in Fig. 6 respectively. It is seen that the resulted LCO frequency is around 30 kHz. As we stated in previous section the discrepancy from designated controller bandwidth is a result of system delays. Form this example, it also shows that the system has an ability to provide a good control bandwidth by itself even in the case of an unrealistic bandwidth setting. The gain of DPWM is obtained to be equal to 5 by applying (7). Figure 7 shows load transient response of the auto-tuned system for output current change from 0.4A-1A. It is seen that the output is able to settle down in 6 switching cycles (30 μ s), which is comparable to state of the art analog solutions. An FPGA-based physical prototype utilizing the presented controller architecture is currently under construction. Experimental results will be presented in our future work.

V. Conclusions

A self-programmable PID compensator is presented. It is shown how the information extracted from limit-cycle oscillations (LCOs) can be used for automatic compensator design. The system has relatively simple hardware structure and as such is suitable for low-power SMPS applications, where auto-tuning methods have not been usually used due to the high complexity of conventional auto-tuning methods designed for high power systems. Effective operation of the system is verified through Matlab/Simulink simulations and it was shown that fast transient response comparable with state of the art analog solutions can be achieved.

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