Digital Pulse-Frequency/Pulse-Amplitude Modulator for Improving Efficiency of SMPS Operating Under Light Loads

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***Abstract*— In this paper we show a novel digital control method for improving efficiency of SMPS operating at light loads and demonstrate its hardware implementation. In discontinuous conduction mode (DCM) it simultaneously performs a change of switching frequency and peak amplitude of the inductor current in order to achieve better efficiency than conventional pulse-frequency modulator solutions. Supporting analysis, simulations, and experimental results verify advantages of this control method.**

I. Introduction

In recent years digital control of low-power switch-mode power supplies (SMPS), used in portable battery-powered devices, has gained significant interest. It offers advantages such as the use of automated design tools to shorten the design time, simple portability among different technology processes, and low sensitivity to external influences such as process and temperature variations. Furthermore, digital control allows a simpler implementation of advanced power management techniques [1] [2]. In battery-powered handheld devices, such as cellular phones, digital still cameras (DSC) and personal data assistants (PDA), these techniques play a very important role. They usually achieve significant extension of battery life through dynamic adjustment of supply voltage and changes of SMPS mode of operations. In all operating modes it is required that SMPS operate with high efficiency. Efficient power processing is required both during heavy mode, when the supplied device performs complex tasks and requires a significant amount of power, and in light mode when the supplied device power requirements are minimized. Even though portable devices usually spend more than 80% of battery energy operating as light loads, most of the attention has been devoted to the problems of efficient digital controller implementation for SMPS supplying heavy loads. Solutions based on the use of linear regulators and analog pulse-frequency modulation (PFM) controllers have been proposed for the light load conditions [3]. These solutions are not so easy to integrate with predominantly digital hardware and in the case of linear regulators result in relatively low overall power processing efficiency. In this paper we show a novel digital control method for improving efficiency of SMPS operating at light loads and demonstrate its hardware implementation, which is shown in Fig. 1. In discontinuous conduction mode (DCM), it performs simultaneous change of switching frequency and peak amplitude of the inductor current to achieve better efficiency than conventional pulse-frequency modulator

The following section describes operation of the new digital pulse-frequency/ pulse-amplitude (DPFM/DPAM) controller. Section III presents a comparative analysis of the efficiency of a converter operating in PFM and DPFM/DPAM showing advantages of the new control method. It also gives guidelines for selection of the optimal peak current amplitude and frequency of operation that, for a given condition, result in maximum converter efficiency. In section IV we show details of DPFM/DPAM controller realization. Section V presents experimental results that verify successful controller implementation.

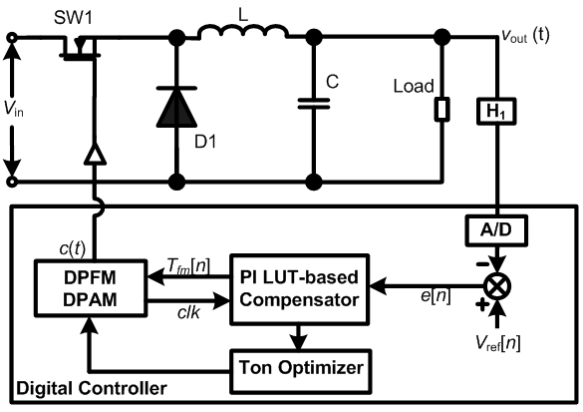

Fig. 1. DPFM/DPAM System Overview

II. Overall System Description

The DPFM/DPAM controller of Fig. 1 is used to regulate the output voltage of a switching converter operating in discontinuous conduction mode (DCM). To obtain an error signal $e[n]$

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the output voltage is converted into its digital equivalent and compared to a reference with a low-power analog-to-digital converter (ADC) [5]. Upon the conversion, the error signal, $e[n]$, is passed to a digital PI compensator and a Ton optimization block that create two control signals for the digital pulse-frequency/ pulse-amplitude modulator (DPFM/DPAM). The switching frequency control signal, $f_{pf}[n]$, is defined through a look-up table based PI compensator and the $t_{ON}[n]$ signal, whose value is proportional to the maximum amplitude of the inductor current. The calculation of $t_{ON}[n]$ is based on a predefined algorithm that maximizes efficiency of the SMPS for all operating conditions. In other words, this controller simultaneously changes switching frequency and transistor on-time to minimize the sum of switching and conduction losses.

To minimize power consumption of the controller, the whole system is clocked at the switching frequency, by f_{clk} signal, created with DPFM/DPAM block.

III. Efficiency Maximization and Optimal DPFM/DPAM Operation

In this section we investigate conduction and switching losses of a converter operating in DCM to determine an optimal control algorithm for the above described controller. As a case study, a conventional buck converter of Fig. 1 is analyzed. The major sources of losses are switching losses and conduction losses. Switching losses occur due to the switching action of current-carrying nodes over some voltage range, and conduction losses occur due to the current flowing through non-ideal resistive semiconductor devices.

The dominant switching losses are due to the high side transistor, $SW1$, because the voltage across it switches all the way from the input voltage, V_G, to the ground voltage. Furthermore, the various capacitances associated with the node that is connected to $SW1$ and the inductor, L, contribute significantly since this node also switches from the input voltage, V_G, to the ground voltage. The switching losses of the low-side device(which can be either a diode or a MOSFET) are negligible since it would be switching with only a diode voltage drop across it in the worst case. The dominant conduction losses are due to the on-resistance, $R_{ON,high}$ of the high side transistor, and in the case of a diode, the forward voltage drop, V_{FD}. If a synchronous transistor were used instead, its conduction losses would be also due its on-resistance, $R_{ON,low}$. In both cases, there is an associated reverse recovery charge associated with the low side power device, Q_r.

Fig. 2 shows the inductor current $i_L(t)$ of the buck converter supplying the same load using different transistor on-times, $T_{ON,1}$ and $T_{ON,2}$. We can see that by decreasing the on-time, we have to increase the switching frequency $f_{sw} = 1/T_{sw}$ to maintain the same average value of the load current. This modulation of the ton time is referred to as Pulse-Amplitude Modulation(PAM). By allowing a larger amplitude (or ton time), we allow the output filter elements to charge up for a longer period of time, hence taking a longer time to dissipate this stored energy, resulting in a smaller switching frequency.

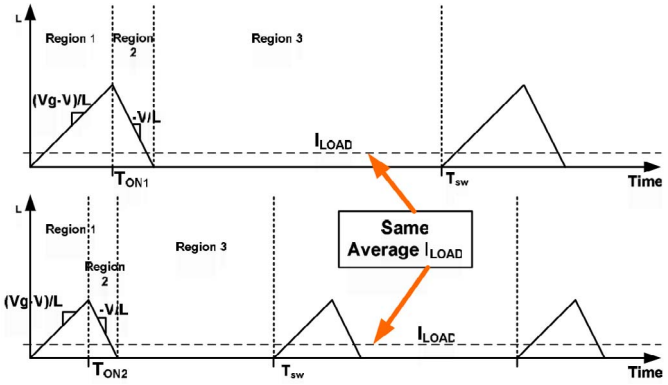

Fig. 2. Induction Current for different values of T_{ON}

Hence, over the same amount of time different conduction and switching losses occur. In the first case, the devices have smaller switching losses since they switch less frequently, but have larger conduction losses due to a longer T_{ON} time. In the second case, they have larger switching losses, but a lower conduction loss due to the smaller T_{ON} time.

Our goal is to analyze the total average power losses, given by the following approximate equations, (1) and (3), to find the optimal operating conditions under which losses will be minimized. The losses are listed for two cases, one where a diode is used as the low-side power device, and one where a synchronous MOSFET is used. For a low-side diode:

$$P_{Loss} = \frac{1}{T_{SW}} \int_1 i_L^2(t) R_{ON,high} dt \quad (1)$$

$$+ \frac{1}{T_{SW}} \int_2 i_L(t) V_{FD} dt + Q_r V_g f_{SW} \quad (2)$$

and for a low-side Mosfet:

$$P_{Loss} = \frac{1}{T_{SW}} \int_1 i_L^2(t) R_{ON,high} dt \quad (3)$$

$$+ \frac{1}{T_{SW}} \int_2 i_L^2(t) R_{ON,low} dt + Q_r V_g f_{SW} \quad (4)$$

Since we are operating under DCM the converter conversion ratio as shown in (5) is:

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + \frac{8LT_{SW}}{RT_{ON}^2}}} \quad (5)$$

For a constant output voltage:

$$\frac{T_{SW}}{RT_{ON}^2} = K \rightarrow Constant \quad (6)$$

By combining the previous two equations and finding the minimum of the function describing the losses we obtain the following expressions for optimal T_{ON} time. In the case of a diode, we have:

$$T_{ON,Opt} = \sqrt[3]{\frac{6Q_r V_G L^2}{R_{ON,h}(Vg - V)^2}} \quad (7)$$

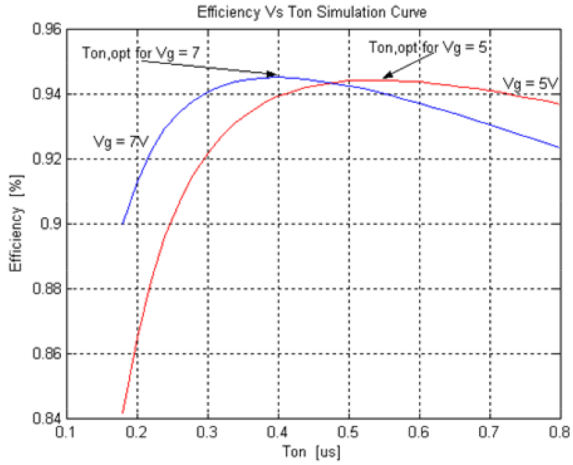

Fig. 3. Simulation Plot of Efficiency Vs T_{ON} for low-side diode

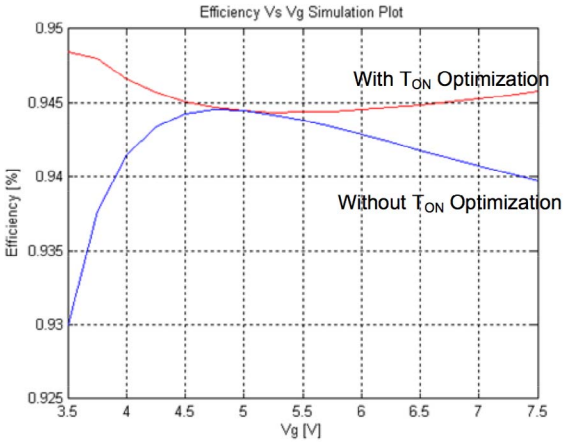

Fig. 5. Simulation Plot of Efficiency Vs V_G

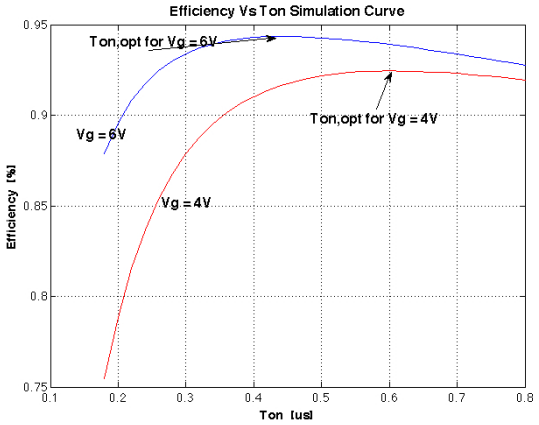

Fig. 4. Simulation Plot of Efficiency Vs T_{ON} for low-side MOSFET

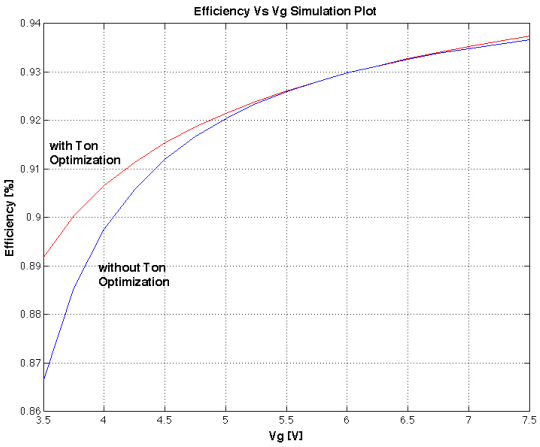

Fig. 6. Simulation Plot of Efficiency Vs V_G

For a synchronous MOSFET, we have:

$$T_{ON,Opt} = \sqrt[3]{\frac{6Q_r V_G L^2}{R_{ON,h}(Vg-V)^2 + R_{ON,l}(V)(Vg-V)^3}} \tag{8}$$

Figs. 3 and 4 show optimal ton times for different supply voltages for the case of a diode and a MOSFET as the low side power device respectively. It can be seen the optimal T_{ON} depends on the supply voltage. As the supply voltage changes, the efficiency of the system also changes if the ton time is kept constant, and so the selection of a fixed on-time, used in conventional PFMs, does not result in minimum losses. Figs. 5 and 6 show a comparison of converter efficiency of conventional PFM versus the one with optimized on-time. From the above figures it can be seen that an approximate improvement of efficiency can be up to 10% for certain operating conditions.

In order to realize a controller that optimizes T_{ON} based on V_G in the digital control architecture shown in Fig. 1, we do not necessarily need to measure V_G. Since in our control loop, information about the T_{ON} time, output voltage, and switching frequency are readily available we can easily estimate the input voltage value and adjust T_{ON} time accordingly. As we have mentioned before, under Discontinuous Conduction Mode, the conversion ratio is given in (5). Re-arranging that equation to solve for V_G, we obtain:

$$V_G = \frac{V}{2}\left(1 + \sqrt{1 + \frac{8LT_{SW}}{RT_{ON}^2}}\right) \tag{9}$$

From the above equation, the only uncertain factor lies in the load resistance value, R. The other factors, T_{ON}, T_{SW}, and V are already available in the control loop. Once this load resistance is estimated, we can directly figure out the input voltage. The switching frequency under steady state in DCM is a function of the load current(which in turn is directly related to the load resistance). If the load current is higher, then the switching frequency is higher as well. This proportionality between the two can be used to estimate the load resistance, and hence, the input voltage, and this information can be pre-stored into the control loop.

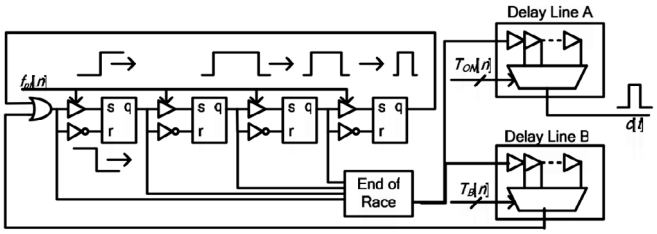

Fig. 7. All-Digital DPFM/DPAM

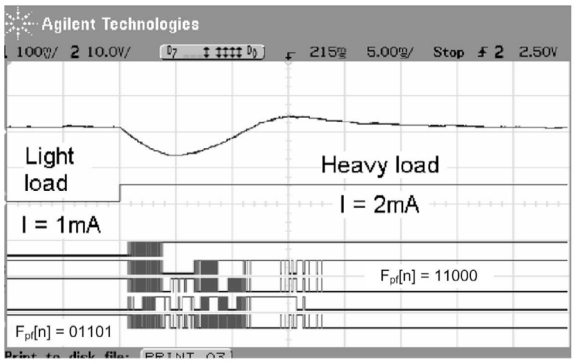

Fig. 8. Closed loop FPGA-based DPFM operation

IV. Digital Pulse-Frequency/Pulse-Amplitude Modulator (DPFM/DPAM)

The digital pulse-frequency/pulse-amplitude modulator shown in Fig. 7 is based on a modification of recently presented DPFM architecture [5] [6]. Unlike the previous design, the new solution allows independent adjustment of switching frequency f_{SW} and transistor on-time and, consequently, successful implementation of the above described optimization algorithm. The modulation of the transistor ton time is referred to as Pulse-Amplitude Modulation(PAM). By changing the ton time, we can directly change how long the inductor can be charged up for, and hence directly control the peak inductor current. This in turn will influence the switching frequency, along with the switching and conduction losses. By increasing the ton time, we will have a smaller switching frequency, as was shown in Fig. 2.

The DPFM/DPAM comprises of four main components, including two programmable delay lines, a ring oscillator, and an end-of-race detection block. Both delay lines consist of a multiplexer and a set of 32 digital delay cells, and both are triggered with the same start signal. The first delay line, A, is used to regulate the transistor on-time, by changing the 5-bit digital control input $t_{ON}[n]$. The second one, delay line B, is part of the frequency regulator block that also includes a 5-bit ring oscillator with programmable delay cells, and the end-of-race detector. To create programmable long time intervals, i.e. low-frequency signals, the delay line B produces two time shifted pulses that propagate through the ring oscillator. The first pulse is initiated with the rising edge of the trigger signal and propagates through the ring oscillator at a slower rate than the second pulse, which is delayed by the delay line

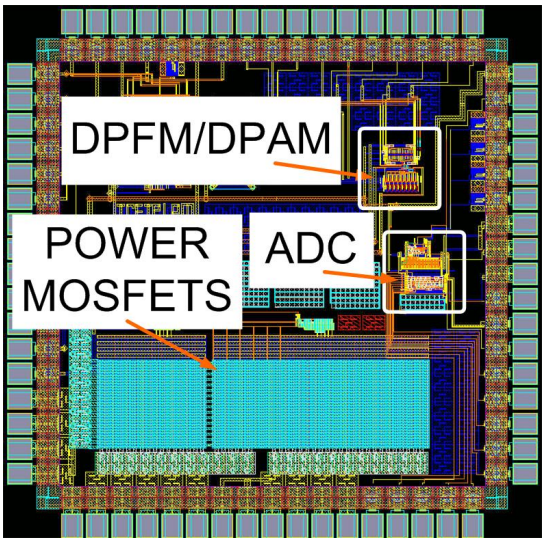

Fig. 9. Layout of DPFM/PAM in standard 0.18um CMOS Process

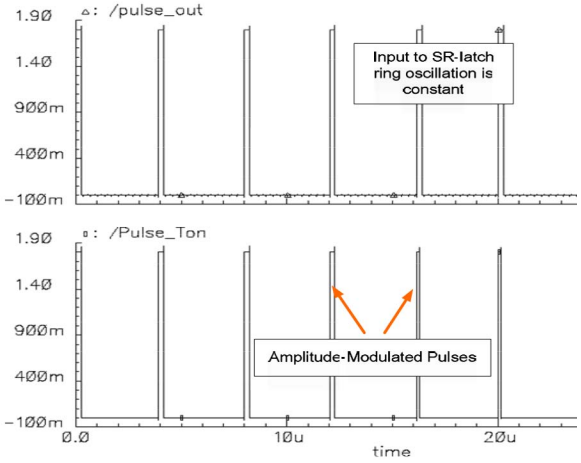

Fig. 10. DPAM in open-loop control input step

B. The first signal passes through the ring oscillator as a rising edge, setting a series of S-R latches into a 'high' state, and the delayed second signal travels as the falling edge and resets the latches. When all the latches are in a 'low' state, the end of race is detected and a new triggering signal is created, thereby restarting the whole process again. In this way long time intervals are created using fast digital logic. Fine adjustment of switching frequency is achieved through the resulting coarse changes of two 5-bit binary signals $T_{ON}[n]$ and $f_{SW}[n]$, which control propagation times through delay line B and programmable ring oscillator cells, respectively. The fine adjustment of the switching frequency is another advantage over the design presented in [5].

V. Simulation and Experimental Verification

The DPFM/DPAM controller described in Figs. 1 and 7 has been implemented on an FPGA system and an application specific IC utilizing the new architecture. The following figures show simulation and experimental results of both structures.

Fig. 8 shows closed loop operation of the FPGA system. It can be seen that the system successfully regulates the output voltage by changing the switching frequency. Figures 9 and 10 demonstrate results of on-chip implementation. Additionally, the main characteristics of the implemented DPFM/DPAM IC are summarized in Table I. They show that the new DPFM/DPAM architecture exhibits very low power consumption and can be implemented on a small silicon area, which make it suitable for portable devices.

TABLE I
ON-CHIP IMPLEMENTATION PARAMETERS

DPFM Range	$20kHz - 500kHz$
DPAM Range	$10ns - 400ns$
Active On-Chip Area	$0.01950mm^2$
Power Consumption	$3\mu A$

VI. CONCLUSION

This paper presents digital PFM/PAM control which results in better efficiency than conventional PFM. To achieve better efficiency the controller utilizes a novel digital architecture that allows active adjustment of both switching frequency and transistor on-time. Effective operation of the new controller has been verified through mathematical analysis, simulations and experimental results.

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