Programmable Digital Controller for Multi-Output DC-DC Converters with a Time-Shared Inductor

Amir Parayandeh, Andrija Stupar, Aleksandar Prodić
Laboratory for Low-Power Management and Integrated SMPS
University of Toronto, ECE Department
Email: {amiran, prodic}@ele.utoronto.ca; a.stupar@utoronto.ca

Abstract— This paper introduces a low power digital PFM controller for multi-output dc-dc converters suitable for integration in modern low-power management systems. It utilizes only one inductor to provide multiple output voltages and has very low power consumption. In addition, its reference voltages and switching frequency can be programmed dynamically. To achieve these characteristics two new key functional blocks are developed, namely Σ-Δ programmable delay-line based comparator utilizing natural filtering of delay cells and on-time control logic. The controller is implemented both on FPGA and a 0.18-*μm* CMOS application specific IC. Experimental results obtained with a 1 W, 9 V, four-output buck prototype and IC simulations successfully verify controller operation.

I. INTRODUCTION

Modern portable applications require multiple supply voltages for two notable reasons. Modern portable devices generally require multiple low-power supplies for their functional blocks. For example, in digital still cameras (DSC) and cell phones, different supply voltages are used for a LCD screen, handset lighting, and camera flash. Additionally, with increase in speed and circuit density, power consumption has become a critical issue in battery operated portable devices. It has been shown that using multiple supply voltages on chip appears as a viable solution for reducing power consumption [1]-[5]. As a result, the means of providing different supply voltages on chip, in low cost and small area solutions, are becoming increasingly important [6]-[11].

Most of the existing commercial solutions combine multiple switching converters to supply the different blocks. In these systems each power stage uses a separate inductor, power switches and controller resulting in relatively large part number and size of the power module. To minimize the number of components and simplify control, multiple output flyback converters are also commonly used. However, they suffer from poor output regulation due to cross-coupling [12]. In addition, switching transistor is exposed to excessive voltage stress [13]. The controller proposed in [6] uses only one feedback loop to provide multiple supply voltages with improved regulation. This solution still requires several inductors, which are among the largest obstacles in successful minimization of low-power switching converters. Reduction in inductor numbers can be achieved through designs proposed in [7-10]. Using time-multiplexing of a single inductor these designs provide multiple regulated outputs. These solutions use analog controllers operating in discontinuous conduction mode (DCM) to provide precise regulation of output voltages However, in these solutions, output voltages are fixed and implementation of advanced power management techniques through dynamic output voltages adjustment is not a simple task. Even though the flexibility of digital hardware is known, in portable applications, digital PFM controllers for multiple-output supplies have not been commonly used, mostly due to their high power consumption that often exceeds the power delivered to the loads.

In this paper we introduce a new low power digital controller architecture that provides tight regulation of multiple programmable supply voltages for light loads and allows simple implementation of power management techniques in portable applications. As shown in Fig.1, similar to analog solutions [7-10], the controller utilizes the fact that in PFM the inductor current is discontinues hence it can be time-shared between multiple outputs. Besides output voltages, the on-times of power switchers can also be dynamically changed. Therefore the switching frequency, maximum currents stress, and output ripple can also be indirectly controlled. Dynamic adjustment of on-times also allows for minimizing the switching losses for a given converter topology [14]. In the following section we briefly explain operation of the time-shared multi-output digital PFM controller. Section III describes novel low-power architectures of basic functional blocks. IC implementation and experimental results obtained with a FPGA prototype utilizing the new architecture are shown in Section IV and Section V summarizes the main results.

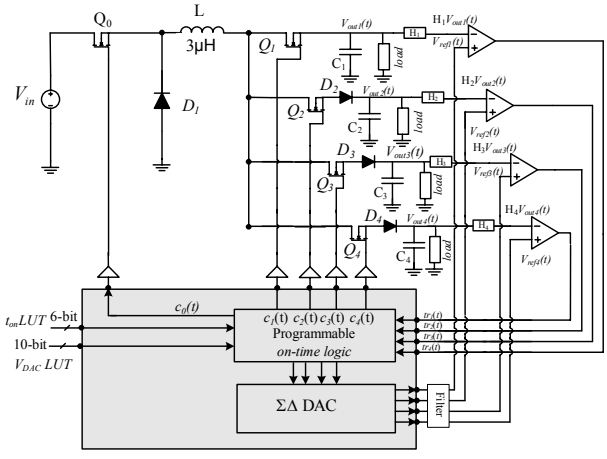

Fig. 1: Single inductor multi-output DC-DC converter based on a Digital PFM controller.

This work of Laboratory for Low-Power Management and integrated SMPS is supported by Sipex, Milpitas, CA, USA.

II. SYSTEM OPERATION

The power supply of Fig.1 is a four-output buck converter controlled with the new digital PFM controller. The output voltages are regulated using a set of four delay-line based comparators and programmable *on-time logic*. The reference voltages of the comparators are programmed by Σ-Δ digital-to-analog converters (DAC) and compared to output voltages. When an output voltage $v_{outi}(t)$ falls below reference, comparator Q_i sends a signal to the *on-time logic* that turns on the corresponding transistor Q_i and the main switch Q_0 simultaneously for the pre-programmed fixed period t_{on_i} allowing output capacitor C_i to be charged. During this time all other transistors are disabled to prevent cross regulation among output stages and if signals from other comparators go high, they will be detected by the *on-time logic* and served in the order of occurrence. The diodes D_2 to D_4 prevent cross-conduction from high to low output voltage stages. The output $v_{out1}(t)$ is reserved for the lowest output and does not require a diode. It should be noted that the diode D_1 can be replaced with synchronous rectifiers having zero current crossing detectors to minimize the losses.

III. ARCHITECTURES OF BASIC FUNCTIONAL BLOCKS

All the blocks of the multi-output controller are designed with two specific goals in mind. They are constructed to be mostly digital and to have very low power consumption, comparable to the state of the art analog solutions. Therefore, the proposed architecture can be easily transferred from one implementation technology to another and used in various low-power applications.

A. Programmable On-Time Logic

Programmable *On-time logic* of Fig.2 consists of a block named *stage selector*, two look up tables (LUT), 4-to-1 demultiplexer, and only one programmable delay line. Based on the trigger signals $tr(t)$ received from output comparators, *stage selector* creates a 2-bit signal *sel*. This signal is fed to inputs of 4-word LUTs that produce binary values $t_{on}[n]$ and $V_{ref}[n]$ for the delay line and Σ-Δ DAC (Fig.1), respectively.

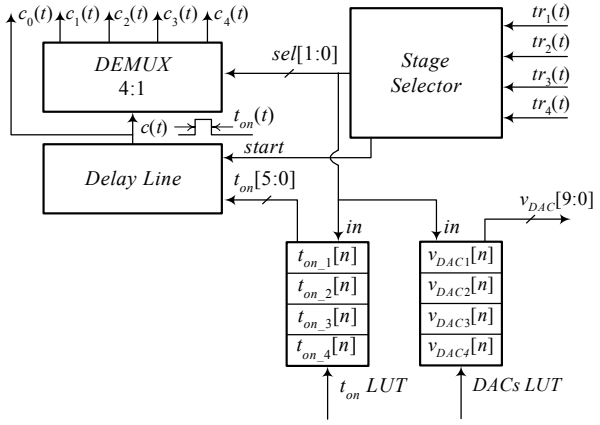

Fig. 2: Programmable on-time logic

The select signal also controls the 4-to-1 demultiplexer which distributes signal $c(t)$, of duration t_{on}(t) to appropriate power switchers. While one trigger signal is served, *stage selector* also monitors outputs of the other comparators and processes any request after the ongoing task is completed.

B. Delay-line

Instead of using a counter that requires an external clock signal and, in some cases, consumes significant amount of power, to create on-time, a programmable delay-line [15] is used. The delay line has very simple low-power structure and does not need a high frequency external clock. Fig.3. shows a six-bit delay line architecture composed of two delay-lines. Each delay-line consists of 8 current-starved delay-elements tabbed into an 8-to-1 multiplexer. The propagation delay of delay-cells in *MSB* delay-line is 8 times larger than in *LSB* delay-line. This is achieved by copying proportionally smaller bias current in delay-cells of *MSB* delay-line.

The on-time value $t_{on}[n]$ is connected to the control inputs of the multiplexers. Three most significant bits are tied to *MSB* MUX and three least significant bits are connected to *LSB* MUX. After *start* signal, created by *stage selector* of Fig.2, goes high the signal first propagates through t_{on}[5:3] *MSB* delay-cells and consequently passes through t_{on}[2:0] *LSB* delay-cells before resetting the SR latch at the output of *LSB* delay-line. Therefore programmable on-time signal is created. Once operation is complete delay-line is reset internally for the next cycle.

C. Delay-line based Comparators

The comparator circuit shown in Fig.4 is a modification of the delay-line analog to digital converters presented in [16],[17]. The inputs of the comparator are a converter output voltage and a reference created by Σ-Δ DAC. The main novelty is that this design utilizes the averaging effect of delay-lines to minimize the size of the filter required at the output of Σ-Δ DAC. The comparator is clocked with an external sampling signal and its output depends on the difference in propagation times of two delay lines. The delay-lines consist of current starved delay-cells [15], [16] where propagation time of each cell is controlled by input

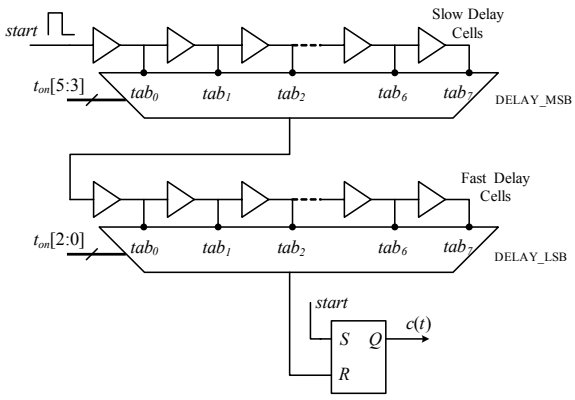

Fig. 3: Segmented Delay-line

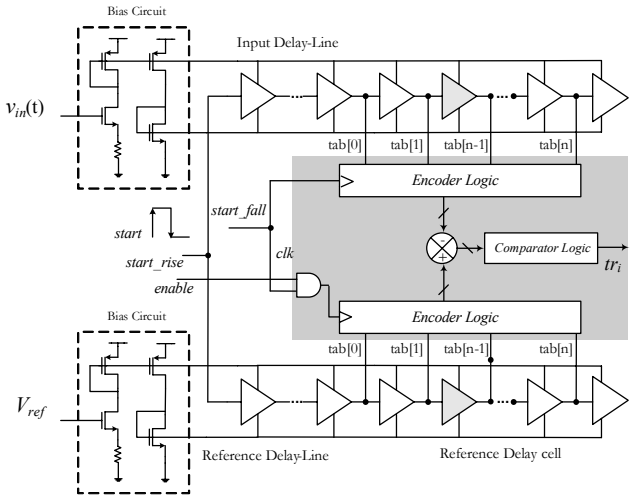

Fig. 4: Delay- line based Comparator.

voltage of the bias circuit. The output of each delay-line is monitored by *Encoder Logic* block which transfers the thermometer output to a binary number.

On rising edge of the clock signal a pulse starts propagating through input delay-line and reference delay-line with a speed proportional to input and the reference voltages, respectively. The *Encoder Logic* captures the output states of delay lines on falling edge of the clock. The digital code from the reference delay-line is subtracted from the input delay-line to represent differential voltage V_{ref} - $v_{out}(t)$. Finally, the comparator logic takes this value and generates the comparator output signal.

To minimize the power consumption *Encoder Logic* and reference delay-line are only active for a few power stage switching cycles, when the Σ-Δ DAC is running. When *enable* signal is low, Σ-Δ DAC goes to sleep mode and the *Encoder Logic* stores the digital code corresponding to the previously captured value of the reference voltage. In subsequent switching cycles the captured value of the output voltage delay line is compared to this stored value.

The low power consumption of comparator is also due to efficient design of delay cells. They only switch once during the comparison period and are designed with bias currents in μA range. In addition the bias circuit is powered down after the comparison is complete. Design specification and power figures of comparators implemented on chip are given in section IV.

D. Programmable Voltage Reference

To create programmable voltage reference a single-bit Σ-Δ digital-to-analog converter (DAC) illustrated in Fig.5 is used. The DAC consists of a bandgap voltage reference, a single-bit Σ-Δ modulator, control transistors, a ring oscillator that provides internal clock for Σ-Δ modulator, and output filter. In this new implementation the output filter comprises of two parts, a small RC-circuit setting the dc reference point for delay line and delay line itself, which eliminates the filter ripple influence.

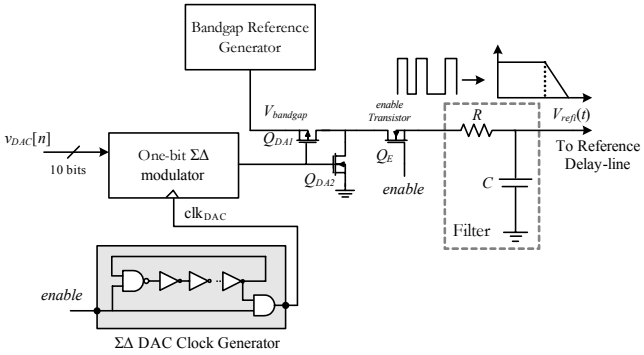

Fig.5: Σ-Δ DAC block diagram

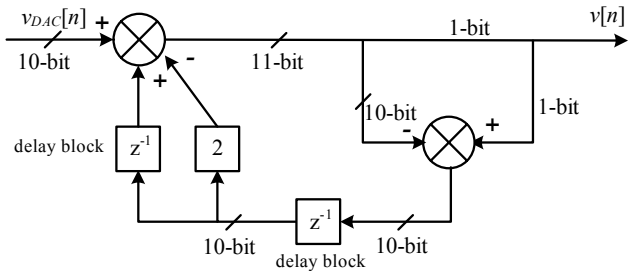

Fig.6: Single-bit Σ-Δ Modulator base on error feedback structure

The Σ-Δ modulator is based on the well-known error-feedback architecture [18] that has low power consumption and simple structure as shown in Fig. 6. Through transistors Q_{DA1} and Q_{DA2} it modulates the bandgap voltage $V_{bandgap}$ to result in an average value proportional to the product $V_{bandgap}$ x $v_{DAC}[n]$, where $v_{DAC}[n]$ is provided from the programmable *on-time logic* of Fig.2. This voltage is passed to the filter through enable transistor, Q_E.

Generally, in Σ-Δ modulators there is a tradeoff between the clock frequency, power consumption, and the size of the output RC filter. To allow fast averaging and small filter size, a high frequency clock signal is required. This results in high power consumption. On the other hand, a low frequency clock requires large RC components to achieve small ripple at the output of the DAC. Such RC filters require large on chip area and are impractical for IC implementation.

To reduce the filter size and maintain low power consumption in this case we used a relatively low frequency clock and divided filtering task in two parts. First, a small RC filter, with low ripple rejection, is used to set the voltage around desired reference. Then, the inherent averaging effect of the reference delay line is utilized to eliminate the ripple component.

The averaging effect of a delay line can be described with the following analysis and its frequency response shown in Fig.7. The propagation time of a pulse through delay-line (Fig.4) depends on the average value of bias current, i.e. applied voltage, over the propagation period T_s.

For the reference delay line, the average voltage and its Fourier transform are

$$v_{ref\_av}(t)=\frac{1}{T_s}\int_{t}^{t+T_s} v_{ref}(\tau)d\tau$$

$$v_{ref\_av}(t)=\frac{1}{T_s}\int_{-\infty}^{t+T_s} v_{ref}(\tau)d\tau-\frac{1}{T_s}\int_{-\infty}^{t} v_{ref}(\tau)d\tau \xleftrightarrow{F}$$

$$V_{ref\_av}(j\omega)=V_{ref}(j\omega).\frac{\sin j\omega\frac{T_s}{2}}{\omega\frac{T_s}{2}}.e^{-j\omega\frac{T_s}{2}} \qquad (1)$$

The frequency response of this function is shown in Fig.7. It behaves as a low-pass filter with cut off frequency of

$$f_c = 0.45\frac{1}{T_s} \qquad (2)$$

In this case, to eliminate RC-filter voltage ripple, f_c is selected to be significantly lower than the Σ-Δ modulator clock frequency.

Eq (2) shows that we can change f_c by regulating propagation time, T_s , through delay lines. This can be achieved by changing the number or propagation delay of delay cells.

As mentioned before, the power consumption of the Σ-Δ DAC is further reduced by operating it sporadically, once in many switching cycles. During this period *enable* signal is high. When *enable* goes low, the ring oscillator is disabled and Σ-Δ modulator goes to sleep mode to reduce power consumption. The transistor Q_E also turns off leaving high impedance across the RC-filter and keeping the output capacitor voltage, $V_{ref}(t)$, constant. Hence, in the following DAC operating cycle a small amount of energy is needed for its recharge. In addition *Encoder Logic* is not clocked any further and retains the digital code corresponding to the average value of $V_{ref}(t)$.

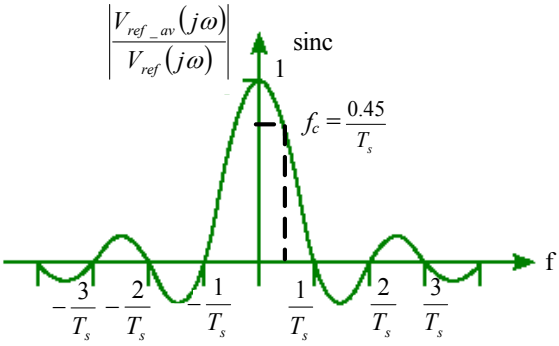

Fig.7: Frequency Response of a delay line.

IV. FPGA EXPERIMENTAL RESULTS AND INTEGRATED CIRCUIT (IC) IMPLEMENTATION

To verify the operation of the new architecture an experimental FPGA prototype based on the diagram shown in Fig.1 is built. In addition we designed an application specific IC utilizing the same architecture. The results of the IC design are verified through HSPICE simulations.

A. FPGA Implementation

The input voltage of the experimental multi-output buck prototype is between 4 V and 8 V, and the outputs are regulated at 1.8V, 2.2V, 2.5V and 3.3V. The output load was varied between 1 mA and 50 mA maintaining discontinuous current and PFM regulation for all operating conditions.

1) Steady State Operation

Fig. 8 demonstrates the operation of the multi-output buck converter in steady state. It can be seen that the simultaneous tight regulation of all output voltages is achieved and that the current going through the inductor is discontinuous and shared among different output stages.

2) Dynamic Mode

Operation of system when the digital reference and output load are changing is shown in Figs. 9 and 10. From Fig.9 it can be seen that the output voltage can be digitally programmed and dynamically changed. Results of the output load change experiment are showed in Fig.10. They demonstrate that the system maintains good output voltage regulation and that the cross-conduction problems between neighboring stages do not exist.

B. IC Implementation

The digital controller architecture is implemented on an application specific IC in 0.18-µm CMOS technology. The layout of the chip and its specifications are demonstrated in Fig.11 and Table I, respectively.

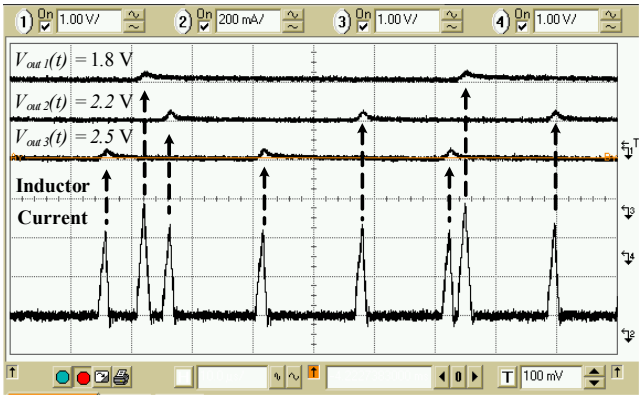

Fig.8: Steady state operation of the multi-output buck converter with time shared inductor: Ch1, Ch3, and Ch4–output voltages; Ch2-inductor current. Time scale is 5µs/div.

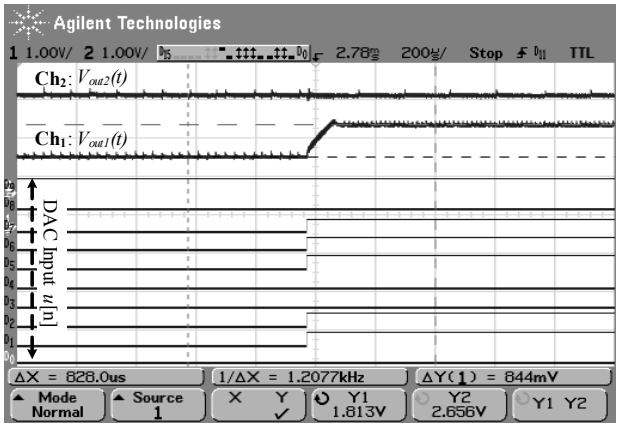

Fig.9: Transient response to change of digital voltage reference: D0 to D9 digital reference; Ch.1: corresponding output voltage change from 1.8V to 2.65V Ch.2: The output voltage of a neighboring stage.

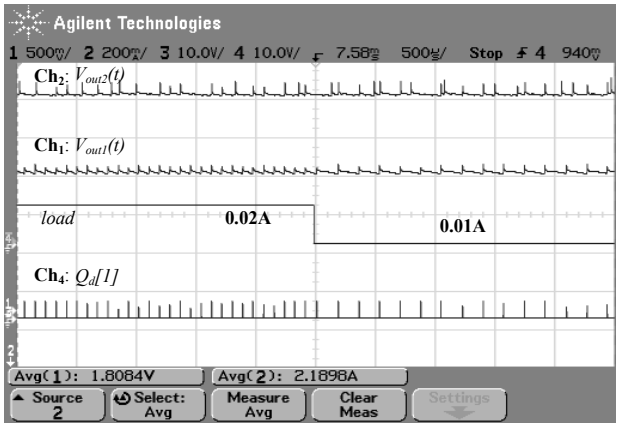

Fig.10: Transient response to load change between 20 mA and 10 mA: Ch.1: the output voltage of stage regulating voltage at 1.8 V and operating in steady state; Ch.4: corresponding gate drive signals; Ch.2: The output voltage of a neighboring stage.

1) IC Specifications

The current consumption of On-Time Logic block of Fig.3 is measured assuming switching frequency of 100 kHz. Table I shows that new functional blocks have very low power consumption. The Σ-Δ DAC current consumption is measured when a conservative update rate of once per one hundred switching cycles is selected. It should be noted that this update rate can be further reduced if frequent calibration of reference is not needed.

TABLE I
CHIP SPECIFICATIONS

Comparator Current Consumption	35 μA at 1MHz comparator clk
On-Time Logic Current Consumption	21 μA/100 kHz
Σ-Δ DAC quantization step	3 mV
Σ-Δ DAC Current Consumption	2.5 μA
Σ-Δ Modulator *clk* frequency	130 MHz
RC - filter values	40 kΩ , 4pF
RC-filter on-chip area	0.009 mm^2

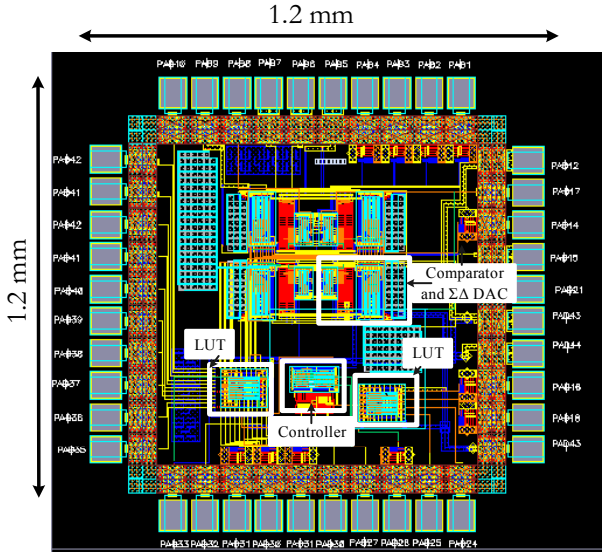

Fig.11: Digital Controller IC Layout

2) Simulation Results

Fig. 12 demonstrates filtering effect of the delay line. It shows the voltage of RC-filter capacitor generated by the Σ-Δ DAC of Fig.5 and digital code for the reference delay-line. It can be seen that the output of the reference encoder (Fig.4) is constant even though a large voltage ripple at the capacitor output exists. To achieve the DAC resolution of Table I using conventional RC-filter the RC product would need to be about 50 times larger resulting in much larger on-chip area

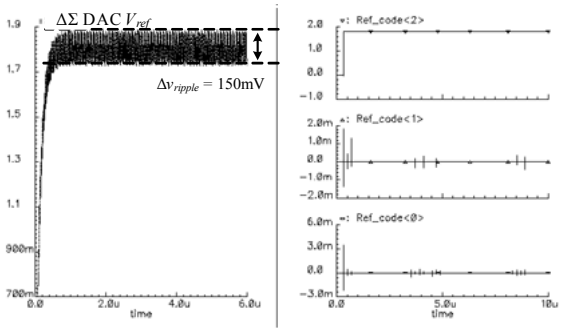

Fig.12: Simulation result of Σ-Δ DAC output voltage , and digital error code for reference delay-line

V. CONCLUSION

A programmable digital controller for low power multi-output dc-dc converters used in battery-powered devices is shown. The controller allows time-sharing of the inductor between programmable output voltages. It features programmable on-time logic and a Σ-Δ DAC with two-step filtering blocks to achieve very low-power consumption and small on-chip area. The operation of the controller is verified by an FPGA prototype and simulation of application specific IC.

REFERENCES

[1] J.M Chang , M. Pedram "Energy Minimization Using Multiple Supply Voltages", *IEEE Trans. Very Large Scale Integration (VLSI) Systems,* Volume 5, Issue 4, Dec. 1997 Page(s):436 – 443.

[2] K. Usami, M. Igarashi, F. Minami, T. Ishikawa,M. Kanazawa,M. Ichida,and K. Nogami, "Automated low-power technique exploiting multiple supply voltages applied to a media processor," *IEEE J. Solid-State Circuits*, vol. 33, pp. 463–472, Mar. 1998.

[3] L. S. Nielsen, C. Niessen, J. Sparsø, and K. van Berkel, "Low-power operation using self-timed circuits and adaptive scaling of the supply voltage," *IEEE Trans. VLSI Syst.*, vol. 2, pp. 391–397, Dec. 1994.

[4] M. Johnson and K. Roy, "Scheduling and optimal voltage selection for low power multi-voltage DSP datapaths," in *IEEE Int. Symp. Circuits and Systems*, Volume 3, 9-12 June 1997 Page(s):2152 – 2155

[5] K. Usami and M. Horowitz, "Clustered voltage scaling technique for low-power design," in Proc. Int. Workshop Low Power Design, 1995.

[6] A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, "High-efficiency multiple-output dc-dc conversion for low-voltage systems," *IEEE Trans.VLSI Syst*., vol. 8, pp. 252–263, June 2000

[7] Ma,W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, "Single-inductor multiple-output switching converters with bipolar outputs," in *IEEE International Symposium on Circuits and Systems* Volume 3, 6-9 May 2001 Page(s):301

[8] D. Ma,W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode" *IEEE J. Solid-State Circuits*, Volume 38, Issue 1, Jan. 2003 Page(s):89 – 100

[9] D. Ma,W.-H. Ki, C.-Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching" *IEEE ISSCC*. Digest of Technical Papers. Volume 1, 3-7 Feb. 2002 Page(s):390 - 476 vol.1

[10] D. Goder and H. Santo, "Multiple output regulator with time sequencing," U.S. Patent 5 617 015, Apr. 1997

[11] Data Sheet No. TPS65120, " Single-Inductor Quadruple-Output TFT LCD Power Supply ", Texas Instruments

[12] D Maksimovic, R.W. Erickson, and C. Griesbach, "Modeling of cross-regulation in converters containing coupled inductors " , *IEEE Trans. PowerElectron*., vol. 15, pp. 607 - 615, July 2000.

[13] R. W.. Erickson, D. Maksimovi´c, Fundamentals of Power Electronics, 2nd edition, Kluwer Academic Publishers, 2000

[14] N.Rahman, K.Wang, A.Prodic "Digital Pulse-Frequency/ Pulse-Amplitude Modulator for Improving Efficiency of SMPS Operating Under Light Modulator for Improving Efficiency of SMPS Operating Under Light Loads.

[15] A. Syed, E. Ahmed, D. Maksimovic, E. Alarcon, "Digital pulse width modulator architectures " in Proc. IEEE Power Electronics Specialists Conference, June 2004, pp. 4689 – 4695.

[16] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. PowerElectron.*, vol. 18, pp. 438–446, Jan. 2003.

[17] N.Rahman, A.Parayandeh, K.Wang, A.Prodic "Multimode Digital SMPS Controller IC for Low-Power Management", *IEEE International Symposium on Circuits and Systems,* May 2006, accepted paper.

[18] D. Johns, K.C. Martin, " Analog Integrated Circuit Design " , 1st edition, John Wiley & Sons, 1997

.