Continuous-Time Digital Signal Processing Based Controller for High-Frequency DC-DC Converters

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Abstract- **This paper introduces a digital dual-mode controller for low-power high-frequency dc-dc switch-mode power supplies (SMPS) suitable for on-chip implementation. In steady state the controller behaves as a conventional digital PWM controller, and during transients it utilizes continuous-time digital signal processing to achieve very fast transient response. The continuous time DSP is triggered by a sudden change of output voltage. Then it performs a charge-balance based algorithm to achieve voltage recovery through a single on-off action of the power switch. The effectiveness of the method is demonstrated on an experimental 5 V-to- 2V, 400 kHz, 2.5 W buck converter that recovers voltage in the time equivalent to 3 PWM switching cycles, approaching converter physical limitations.**

I. INTRODUCTION

Low power consumption and fast transient response are among the most common requirements in low-power switched-mode dc-dc power supplies (SMPS) for handheld devices. In analog controller implementations such characteristics are achievable with various types of designs [1]-[2]. On the other hand, even though advantages of digital control have been recognized (flexibility, design portability, simple implementation of power management techniques), they have not been widely adopted in low-power systems. Most of the existing low-power digital controllers still use simple proportional-integral-derivative (PID) compensators with very limited bandwidth. The bandwidth limitation is mostly caused by sampling effects and various delays introduced by the voltage loop. As shown in [3] higher sampling frequency allows limited expansion of the controller bandwidth, but at the same time puts a requirement for a power hungrier analog-to-digital converter (ADC).

In analog implementations, nonlinear strategies, such as hysteresis control [1]-[2] show faster responses than linear PID compensators. However, in conventional hysteretic implementations the switching times are not optimized and in some cases, large overshoots and sags in output voltage due to a large amount of accumulated current in inductor could occur [4]. As a result the power stage components go through an extra stress and overdesign of the system is often required. In [4], an enhanced version of hysteresis control is proposed where optimal power switch on/off time is calculated from capacitor charge balance to prevent large overshoots. It achieves steady state in one single switching cycle but still requires costly and power consuming current sensing. This method still suffers from the most common drawbacks of analog hysteresis control. The converter operates at a variable switching frequency causing additional stress on components and undesirable noise.

Fast transient response can also be obtained with methods presented in [5]-[6], which implement charge balance based algorithms. The presented systems are targeted for medium and higher power applications, where complex calculations in digital domain are performed. The systems are based on a modification of digital current-mode PWM controller. These controllers result in very fast load transient responses, but also require real-time inductor current sensing and a high-resolution ADC. The complexity of hardware requirements makes this implementation less suitable for low-power applications, operating at high switching frequencies.

In this paper, we introduce a digital controller that achieves very fast transient responses without the need of current sensing and can be implemented with fairly simple power-efficient hardware. The controller, shown in Fig.1, achieves low power consumption in steady state by using a PID compensator that does not change its states frequently. During transients, a novel continuous-time digital signal

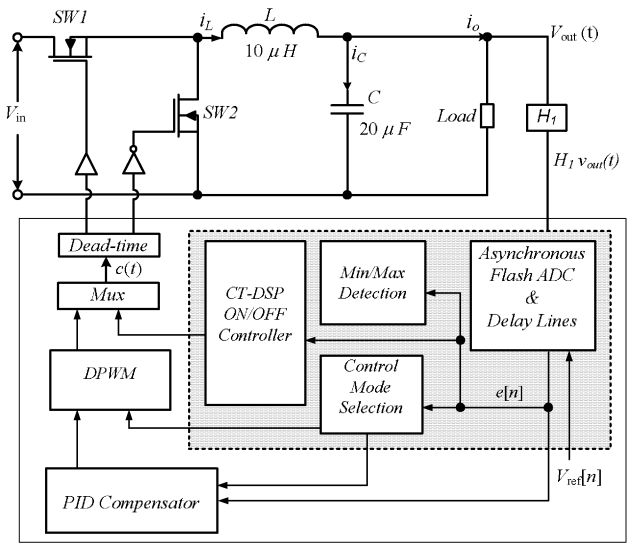

Fig. 1 Digitally controlled SMPS with a dual mode controller using continuous-time digital signal processing technique.

processor (CT-DSP) is used, to achieve very fast dynamic responses. The CT-DSP instantaneously identifies the quantities needed for capacitor charge-balance calculations, such as peak/valley voltage values and the time points at which they occur. The capacitor charge-balance calculation is then performed with the assistance of look-up tables to determine the optimal on and off switching time for the controlled SMPS.

The following section gives a brief review of the continuous-time digital signal processing concept and explains the benefits of applying it to SMPS. In Section III we describe a new charge-balance based control algorithm utilizing this concept to improve controller responding speed while eliminating the need of current sensing. The experimental setup and results are presented in Section IV. Section V concludes the paper.

II. Continuous-Time Digital Signal Processing

Continuous-time DSP concept, introduced by Tsividis [7]-[9], is a means of performing digital signal processing without conventional time sampling. Having no sampling makes the output of CT-DSP a function of continuous time. The typical setup of CT-DSP requires an asynchronous ADC or quantizer as its input port and a set of delay cells. When a continuous input signal $x(t)$ is quantized by the asynchronous ADC with quantization levels q_i, $i=1,2...k$, as shown in Fig. 2, the output data $b(t)$ has discrete amplitude values but is a function of continuous time [8]. The signals are then processed instantly with combinational logic.

As an example, Fig.3 shows a typical block diagram of CT-DSP for a one-bit FIR filtering application. Analog signal $x(t)$ is quantized by an array of asynchronous comparators, i.e. a flash ADC. The digital output of each comparator is used to trigger a string of adjustable continuous-time delay cells T. The delayed binary data is fed to combinational logic realizing an FIR filter. The details of CT-DSP implementation can be found in [9].

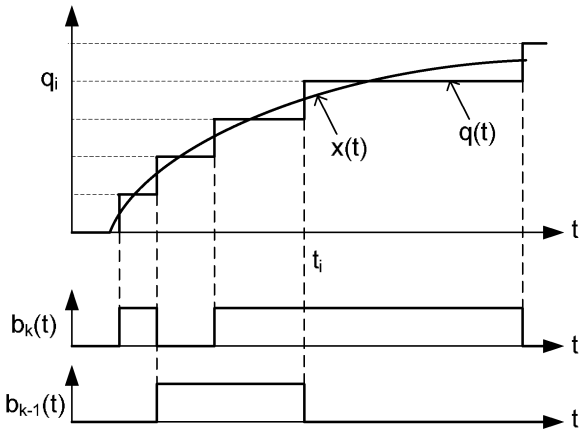

Fig. 2 Waveforms for analog input signal x(t) and two output bits of asynchronous ADC as well as quantized input signal q(t) .

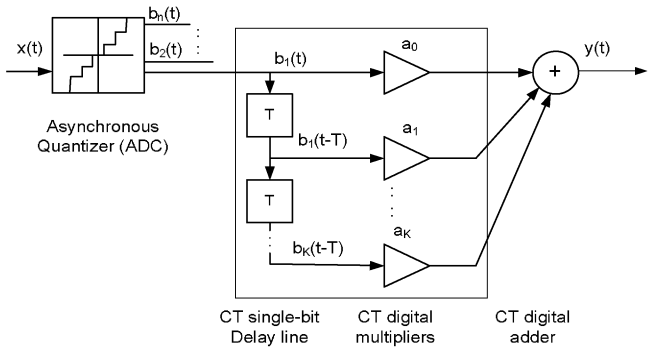

Fig. 3 A typical FIR filter structure realized by CT-DSP

In the context of SMPS control, the main advantage of non-clocked CT-DSP is ability to instantaneously detect output voltage changes and its values during transition period. The detection can be performed without aliasing and quantization errors [7] and it can be followed by immediate data processing in digital domain. The quantization step in CT-DSP as well as propagation times of delay cells are chosen by the designer and the continuous-time analog signal can be reconstructed from the states of delay cells. In addition, with the utilization of asynchronous comparators as quantizers it can be made very power efficient. This is because asynchronous comparators can be designed to consume power only during state transitions [11]. In steady state the CT-DSP is practically inactive and consumes no power.

Because of the abovementioned advantages of CT-DSP, the responding speed of SMPS controllers can be improved significantly. For example, in a traditional PID compensator, output voltage change is detected with a certain delay, upon periodic sample of the output is taken. In addition to that processing of the sample takes certain amount of time and a strong reaction of the compensator is usually delayed by several switching cycles. On contrary, the CT-DSP based controller detects the transient upon the triggering of any of its comparators. Practically, at the point of triggering the exact output voltage is sensed without quantization error (i.e. it is the same as the threshold of the comparator) and is processed instantly by combinational logic so that accordance control actions can be taken immediately. In addition, the processing of quantized signals in the digital domain preserves all the benefits of digital control.

The implementation of CT-DSP has matured significantly since it was first introduced. On-chip implementation and results have been reported in [9]. In this paper we show that low-power SMPS can also benefit from the utilization of this novel concept. As it will be shown soon, transients response limited by the size of output filtering components only can be achieved without paying a significant penalties in hardware complexity and power consumption.

III. DUAL-MODE CONTROLLER ARCHITECTURE

A. System Operation Overview

In this section, we present a dual-mode controller for effective and fast control of load transients. The controller consists of a slow PID compensator and CT-DSP structure. Fig.1 shows the overview of controller architecture. In steady-state the PID compensator, which is designed to be very power efficient [8], regulates the voltage. During transients, the CT-DSP on-off controller takes over and provides very fast responses. Based on the error signal *mode selection* module determines the mode of operation.

The PID compensator operates only when the error, $e[n]$ is within ± 3, while the on-off controller is in action when that range is exceeded. The PID law generates the duty cycle control variable $d[n]$ by summing the previously sampled error values, $e[n\text{-}1]$ and $e[n\text{-}2]$ with the past output value $d[n\text{-}1]$ [8]:

$$d[n] = d[n-1] + Ae[n] + Be[n-1] + Ce[n-2] \qquad (1)$$

where, A, B, and C are compensator coefficients.

The operation of the on-off CT-DSP controller is based on simple capacitor charge-balance principle. It can be explained by observing arbitrary heavy-to-light load transient waveforms of output voltage and inductor current, shown in Figs. 4 and 5. The controller response is divided into two phases. In the first phase, upon the load transient, the CT-DSP turns the main switch M_1 on (see Fig.1) to accommodate the change in output load. The first period is limited by the valley point, as shown in Fig.4. At that time instant, local minimum is reached and *the load current and inductor current are the same.* In the second phase the controller makes up for the charge lost in output capacitor. It calculates t_{on} and t_{off} sequence needed for the fastest possible compensation of the lost capacitor charge and

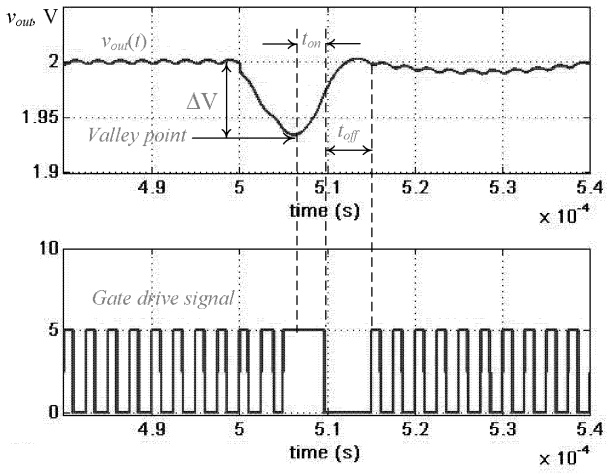

Fig. 4 A typical light-to-heavy load transient response of the CT-DSP controller (output voltage).

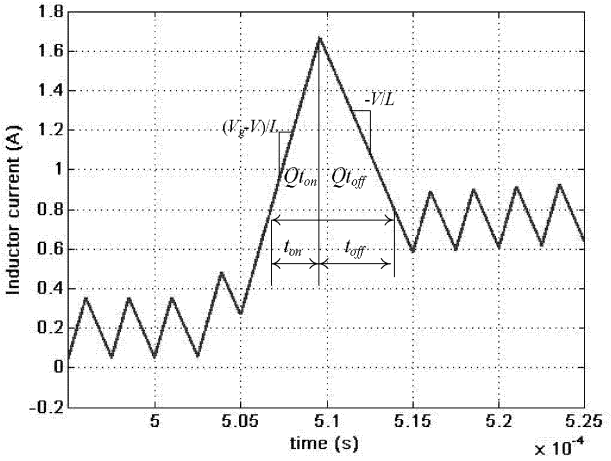

Fig. 5 A typical inductor current waveform of a light-to-heavy load transient response of the CT-DSP

delivers a smooth transition from the transient to steady-state. As soon as the second phase ends, the conventional PID compensator again takes over the control and ensures stable operation. Similarly off-on sequence is used to control heavy-to-light load change.

B. Charge-balance based Algorithm for Optimal On-Off Time Sequence Calculation

It has been shown in [5]-[6] that SMPS converters recovers from load variation in optimum time by employing a single power switch on-off (or off-on) action. In the presented papers a current measurement based computations are used. In here, we show how the calculations of the optimal time can be done without current sensing.

The t_{on}/t_{off} sequence is calculated under the assumption that the voltage dip during the transient is relatively small compared to regulated dc value (less than 10 %). The load transient triggers *min/max* module (Fig.1), which finds the valley and peak points (local minimum or maximum) of the output voltage. For the waveform of Fig.4, the valley is found by examining the sign of the error signal and the change in slope of the output voltage reconstructed in CT-DSP delay lines. Once the valley is found, the amount of the lost/gained charge in output capacitor is obtained by:

$$Q = C\Delta V \qquad (2)$$

where ΔV is the voltage deviation at the peak/valley point.

During "t_{on} time" (see Fig.5) $i_L = i_C + i_{load}$ the change of i_L, Δi_L, equals approximately the change of capacitor current i_C, Δi_C.

It should be noted that CT-DSP automatically detects the local minimum/maximum, as a mid-time point at which the largest excitation of the output voltage has been detected.

Thus, the amount of charge transferred to the capacitor during t_{on} and t_{off} intervals can be described with the following equations:

$$Q_{t\_on} = \iint_{At_{on}} \frac{V_g - V_{out}}{L} dtd\,\tau \quad (3)$$

$$Q_{t\_off} = \iint_{At_{off}} \frac{V_{out}}{L} dtd\tau \quad (4)$$

where V_g and V_{out} are input voltage and dc value of the output voltage, respectively.

As demonstrated in Fig.5 the relation between t_{on} and t_{off} can be obtained geometrically, by knowing the input voltage value (we assume that the output voltage is known as the reference voltage):

$$\frac{t_{on}}{t_{off}} = \frac{Q_{t\_on}}{Q_{t\_off}} = \frac{V_{out}}{V_g - V_{out}} \quad (5)$$

By combining (2), (3) and (4) we obtain the following condition for the charge balance.

$$Q_{t\_on} + Q_{t\_off} = Q = \Delta VC \quad (6)$$

or

$$t_{on} = \sqrt{\frac{2LC\Delta V V_{out}}{V_g\left(V_g - V_{out}\right)}} \quad (7)$$

It can be seen that (5) requires the knowledge of LC product, V_g, as well as calculation of the radical. Inaccurate knowledge of LC product value influences the performance of the proposed control algorithm. However, as it is shown in [10] the accurate knowledge of LC and V_g can easily be obtained by performing a simple limit-cycle oscillation based power stage identification test. The calculation of the radical values is performed using look-up tables.

From (5) t_{off} is obtained for each operating point. As soon as t_{off} interval ends, the control law is switched back to PID. The initial conditions for the PID compensator is reset to have all zero values for $e[n\text{-}1]$ and $e[n\text{-}2]$ and initial duty ratio equal to V_{out}/V_g. Presumably, at this moment, the output voltage and inductor current are at their new steady state values, the small discrepancy of duty ratio from its new steady state value will be corrected by the PID control law without causing large output deviations. This effect will be observed in next section where experimental results are shown.

IV. Experimental System and Results

The proposed CT-DSP based high performance SMPS controller of Fig 1 is implemented with a Cyclone II Altera DE2 FPGA, and standard high speed comparators. The programmable delay cells in CT-DSP are emulated on the FPGA board although they can also be implemented with solid-state components. The experimental setup has a switching frequency of 400 kHz, an output capacitor C = 20uF and an inductor L = 10uH.

First, to verify benefits of this method responses to light-to-heavy step load changes of a conventional PID compensator and the proposed dual-mode controller are compared. The load current is stepped up from 0.2A to 1.2A. The output voltage responses of the controlled buck converter as well as the inductor current waveforms in both cases are shown in Fig. 6 and Fig. 7 respectively. It can be seen that the PID takes 60 us

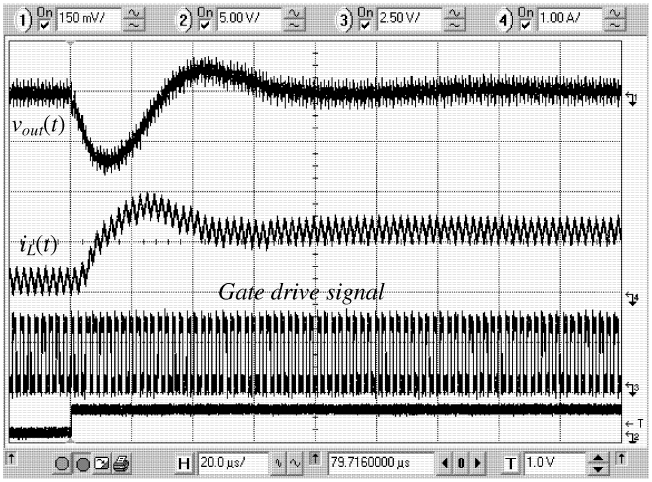

Fig. 6 PID controller response to a 0.2A->1.2A load step change. The waveforms from top to bottom are: output voltage $v_{out}(t)$ (150mV/div), inductor current $i_L(t)$ (1A/div), gate drive signal (2.5V/div) and load change command signal (5V/div) respectively. X-axis:20us/div.

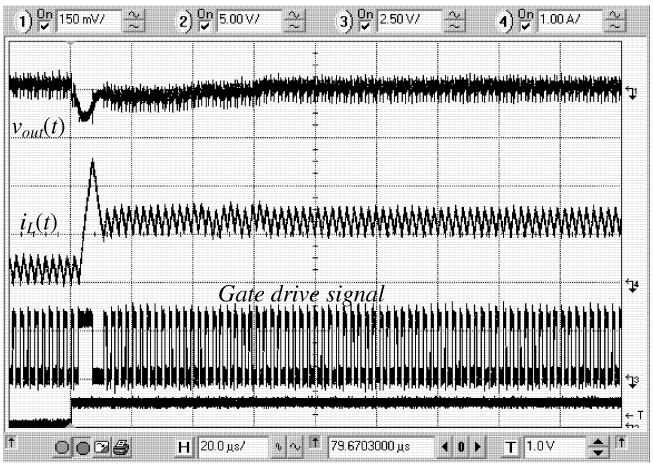

Fig. 7 CT-DSP controller response to a 0.2A->1.2A load step change. The waveforms from top to bottom are: output voltage $v_{out}(t)$ (150mV/div), inductor current $i_L(t)$ (1A/div), gate drive signal (2.5V/div) and load change command signal (5V/div) respectively. X-axis:20us/div.

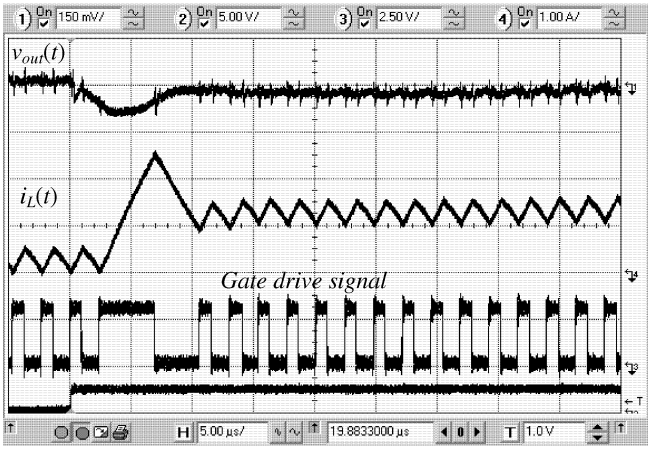

Fig. 8 Enlarged view of CT-DSP controller response to a 0.2A->1.2A load step change. X-axis:5us/div.

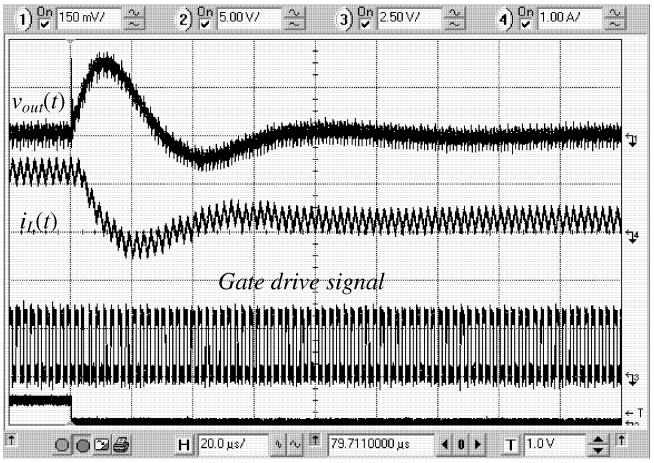

Fig. 9 PID controller response to a 1.2A->0.2A load step change. The waveforms from top to bottom are: output voltage $v_{out}(t)$ (150mV/div), inductor current $i_L(t)$ (1A/div), gate drive signal (2.5V/div) and load change command signal (5V/div) respectively. X-axis:20us/div.

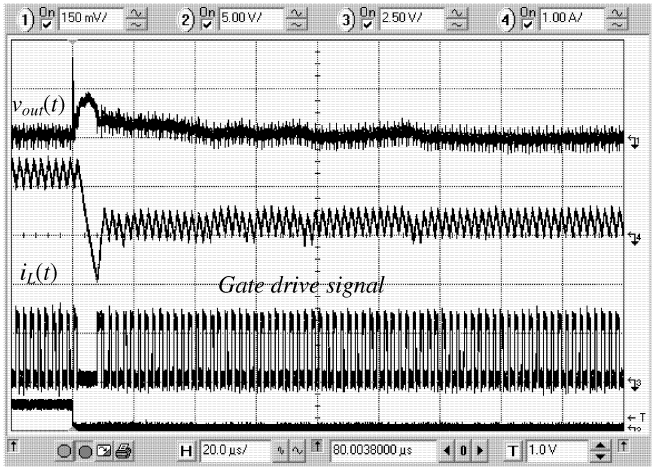

Fig.10 CT-DSP controller response to a 1.2A->0.2A load step change. The waveforms from top to bottom are: output voltage $v_{out}(t)$ (150mV/div), inductor current $i_L(t)$ (1A/div), gate drive signal (2.5V/div) and load change signal (5V/div) respectively. X-axis:20us/div.

to settle down and that maxim voltage deviation is approximately 200 mV. The proposed controller on the other hand recovers the output voltage in less than 10 us with 100 mV voltage deviation. These values are limited only by the size of LC components in the converter circuit. The current waveforms of Fig. 7 also show that at the end of the CT-DSP mode operation both the output voltage and inductor current reach their steady states in the shortest time possible. After the control is handed back to the PID controller, any imperfection in the on/off time calculation is corrected without causing large voltage overshoots. A closer view of the CT-DSP transient response is shown in Fig. 8. A single on-off action of the power switch can be clearly observed.

Figures 9, 10 show load transient responses of the converter subjected to a 1.2A-to-0.2A step load change with pure PID control and CT-DSP control respectively. Similar improvements verifying effectiveness of this method can be observed.

V. Conclusions

A new digital controller for low-power high-frequency SMPS suitable for low-power on-chip implementation is presented. It utilizes continuous-time digital signal processing to obtain a power efficient architecture and very fast dynamic response. The controller architecture is successfully tested with an FPGA experimental system and dynamic response approaching physical limitations of the power stage is achieved.

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