Universal and Fault-Tolerant Multiphase Digital PWM Controller IC for High-Frequency DC-DC Converters

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Abstract - **This paper describes a flexible 4-phase digital PWM controller IC that can be used with interleaved, multi-output, and parallel dc-dc switching converters operating at frequencies up to 10 MHz. The IC can be programmed to operate with any number of phases and it is fault-tolerant. If during interleaved mode a failure in one of the phases occurs, it automatically switches to operation with reduced number of phases by disabling the critical phase and adjusting the angles of the remaining ones. The key element of this IC is a new multi-phase digital-pulse width modulator (MDPWM) that utilizes a programmable counter, a delay line, and a digital logic with variable numbers representation. This IC is realized in a standard 0.18 μm CMOS process and exhibits low power consumption of 45 μA/MHz per phase. The controller operation is also experimentally verified with a 1 MHz, 25 W, 4-phase interleaved buck converter.**

I. INTRODUCTION

In multi stage converters, advantages of digital controllers over traditional analog solutions are becoming more evident. Digital systems allow simpler implementation of power management techniques and advanced control laws. It has also been shown that the digital controllers provide more accurate matching of multiple pulse-width modulated signals [1]-[2] and a reduction of the output voltage ripple through phase shifting. Despite these advantages, the utilization of the digital controller flexibility has been very limited. In addition, compared to analog solutions most of the existing digital controllers still suffer from the problem of a relatively high power consumption (from several tens to hundreds of miliwatts) that linearly increases with switching frequency. The high power consumption is likely to hinder the use of most of the existing digital solutions in upcoming converters, which are expected to switch 10 to 100 times faster than the existing power stages.

The main goal of this paper is to introduce a new universal IC controller (shown in Fig.1) that has low power consumption, occupies small silicon area, and exploits flexibility of digital implementation. The IC can operate as a controller for interleaved converters having 2 to 4 phases and/or simultaneously regulate operation of up to 4 different converters. Additionally, switching frequency, phase shifts, and dead-times can be digitally programmed as well. These features allow the use of this flexible controller in various applications, including voltage regulator modules (VRMs), multiple output converters for communication devices and television sets as well as in portable electronics. In interleaved mode the controller tolerates failure of up to three phases and it automatically switches to operation with reduced number of phases (for example, from 4 to 3) allowing uninterrupted operation until the problem is corrected. Although extremely valuable, these features have not been presented in other MDPWM architectures [1]-[3], mostly due to the lack of solutions for the operation with an odd number of phases.

The following section explains the operation of the universal controller IC. Section III describes the architectures of basic functional blocks. In Section IV we show an application specific IC that utilizes the new controller architecture. Experimental results verifying proper system operation are also shown in that section.

II. SYSTEM OPERATION

Fig.1 shows the universal controller regulating operation of a 4-phase interleaved buck converter. The controller consists of

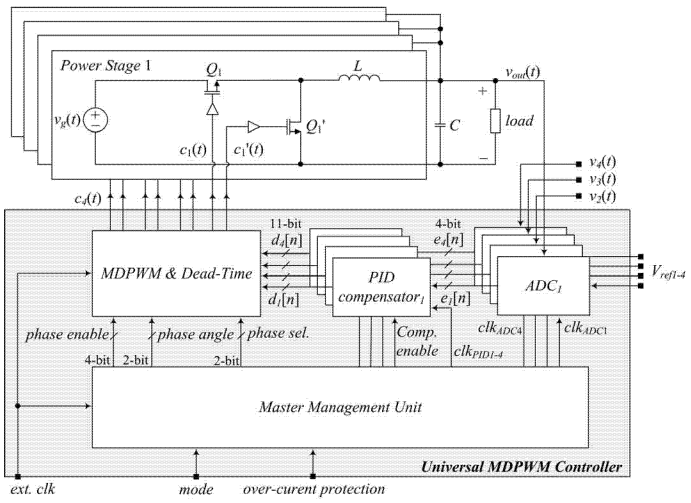

Fig.1. Universal MDPWM controller IC regulating operation of a 4 phase interleaved buck converter.

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four windowed analog-to-digital converters (ADCs) [4], four programmable PID compensators, MDPWM and dead-time blocks, both of which are also programmable, and master management unit (MMU). The number of active ADCs and compensators is regulated by MMU through mode control and over-current protection signals (*mode* and *OCP*). In interleaved mode, only one ADC and a compensator are used. When the regulation of multiple outputs is required, proportionally larger number of these blocks is activated. The MMU also creates clock signals for ADCs and PID compensators, adjusts phase shifts, and shuts down critical phases if the over-current protection signal is received. Based on reference V_{ref} the ADCs produce error signals $e[n]$ for PID compensators that create control signals for MDPWM. Depending on mode of operation, the MDPWM creates one or more pulse-width modulated signals, whose duty ratios can be independently adjusted.

III. Controller Architecture

A. Analog-to-Digital converters (*ADCs*)

The ADCs are implemented as described in [4]. An input stage based on a differential-pair and delay lines are combined to result in low power consumption and eliminate the dependence of conversion time/quantization steps on the reference voltage $V_{ref.}$ This structure also allows measurement of output voltages that are in vicinity or below CMOS transistors' threshold levels. This allows the use of this controller in modern power management system with dynamic or adaptive voltage scaling [5], where operation at voltages below 1 V is often required.

B. Multi-Phase Digital Pulse-Width Modulator (*MDPWM*)

The architecture of the 4-phase MDPWM shown in Fig. 2 is based on a modification of single-phase hybrid DPWM [6], in which a low-resolution counter and delay line are used to create a pulse-width modulated signal. In this case, a programmable counter and an element called synchronization block are introduced, both of which are shared by all phases. Each of the phases contains a Σ-Δ modulator, a programmable delay line, a logarithmic delay matching circuit and a variable number conversion block. The system is clocked by an external clock signal whose frequency never exceeds nine times the switching frequency making MDPWM chip power consumption low.

At the beginning of each switching cycle, in each of the phases, a set pulse for the RS latch is created and the corresponding dpwm signal is turned on. Its duration is varied using the counter and delay lines, which reset the latch. The core steps of the desired 11-bit duty ratio value $d_i[n]$ are set by the counter, fine adjustments are performed through delay lines, and even finer ones with the Σ-Δ modulator.

The mode of MDPWM operation depends on *phase enable* and *phase angle* signals, which select the combination of active phases and the angles between them, respectively. When the number of selected phases is 1, 2 or 4, the counter output change from 0 to 7, while when operating with 3 phases, it counts from 0 to 8. Based on *phase angle* signal, synchronization block creates set pulses sp_i that set SR latches. As an example, Fig. 3 illustrates set and counter's output signals when interleaved operation with 4 and 3 phases with phase shifts of 90° and 120° respectively is required.

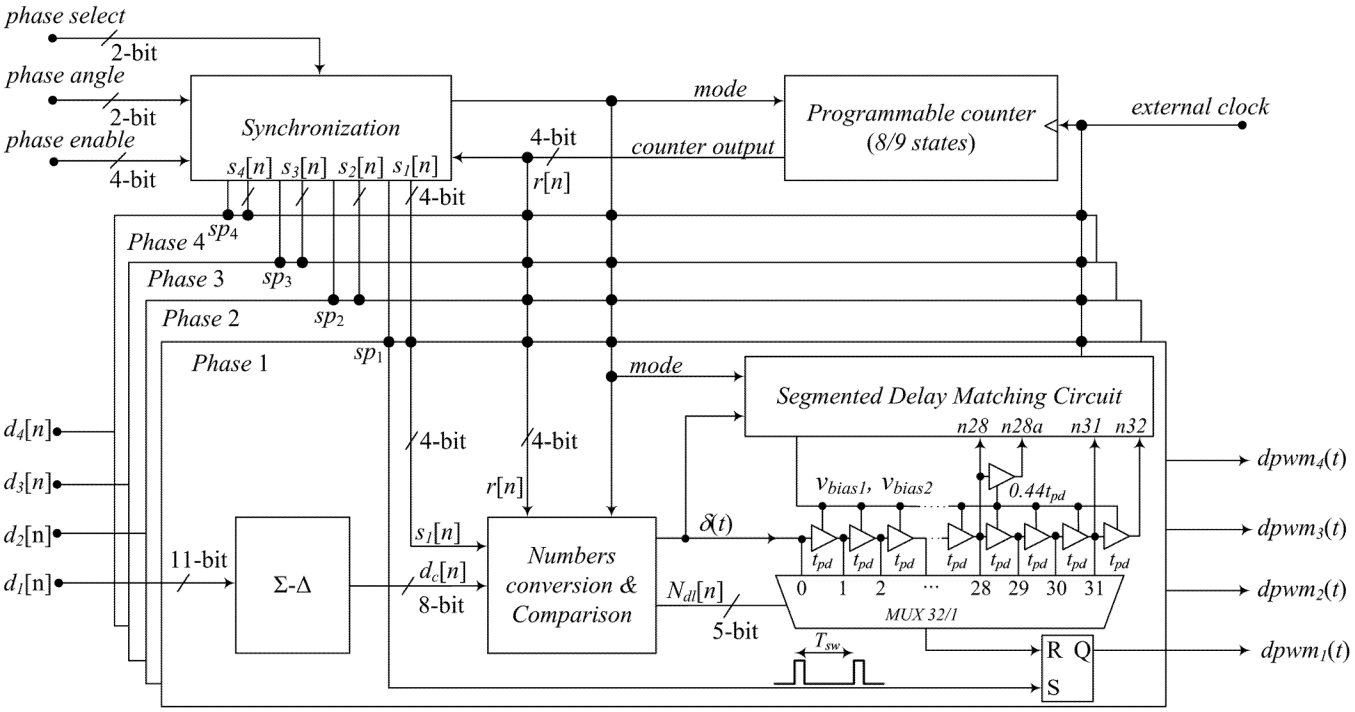

Fig.2. A block diagram of multi-phase digital pulse-width modulator.

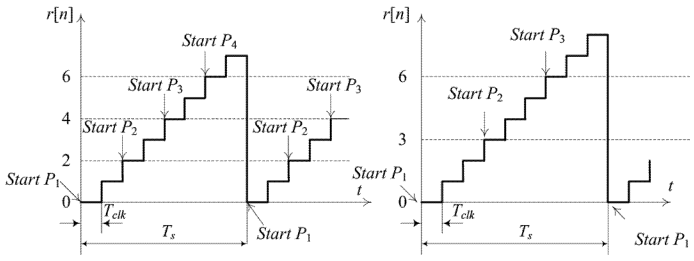

Fig.3. (a): left, start signals during 4-phase interleaved operation; (b): right, 3-phase interleaved operation.

B.1 Operation with 3 phases and Number Conversion Logic

When operating in single-phase mode or with even number of phases, creation of duty ratio value proportional to the 8-bit control input $d_c[n]$ (see Fig.2) is quite simple. Counter output goes through eight cycles and its ramping output $r[n]$ is compared with the 3-MSBs of $d_c[n]$ increased by *phase angle* value. When the two compared numbers are equal, pulse $\delta(t)$ for delay line is created. The propagation time of the pulse through 32-cell-long delay line is defined with the 5-MSBs of $d_c[n]$. In the 3-phase mode, situation is more complex. Now, in each switching cycle the counter goes through 9 steps, which combined with 32 delays, result in 288 different output duty ratio values. This number is higher than the number of possible values for $d_c[n]$ and the problem of assigning duty ratio value to appropriate input exits. If wrongly interpreted, the input values can cause non-linear or even non-monotonic input-to-output DPWM characteristic and consequent stability problems.

In order to generate a linear and monotonic characteristic, for each input value $d_c[n]$, we need to define proper portions of duty ratio increments created by the counter and delay line.

Let us define the counter and delay line increments as $\Delta D_{cn} = N_{cn}[n]/9$ and $\Delta D_{dl} = N_{dl}[n]/256$, respectively, where $N_{cn}[n]$ is a 4-bit value controlling the number of counter steps

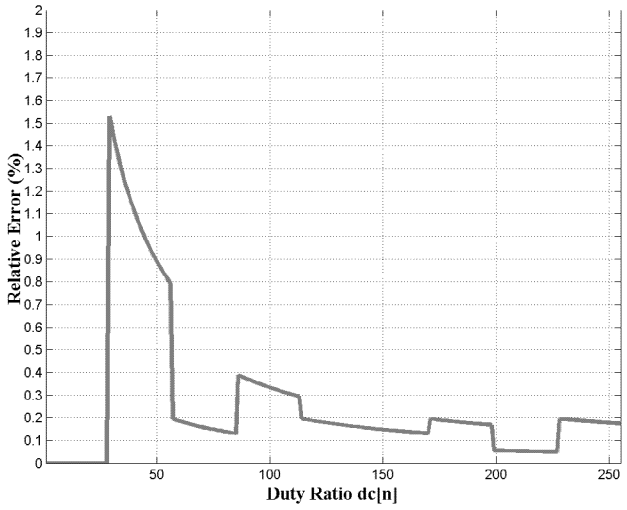

Fig.4. The relative error vs. 8-bit duty ratio command $d_c[n]$ for 3-phase MDPWM operation.

before the delay line is triggered and $N_{dl}[n]$ is a 5-bit value defining the number of delay cells as shown in Fig.2. To define these two numbers for each $d_c[n]$, we use minimum error criteria. More precisely, we look for the minimum of the following function representing the relative error in $d_c[n]$ representation:

$$\Delta_d = \frac{d_c[n]}{256} - \left(\frac{N_{cn}[n]}{9} + \frac{N_{dl}[n]}{256} \right). \quad (1)$$

The solution of this equation gives a set of 256 values of N_{cn}[n] and $N_{dl}[n]$ that result in the error distribution shown in Fig.4. These values are stored in two look-up tables and used for generating proper increment portions during 3-phase operation.

B.2 Linearization and a dual-biased logarithmic delay cell

One of the main problems in creating DPWM architectures involving a delay line and a counter [6] or segmented delay lines [6] is linearity. When a good matching between the minimum time increment of the counter and the total propagation time of delay cells is not achieved, a non-monotonic characteristic can occur [6]. As a result, at certain operating points a local positive feedback and stability problems can occur. To eliminate this problem delay-locked loop (DLL) based structures can be implemented [3], [7]. The previously presented implementations [3], [7] of the DLL are not designed for the operation over a wide-range of programmable frequencies, since they rely on delay cells that have constant time increments. Consequently, they cannot be used for the controller structure presented in this paper, where the programmable frequency can be changed between 100 kHz to 10 MHz. In this case to achieve an 8-bit resolution, the delay of cell $t_d = 1/(2^8 \cdot f_{clk})$ t_{pd} needs to vary between 390.6 ps and 39.06 ns. Conventional current starved delay cells [8] are not suitable for the targeted application either. In the conventional implementation, the power taken by a delay line is proportional to the switching frequency. This is because at higher frequencies a current source having large bias current is required to produce a small delay.

To allow the use of this programmable frequency controller in low-power supplies, which usually operate at high switching frequencies and have efficiency strongly dependent on the controller's power consumption, we developed a power efficient dual-bias delay cell, shown in Fig.5. It consists of a CMOS inverter and a dual current mirroring input stage that discharges equivalent capacitance seen at the node *a*. The propagation time of signal entering the cell is inversely proportional to the instantaneous current of the mirroring stage $i(t)_{mirrored}$. This current is formed as a scaled sum of current produced by two sources I_{coarse}, I_{fine} and during the delay cell transition period its value is:

$$i(t)_{mirrored} = I_{fine}/K_1 + I_{coarse}/K_2 \quad (2)$$

where $K_1 > K_2$.

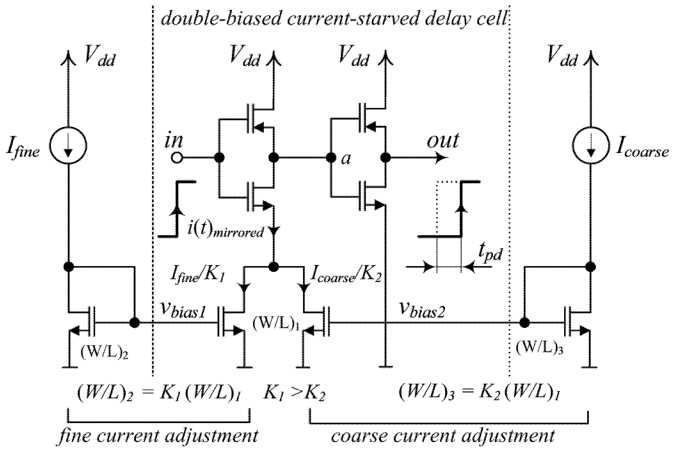

Fig.5. Dual-bias current starving cell.

In this way, the need for a single current source having a wide current range and high power consumption, at high switching frequencies, is eliminated. Still, a relatively high current $i(t)_{mirrored}$ ensuring short propagation time of delay cells can be achieved by setting I_{coarse} at a high value. When long propagation times are required, I_{coarse} can be reduced and a precise delay regulation can be achieved through I_{fine} adjustments. It should be noted that, in this application, $i(t)_{mirrored}$ has a relatively small influence on the delay line's power consumption. This is because $i(t)_{mirrored}$ occurs only during short delay-cell state transients, and in the targeted range of switching frequencies its average value is small. This structure also provides more accurate regulation of delay times. For large delays conventional current starved delay cells have poor regulation of delay times, due to inaccurate adjustment of low bias currents. In this case, this problem is minimized. Now, since the currents I_{coarse} and I_{fine} do not change over a wide range, precise adjustments of large delays can be achieved by reducing I_{coarse} and by varying I_{fine} only.

Current sources I_{coarse} and I_{fine} are digitally programmable and implemented as described in [9].

The delay matching control logic block is shown in Fig. 2. It compares the propagation time of $\delta(t)$ through 32 delay cells with the DPWM's clock period. If the clock period is larger the bias current of delay cells is decreased and if it is faster $i(t)_{mirrored}$ is increased.

IV. Experimental Results and IC Implementation

The MDPWM IC controller was implemented in a standard 0.18 μm process, using mixed-signal design approach. The largest portion of the circuit, taking more than 80% of silicon area is digital. It was constructed with automated design tools starting from Verilog code. The analog portion of the design includes input differential stages of ADCs, delay-lines both for ADCs and MDPWM and bias circuits for MDPWM. Fig.6 shows layout of the chip and Table I gives a summary of its main characteristics. It can be seen that it takes relatively small silicon area and has very low power consumption, comparable to the state of the art analog solutions.

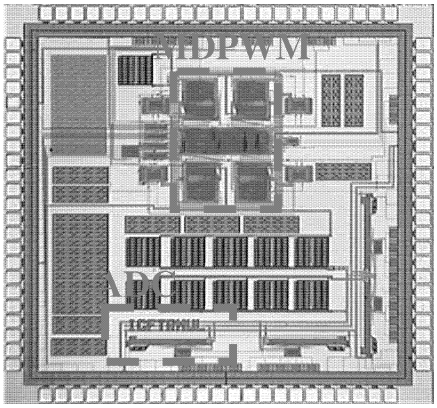

Fig. 6. Chip Layout of the controller IC

TABLE I

Important Chip Parameters

MDPWM	Frequency: 100KHz to 10 MHz Effective Resolution: 11-bits Hardware resolution: 8-bits Silicon area: 0.435 mm^2
ADC	Conversion time: 35 ns Quantization step : 20mV/10mV Silicon area: 0.052 mm^2
Current Consumption	1.8mA @ 10MHz (VDD=1.8V)

A. Power Consumption

Power consumption of the chip core is measured for switching frequencies ranging from 100 KHz to 10 MHz. The measured results are plotted in Fig. 7. The chip consumes only 1.8mA at 10 MHz switching frequency when all 4 phases are active and running.

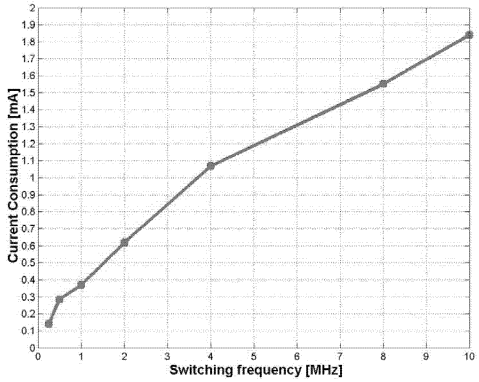

Fig.7. Chip current consumption vs. switching frequency

B. MDPWM Open Loop Test Results

Open loop tests of MDPWM's linearity and the range of switching frequencies are performed. To test the linearity

MDPWM is connected in an open loop to a buck converter, and duty ratio control signal $d[n]$ was gradually changed between 10 % and 90 % of its maximum value. The waveform shown in Fig. 8 demonstrates that the output voltage changes linearly. Non-linear, or even worse, non-monotonic regions cannot be observed.

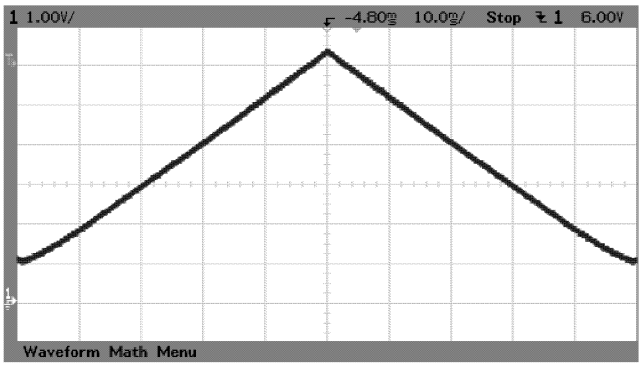

Fig. 8. MDPWM linearity test – Ch1: Output converter voltage (1V/div); Time scale is 10ms/div.

Fig. 9 shows operation over a wide range of switching frequencies. In this case, the duty ratio value is kept constant, and the clock frequency was changed between 1.2 MHz and 80 MHz to result in switching frequencies of 150 KHz and 10 MHz, respectively. It can be seen that the value of the duty ratio is maintained constant, and verification of automatic delay adjustment as well as operation at high switching frequencies is obtained.

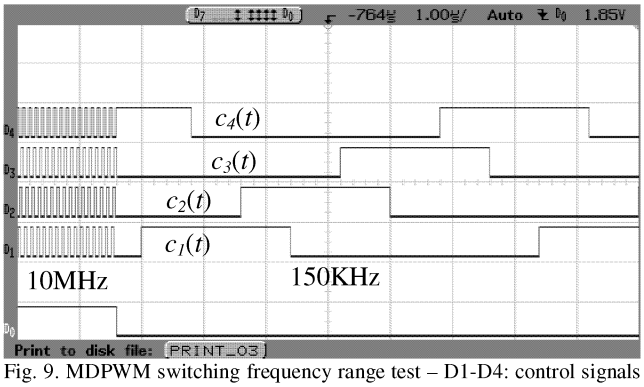

Fig. 9. MDPWM switching frequency range test – D1-D4: control signals switching; D0 – frequency step command. Time scale is 1μs/div.

C. Closed Loop Steady-State and Load Transient Test Results

The closed loop operation of the MDPWM controller IC is tested both for multiple-output and interleaved modes of operation. In the multiple-output mode, 4 buck converters operating at 1MHz are used to provide the following output voltages 1.2V, 1.8V, 2.5V and 3.3V. Fig. 10 presents the captured waveforms. All output voltages are well regulated at their designated values.

The load transient operation is verified in the interleaved MDPWM mode at 1MHz for a load change between 0.75A and 1.5A. The output voltage nominal value is 1.8V. As shown in Fig. 11, the controller exhibits fairly fast transient response.

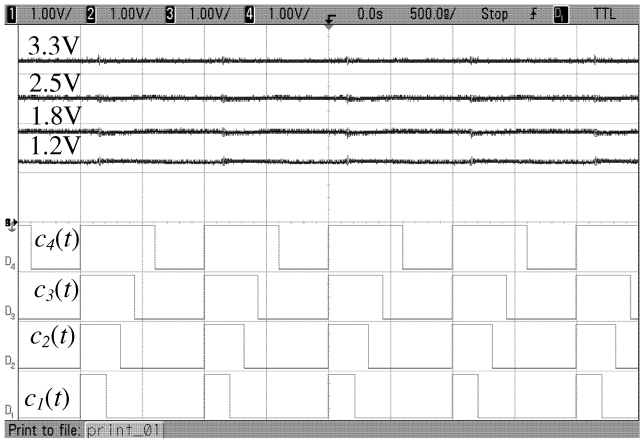

Fig. 10. Steady-state operation with 4 buck converters switching at 1MHz – Ch1,Ch2,Ch3,Ch4: Output converter voltage at 1.2, 1.8, 2.5, and 3.3V respectively (1V/div); D1-D4: MDPWM control signals switching at 1MHz; Time scale is 500ns/div.

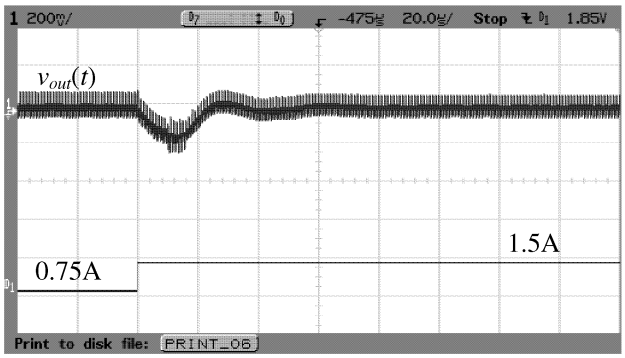

Fig. 11. Load transient response – Ch1 : output converter voltage - AC component (200mV/div); D1 – load step command. Time scale is 20μs/div.

C.1. Fault-Tolerant Operation and Interleaved Mode

The fault tolerant operation is tested by intentionally causing over current protection signal (OCP) in one of the phases, and consequent turning off the same phase as shown in Fig 12. The 4-phase interleaved buck converter (switching frequency is 1MHz) regulated at 1.8V is utilized for this test. Initially, all converter phases are running with control signals shifted by ¼ of the switching period. Once, phase 4 is turned off, the master

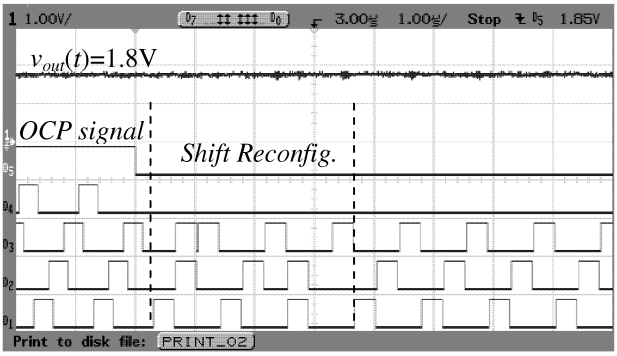

Fig. 12. Fault-tolerant operation in the interleaved mode – Ch1: Output converter voltage at 1.8 (1V/div); D1-D4: MDPWM control signals switching at 1MHz;D5 – OCP signal; Time scale is 1μs/div.

management unit observes the remaining number of phases and based on the pre-stored look-up table values starts refreshing phase angles for all active phases until they are set to their predefined phase angle values. In this way, after the reconfiguration is completed, the control signals are phase shifted by 1/3 of the switching period. Similarly, if one more phase is turned off, master management unit will adjust the phase shift to ½ of the switching period.

V. Conclusion

A universal multi-phase IC controller having low power consumption and high flexibility is presented. To achieve these characteristics, it utilizes the novel number-interpretation logic, delay-matching circuit based on a new design of current starved delay cell, and operation at a relatively low clock rate. The performance of the controller IC is experimentally verified on several experimental setups, including multiple-output and interleaved converters.

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