Sensorless Digital Peak Current Controller for Low-Power DC-DC SMPS Based on a Bi-Directional Delay Line

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***Abstract*— Peak current mode control is challenging to implement in integrated dc-dc converters for sub 1 W applications due to the need for an integrated high-bandwidth, low-noise current sensor. The analog sensor must typically consumes less than a few hundred micro-amps while amplifying the current through the high-side switch, which has frequency components extending into the ten's of MHz. Sensorless current mode control (SCM) eliminates the need for an explicit current sensor by reconstructing the inductor current from the system input/output voltages and the PWM signal pulse-width. In this work, a bi-directional delay line based digital SCM scheme is proposed. The inductor current is mapped onto the bi-directional delay line whose propagation delay tracks the inductor current slopes. An integrated digital current observer designed in a 0.18 μm CMOS process is compared to a benchmark analog current sensor operating at 2 MHz and fabricated in the same process. The digital current observer consumes 168 μA, or 20% less then the benchmark at I_{out} = 100 mA, while avoiding signal-to-noise degradation at light loads. A prototype of the digital current sensor operating at 1 MHz is demonstrated on a CPLD platform.**

I. Introduction

Low-power, sub 1W switch-mode power supplies (SMPS) rarely employ peak current program mode control (CPM) [1], mainly because of the need for a high bandwidth current sensor. This analog sensor significantly increases the total current consumption of the controller and reduces the overall system efficiency. Compared to voltage mode control, CPM offers inherent peak current protection, reduced audio susceptibility and simplifies the implementation of the voltage loop compensator. One possible architecture for mixed-signal CPM [2], [3] is shown in Fig. 1(a). A flexible digital compensator is used in the voltage loop to regulate $v_{out}(t)$ based on the quantized error $e[n]$ and the analog reference voltage V_{ref}. A DAC converts the digital current command $i_c[n]$ from the compensator into an analog voltage $v_c(t)$. A high-speed analog comparator generates the *reset* pulse for the SR-latch based on the sensed current through M_1, $V_{sense}(t)$. A $\Delta\Sigma$ DAC architecture with adaptive sampling rate was discussed in [3] for this architecture.

The high gain-bandwidth required in the current sensor for today's sub-1W converters implies that CPM cannot compete with the state-of-the-art micro-watt voltage-mode controllers [4]. In addition, the current sensing amplifiers have a limited dynamic range due to signal-to-noise ratio degradation at light loads, and, in some cases, cannot operate with low duty ratios due to the need for a leading edge blanking circuit.

This work was supported by NSERC and U of T Open Fellowship.

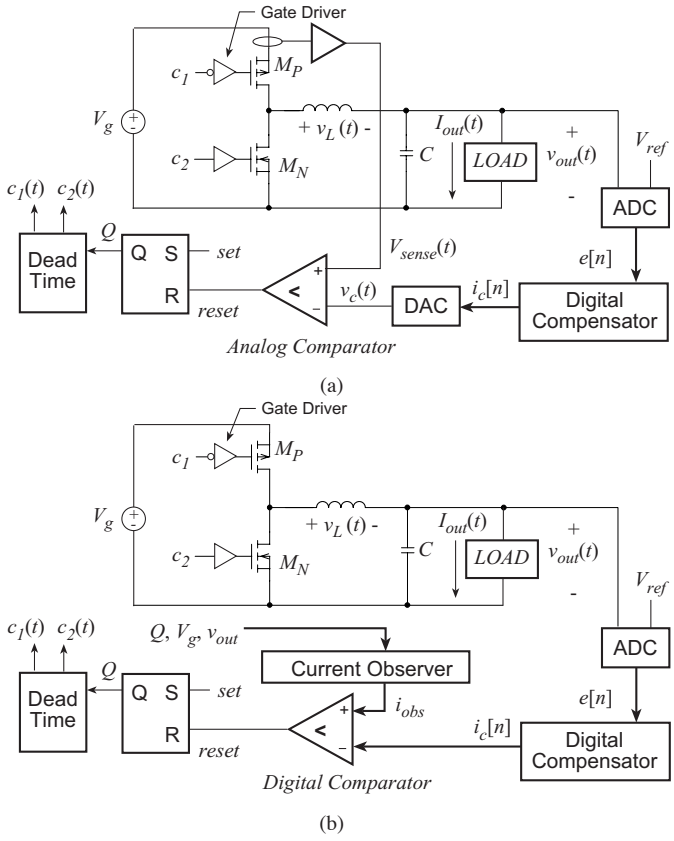


Fig. 1. Conceptual architecture of a buck converter operating in (a) mixed-signal CPM with a current sensor and (b) sensorless CPM as presented in this work.

An observer-based CPM controller was demonstrated in [5] to eliminate the need for an explicit current sensor. In this sensorless current mode control (SCM) method, the inductor current is artificially reconstructed by integrating the time varying inductor voltage $v_L(t)$ using analog circuitry. This method is not the most suitable for monolithic integration with digital systems implemented in the latest CMOS technologies. The low supply voltage of the modern digital ICs

severely limits the possibility for the realization of the analog components used in the existing SCM method [5]. In this work, the primary objective is to demonstrate a digital SCM controller architecture suitable for low-power dc-dc SMPS, as shown in Fig. 1(b). The main feature of the new architecture is that the need for analog circuitry in both the current and voltage feedback loops is virtually eliminated. A novel current observer provides a digital representation of the instantaneous current in M_1, i_{obs}. The digital nature of both i_{obs} and $i_c[n]$ allows the high-speed analog comparator to be eliminated. The waveforms associated with the architecture of Fig. 1(b) are shown in Fig. 2.

The digital SCM control method introduced in this work is compatible with efficient monolithic implementation in modern CMOS processes. In addition, it is significantly simpler and more power efficient than the existing state-of-the-art digital current-mode solutions [6], [7] that rely on relatively complex digital signal processing to achieve superior transient response.

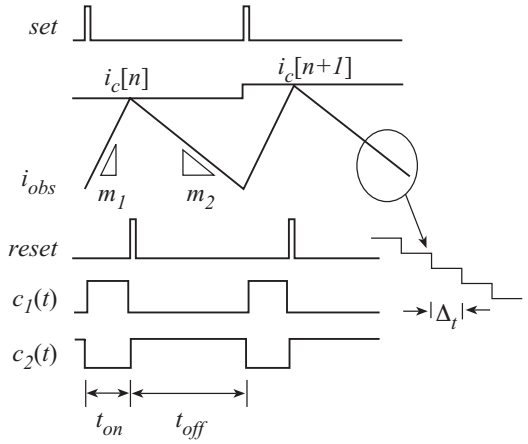


Fig. 2. Switching waveforms for SCM.

II. Digital Sensorless Current Mode Control

A. Digital Observer-based Control

The most intuitive method of implementing the digital current-loop module is shown in Fig. 3. This architecture is essentially a digital equivalent of the existing analog SCM control scheme [5]. The inductor voltage is integrated in the digital domain using a counter that counts up during t_{on} (Q=1) and down during t_{off} (Q=0). A combination of a delay control circuit and a voltage controlled oscillator (VCO) are used to control the frequency of the counter's clock. In this way, the counter output tracks $i_L(t)$ since the clock frequency varies according to slope of $i_L(t)$; m_1 and m_2 during t_{on} and t_{off} respectively. The proper delay ratio is achieved inside the calibrated delay control block that sets $V_{cntrl}(t)$. The inductor slopes m_1 and m_2 are given in Table I for several non-isolated topologies commonly used for portable applications. Despite its simplicity, this architecture does not scale favorably to multi-MHz switching frequencies since the VCO frequency must be at least two orders of magnitude higher than f_s to achieve tight regulation and avoid limit cycle oscillations.

TABLE I
Inductor Current Slopes for Common DC-DC Topologies

Topology	m_1	m_2
Buck	$(V_g - v_{out})/L$	$-v_{out}/L$
Boost	V_g/L	$-(v_{out} - V_g)/L$
Non-Inverting Buck-Boost	V_g/L	$-v_{out}/L$

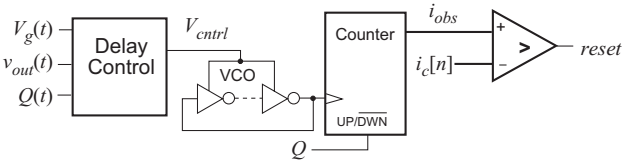


Fig. 3. Digital current-loop module using a VCO/counter-based current observer.

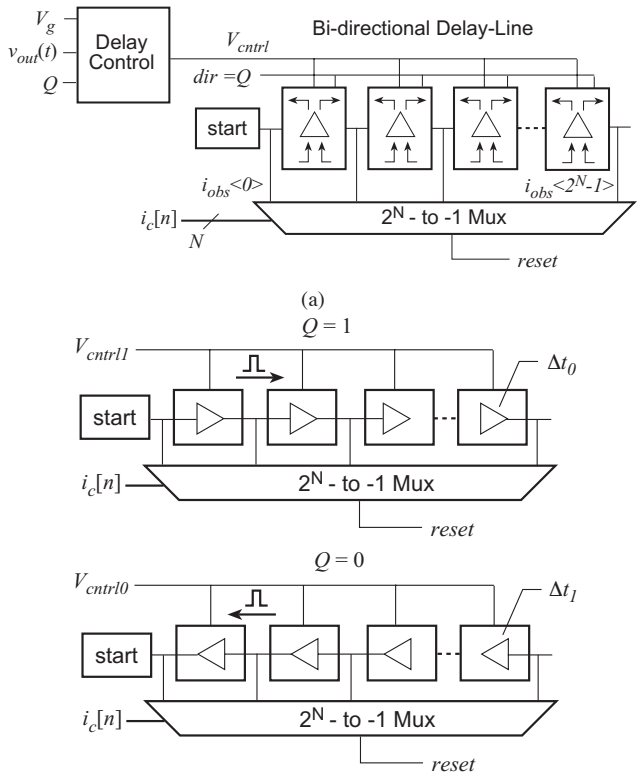
An alternate architecture for the digital current-loop module that does not require a high frequency clock is shown in Fig. 4(a). A single pulse travels to the right (Q = 1) with a propagation speed proportional to m_1, until the observed current reaches the output of the N-bit voltage loop current command $i_c[n]$ and the SR latch is reset by the 2^N-to-1 multiplexer output. At the instant when the latch is reset (Q = 0), the delay line direction and control voltage V_{cntrl} are switched inside the delay control block, causing the pulse to propagate in the opposite direction with a speed proportional to m_2. The delay-line configuration for each value of Q is shown in Fig. 4(b). The inductor current is therefore mapped directly onto the delay line outputs in real-time, without requiring a high frequency clock or a power hungry current sensor. In addition, the digital comparator of Fig. 1(b) is implemented using the 2^N-to-1 multiplexer.

One limitation of the SCM architecture of Fig. 4(a) is the need for a lengthy delay line that can accommodate the entire range of the instantaneous inductor current, as illustrated in Fig. 5(a). The 2^N-bit delay line output i'_{obs} is an encoded representation of $i_L(t)$, which ranges from $i_{L,min}$ to $i_{L,max}$. The quantization interval of $i_L(t)$ is therefore given by:

$$\Delta i_{obs} = \frac{i_{L,max} - i_{L,min}}{2^N} \tag{1}$$

If i_{obs} saturates to zero due to insufficient head-room in the delay line when $i_L(t)$ drops, the observer will incorrectly predict that the inductor current is discontinuous. Under this condition, the controller ceases to operate in current-mode and the observer behaves like a classical delay line digital pulse width modulator (DPWM) with voltage feed-forward [8], since the pulse will always be injected from the same starting point. When operating in closed loop, the change in inductor current that results from a change in the LSB of the current command $i_c[n]$ can be estimated using Fig. 5(b). A 1 LSB change in $i_c[n]$ will delay the *reset* pulse by $\Delta t_1 \propto 1/(V_g - V_{out})$. The resulting change in the inductor current is given by (2) for a buck converter:

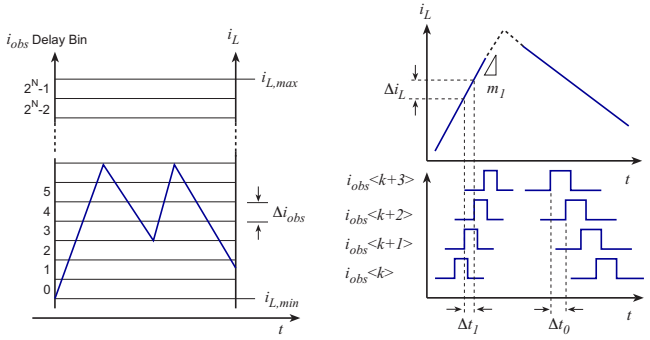
$$\Delta i_L = m_1 \Delta t_1 = (V_g - v_{out})\Delta t_1 / L \tag{2}$$



(a)

(b)

Fig. 4. (a) Current observer using a bi-directional delay line. (b) Delay line configuration for *dir* = 1 and *dir* = 0.



(a) (b)

Fig. 5. (a) Mapping of the inductor current onto the delay line. (c) Illustration of the current loop gain from Δt_1 to Δi_L.

B. Hybrid SCM Current Observer

The hybrid combination of a counter and a delay line, which was proposed for a voltage mode DPWM [9], [10], can also be applied to the delay line current observer. This approach reduces the total number of delay elements for a given resolution of $i_c[n]$, as dictated by limit-cycle and output regulation requirements. The hybrid architecture adapted for this work is shown in Fig. 6 . Each bi-directional delay element contains two multiplexers, one S-R latch and a delay cell having an externally adjustable delay, as explained in the following section. The delay line has j elements and is wrapped. The final delay cell's output is used to clock the counter. The startup/saturation circuitry is omitted for the sake of clarity. The saturation block is used to stop the pulse when i_{obs} reaches either 0 or 2^N.

The *count* is incremented by the last delay cell while the inductor current rises (*dir* = 1) and decremented while the inductor current falls (*dir* = 0). The *reset* pulse is generated once *count* reaches $i_c < N-1 : j >$ and the pulse reaches the delay cell selected by $i_c < j-1 : 0 >$.

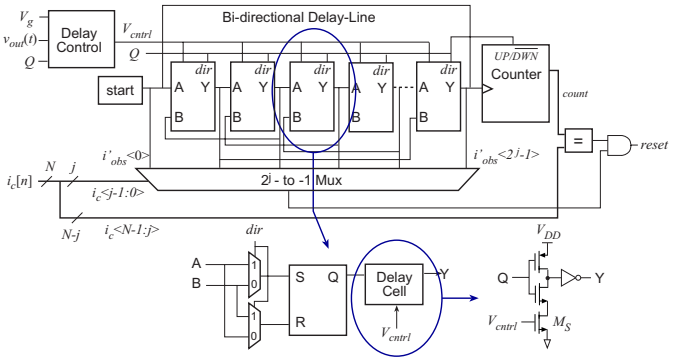


Fig. 6. Simplified architecture for the hybrid delay line/counter current observer.

C. Delay Control Block

The delay control voltage V_{cntrl} is set to V_{cntrl1} and V_{cntrl0} for Q = 1 and Q = 0 respectively. The delay control circuit suitable for a buck converter topology is shown in Fig. 7. The inductor slopes for the buck topology are given in Table I as $m_1 = (V_g - v_{out})/L$ and $m_2 = -v_{out}/L$.

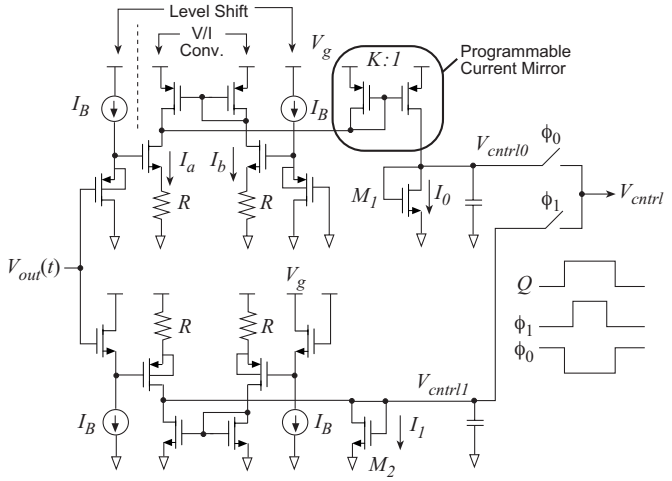


Fig. 7. Control circuit for the SCM intended for a buck topology.

The delay cell shown in Fig.6 consists of a current-starved inverter, where the discharge current and propagation delay are set by M_S through V_{cntrl}. The delay control block was adapted from [11], where an offset-free V/I converter was used for slope compensation. Transistors M_1 and M_2 in Fig. 7 are used to form a current mirror with M_S in the delay cell. Two non-overlapping clocks ϕ_0 and ϕ_1 are used to connect V_{cntrl} to either V_{cntrl0} or V_{cntrl1} depending on the state of Q. A

combination of a level shifter and V/I converter is used to generate the required current I_0, which is set by the difference of the current in the two V/I converter legs:

$$I_a = \frac{v_{out}(t) + V_{sg,P} - V_{gs,N}}{R} \quad (3)$$

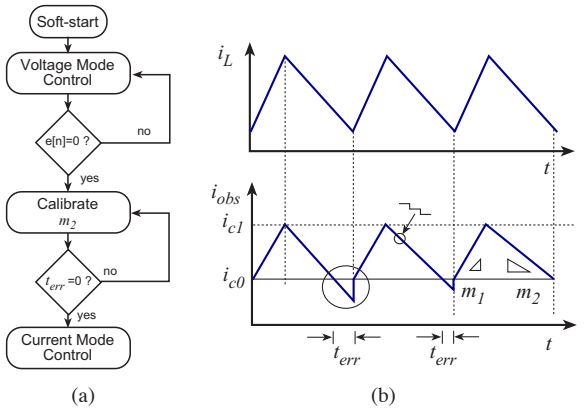
$$I_b = \frac{V_{sg,P} - V_{gs,N}}{R} \quad (4)$$

$$I_0 = \frac{I_a - I_b}{K} = \frac{v_{out}(t)}{KR} \propto m_2 \quad (5)$$

Similarly, the current in M_2 is given by;

$$I_1 = \frac{V_g - v_{out}(t)}{R} \propto m_1 \quad (6)$$

The power dissipation in this simple delay control block is dominated by the four resistors in the V/I converters.



(a) (b)

Fig. 8. (a) Flow chart and (b) ideal waveforms during calibration of the observer slopes. The calibration is complete when the pulse travels back to the injection point at the end of the switching cycle

D. Calibrating the Observer Slopes

One limitation of SCM is the sensitivity to mismatch between the observed and actual inductor current slopes. The most important source of mismatch is the non-linearity of the voltage-to-delay conversion within the delay control block of Fig. 7. In addition, the actual inductor current waveform typically has a significant curvature due to parasitic series resistance and magnetic-related non-idealities. Body-diode conduction, R_{ds-on} variations as well timing delays in the gate-drivers also contribute to significant errors in i_{obs}.

If the m_1/m_2 ratio is not accurately implemented by the observer, the error between i_{obs} and $i_L(t)$ will grow every switching cycle due to the integral nature of the current observer. This leads to eventual saturation of $i_c[n]$ due to the finite range imposed by the digital hardware. Unlike the digital SCM scheme demonstrated in this paper, analog SCM [5] is especially sensitive to mismatches since there is no quantization of the observed current and therefore even the slightest mismatch in m_1/m_2 will eventually cause saturation. Any practical implementation of either analog or digital SCM therefore requires a slope calibration mechanism. One such calibration scheme is illustrated in Fig. 8(a) and can be explained as follows. During startup and calibration, the system is made to operate in voltage-mode control by simply injecting the pulse into the same delay cell of the delay line each cycle. Under this condition, the current observer effectively behaves as a digital DPWM. After bringing the converter into steady-state (where $e[n]$=0), calibration is initiated by examining the timing of the returning pulse in order to calibrate the return slope m_2. The calibration of m_2 is achieved by digitally adjusting the current mirror ratio in Fig. 7(b) to control K in (5) until the pulse returns to the original injection point by the end of the switching cycle, as shown in Fig. 8(b).

III. Benchmark: Analog Current Sensor and Comparator

The current sensor and high-speed comparator of Fig. 1(a) and presented in this section were fabricated in the same 0.18 μm CMOS technology as targeted for the sensorless current observer. These blocks are replaced by the SCM scheme presented in Fig. 1(b) and hence the performance of these blocks will be used as a benchmark since there is a lack of controller power consumption data in publications having low-power integrated current sensors [11].

A. Monolithic SenseFET

The circuit used as the benchmark on-chip current sensor is shown in Fig. 9. The CMOS topology is based on the architecture demonstrated in [11]. The sensing transistor M_1, or SenseFET [12] is embedded in the layout of the high-side power transistor and forms a current mirror with M_P. Using this current mirror, the sensed current $I_1 = I_P/K$ is converted into a voltage by the sense resistor R_{sense}. The sensing ratio K_s is therefore given by:

$$K_s = \frac{V_{sense}(t)}{I_P(t)} = \frac{R_{sense}}{K} \quad (7)$$

A sensing gain of K_s = 1.28 Ω (2.1 dB) is achieved using K = 1170 and R_{sense} = 1.5 kΩ. The maximum value of K, which determines the current overhead, is constrained by matching requirements. Accurate current mirroring from M_P to M_1 is achieved by forcing the drain of M_1, V_y to equal the drain voltage of M_P, V_x when M_P is *on*. This condition is enforced by the high-bandwidth amplifier and the voltage sampling circuit consisting of M_2, M_3 and C_1. The minimum duty cycle is limited by the response time $V_{sense}(t)$ following the turn-on of M_P. The transistors M_4 and M_5 are used to maintain a minimum bias current through M_1 when M_P is off. The internally compensated amplifier has a folded cascode topology and uses the 5 V compatible transistors in the 0.18 μm CMOS process. The simulated closed-loop sensing response $H_{sense}(j\omega) = V_{sense}/I_P$ is shown in Fig. 10. The closed-loop 3 dB bandwidth ranges from 25.5 MHz at V_g = 2.7 V to 17.9 MHz at V_g = 4.2 V, making this current sensor suitable for switching frequencies up to 5 MHz, based on system-level simulations.

B. Analog Comparator

The analog continuous-time comparator used in the benchmark CPM design is shown in Fig. 11. The cross-coupled transistors M_1 and M_2 are used to increase the comparator

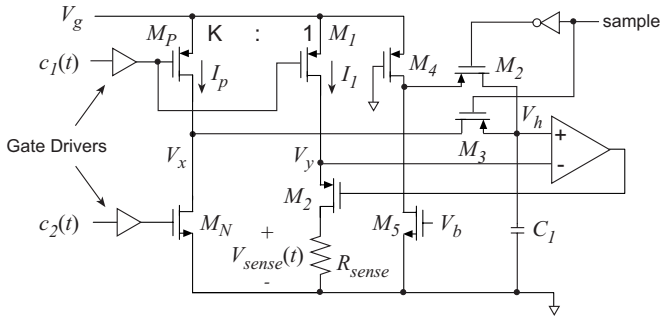


Fig. 9. CMOS monolithic senseFET current sensor.

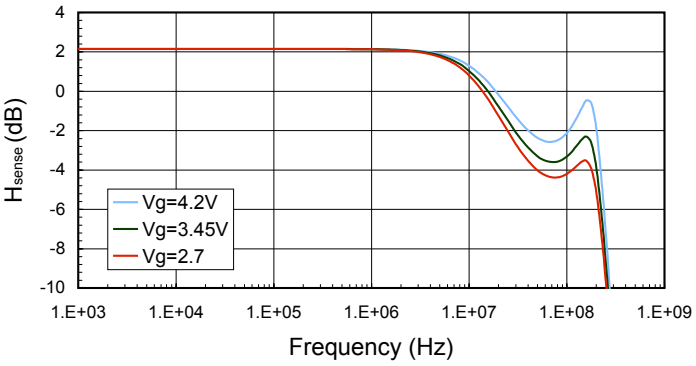


Fig. 10. Closed-loop frequency response of the benchmark current sensor for 2.7 V $< V_g <$ 4.2 V.

switching speed when the differential input voltage changes polarity. Three cascaded inverters are used to-regenerate a rail-to-rail output. A p-channel differential pair is used in the input stage to allow a low common-mode voltage on the sense voltage node $V_{sense}(t)$. During steady-state, the comparator's negative input $in-$ is connected to the steady-state $v_c(t)$ from the compensator, while $in+$ is connected to the sense current $V_{sense}(t)$. The comparator delay is heavily dependent on the slope of $V_{sense}(t)$ during t_{on}. The voltage slope is obtained from (7) and given by (8) for a buck converter:

$$m_v = K_s m_1 = \frac{(V_g - V_{out})R_{sense}}{LK} \tag{8}$$

The simulated comparator delay ranges from 6.2 ns and 13.8 ns for SR = 2 V/μs and SR = 0.1 V/μs respectively. The total current consumption for the comparator is 59.4 μA from the internal 1.8 V supply, for a switching frequency of f_s = 2 MHz.

IV. Simulation Results

The hybrid current observer described in Section II was designed in a 0.18 μm CMOS process to evaluate the feasibility of the digital SCM technique. The circuit was designed to operate at f_s = 2 MHz, with 2.7 V $< V_g <$ 4.2 V, V_{out} = 1.5 V and L = 2 μH. The delay line of Fig. 6 has 32 elements (5-bits) and a 4-bit counter, for a total of N = 9 bits. The simulated delay-cell propagation delay versus V_{out} at V_g = 4.2 V is shown in Fig. 12(a) for the two propagation directions

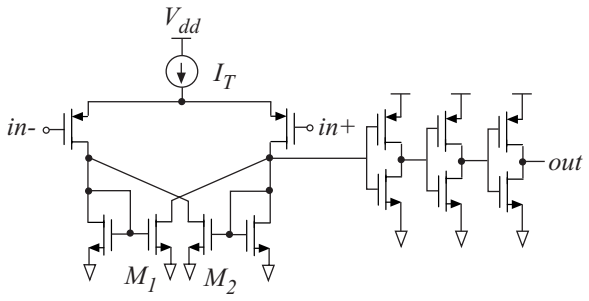


Fig. 11. CMOS High-speed analog comparator.

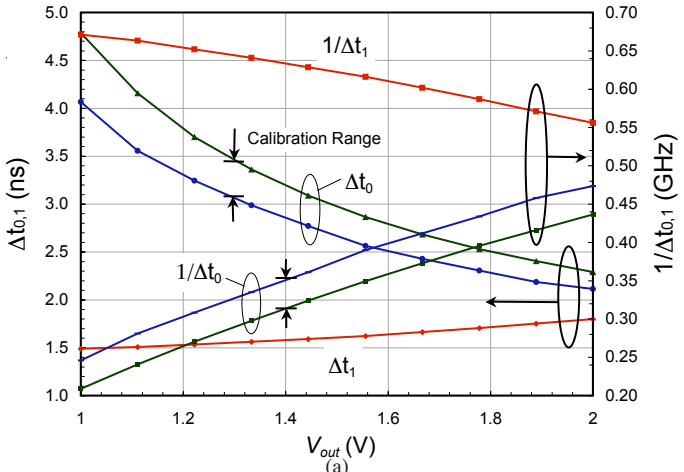
(Δt_1 for Q = 1 and Δt_0 for Q = 0). This simulation shows the linearity of $1/\Delta t_{0,1}$ versus V_{out} for the delay control circuit of Fig. 7, in addition to the calibration range of Δt_0. A transistor-level simulation of the system is shown in Fig. 12(b) for a step in $i_c[n]$ from 225 to 275. The delay cell, counter and $Q(t)$ outputs are shown at the top, while the corresponding value of i_{obs} is shown in the bottom trace. The i_{obs} tracks the inductor current, which is shown in the middle trace.

V. Experimental Results

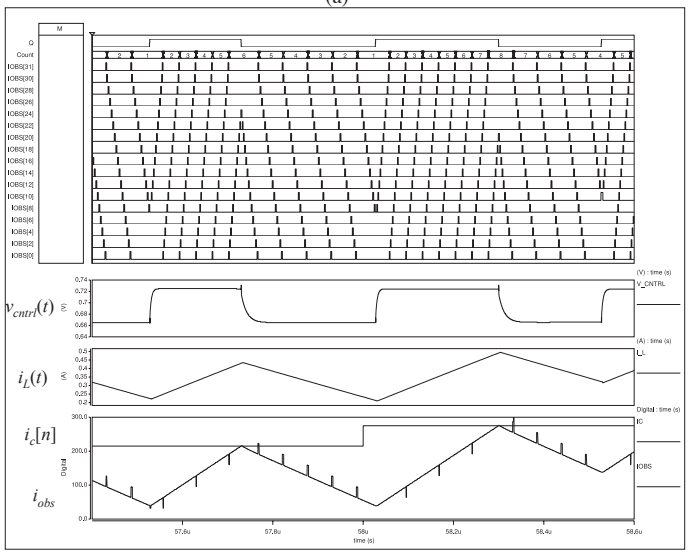
A. Sensorless Current Mode Prototype

An experimental 1 W dc-dc converter operating at f_s = 1 MHz was built to demonstrate the digital SCM concept of Fig. 6 using off-the-shelf components. The non-inverting buck-boost topology was used for the prototype due to it's convenient inductor current slope ratio of $m_1/m_2 = -V_g/V_{out}$. This simple ratio allows the delay control circuit to be easily implemented using off-the-shelf components during the proof-of-concept phase. The bi-directional hybrid delay line current observer was created using a dedicated CPLD IC whose supply voltage is modulated by a 2 Ω analog SPDT switch to achieve the variable propagation speed. The corresponding delay control circuit is shown in Fig. 13.

The measured variation in Δt_1 and Δt_0 for the experimental current observer is shown in Fig. 14. The LSB delay can be controlled from 3.78 ns to 6.65 ns over a 550 mV operating range, which sets the maximum m_1/m_2 ratio to 1.76. Neglecting the converter losses, this in turn limits the DC-conversion ratio to $\approx M = V_{out}/V_g = D/D' > 1.76$ and hence $D > 0.36$ for the buck-boost converter. In this case the duty ratio is limited to $0.36 < D < 0.5$ due to the lack of slope compensation in the experimental setup. The experimental waveforms in Fig. 15(a) and (b) show the converter operating in closed loop with V_{out} = 1.6 V and V_g = 2.7 V. The delay line supply voltage is properly modulated by $Q(t)$ and the pulse is slowed down in the reverse direction, as evidenced by the wider spacing of Δt_2 compared to Δt_1. The counter output cycles between 8 (*4'b1000*) and 6 (*4'b0110*) as the pulse follows the inductor current. This demonstrates that the current observer does not saturate and the $\Delta t_1/\Delta t_2$ delay ratio matches the ratio of the inductor current slopes m_2/m_1. Six out of the 32 delay outputs are shown explicitly in Fig. 15(b).



(a)



(b)

Fig. 12. (a) Simulated delays Δt_1 and Δt_0 versus V_{out} for the digital current observer. (b) Transistor level transient simulation of the full system for a step change in $i_c[n]$.

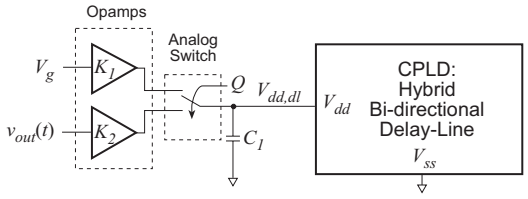


Fig. 13. Delay control circuit for the experimental system.

B. Benchmark: SenseFET Current Sensing Scheme

A partial chip micrograph of the fabricated IC containing the benchmark current sensing scheme is shown in Fig. 16. The IC was fabricated in a 0.18 μm CMOS process where 5V thick oxide transistors are available for the output stage and the current sensing circuit of Fig. 9. The IC includes an output stage with a measured pin-to-pin on-resistance of of 290 mΩ (nMOS) and 338 mΩ (pMOS) at V_g = 4.2 V. The active area for the current sensing circuit and high-speed comparator

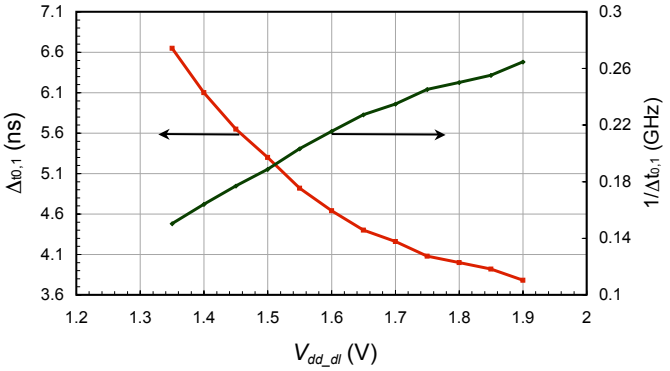
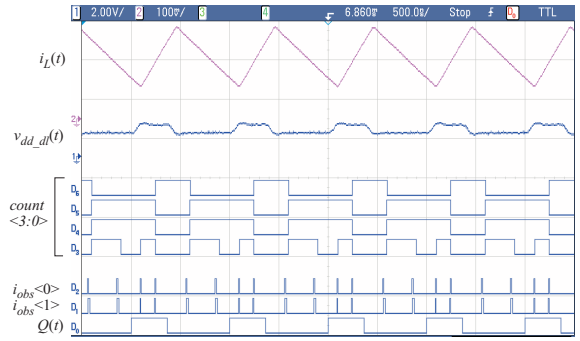
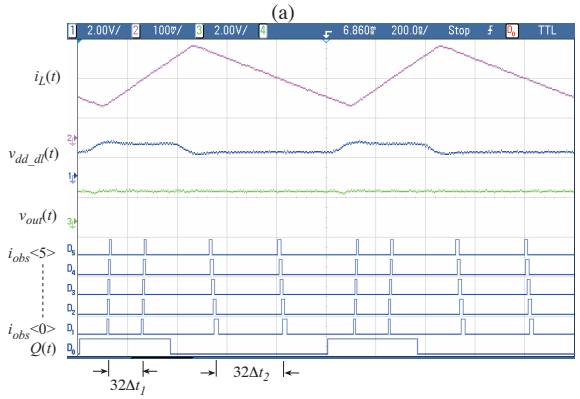


Fig. 14. Measured propagation delay versus supply voltage for the experimental delay line.



(a)



(b)

Fig. 15. (a) Steady-state waveforms for the buck-boost converter operating in closed-loop with V_{out} = 1.6 V, V_g = 2.7 V. Ch-1: $v_{dd,dl}(t)$, 2V/div, Ch-2: $i_L(t)$, 100 mA/div. (b) Same operating point as (a) with $V_{out}(t)$ and $i_{obs} < 5 : 0 >$ included.

are 0.003348 mm^2 and 0.001026 mm^2 respectively. Steady-state waveforms for the current sensor operating at 2 MHz are shown in Fig. 17.

VI. Comparison of Sensing Schemes and Discussion

A brief comparison of the digital SCM design outlined in Section II and the fabricated benchmark analog current sensor is given in Table II. The transistor count is increased by 50$\times$ for digital SCM compared to the benchmark, while the actual silicon area increase is expected to be much lower due to the digital nature of the SCM. The current consumption in the benchmark sensor scales with the load current I_{out}

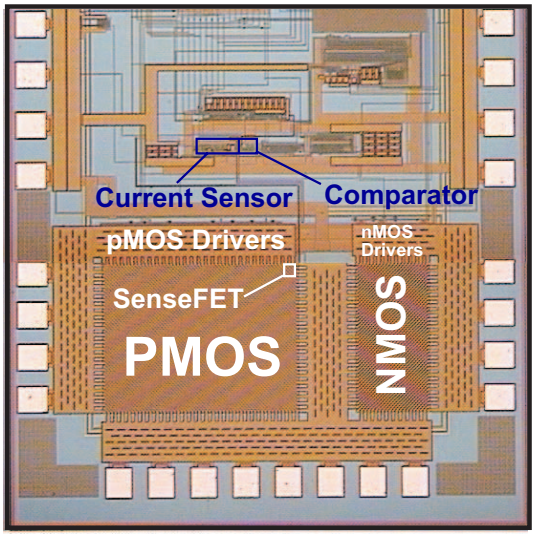
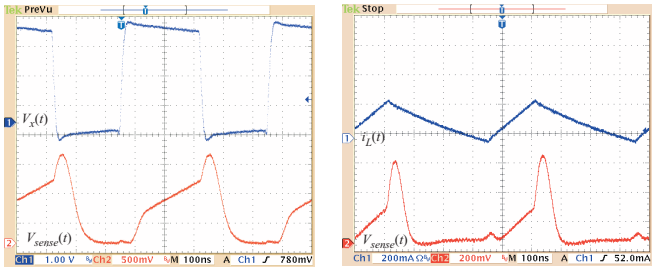


Fig. 16. Partial chip micrograph of the benchmark IC, which contains the monolithic senseFET-based current sensor and output stage.



(a) (b)

Fig. 17. (a) Steady-state waveforms for the integrated analog current sensor with V_g = 4.2 V, f_s = 2 MHz. Ch-1: $V_x(t)$, 1 V/div, Ch-2: $V_{sense}(t)$, 500 mA/div. (b) SenseFET circuit operating at I_{out} = 125 mA. Ch-1: $i_L(t)$, 200 mA/div, Ch-2: $V_{sense}(t)$, 200 mV/div.

due to I_1 in Fig. 9. The total senseFET current consumption varies with the average current in the senseFET transistor $< I_1 >=< I_P > /K$. At I_{out} = 100 mA and f_s = 2 MHz, V_g = 4.2 V, V_{out} = 1.5 V and L = 2 μH, the digital SCM sensor draws a fixed 168 μA (60 μA in the delay-line) irrespective of the load current, compared to 59+112+$< I_1 >$= 209.1 μA for the benchmark, which represents a reduction of 20%. In general, while the benchmark SenseFET provides a compact on-chip sensing solution for low frequencies, it is very challenging to scale beyond switching frequencies of 5 MHz while maintaining reasonable current consumption due to the high precision and high bandwidth requirements of the analog circuitry that operates in closed-loop. In addition, the wasted current in the SenseFET branch reduces the light-load efficiency. The digital SCM technique described in this work requires only simple/conventional analog circuitry operating in open-loop in the bias stage, while the majority of the functionality is achieved using standard digital gates. Unlike the benchmark analog current sensors, the digital SCM scheme does not suffer from reduced signal-to-noise ratio at light loads, while it does requires periodic calibration.

TABLE II

BASIC COMPARISON FOR THE CURRENT SENSING SCHEMES

	Benchmark Analog		**Digital SCM Sensor**	Units
	Comparator	SenseFET		
CMOS Process	0.18 μm		0.18 μm	
Frequency f_s	2		2	MHz
Supply Voltages	1.8	2.7-4.2	1.8, 2.7-4.2	V
Transistor Count	20	30	2490	
Current Consumption	59	112 + $< I_P > /K$	168	μA
Key Specifications	t_d=3.2ns (@2V/μs)	K_s=1.28Ω f_{3dB}=26MHz	9 bits Δt_1=1.6ns	

VII. CONCLUSION

A novel sensorless digital current program mode controller architecture suitable for low-power dc-dc converters and monolithic integration with digital hardware was introduced. The key element of the controller is a bi-directional delay line that is used for inductor current estimation. The digital SCM scheme has a comparable current consumption at 2 MHz while eliminating the need for a high bandwidth amplifier and a fast comparator required in traditional peak current mode control schemes.

ACKNOWLEDGMENT

The authors would like to thank the Canadian Microelectronics Corporation (CMC), NSERC and Fuji Electric Advanced Technology Co. Ltd for their valuable support.

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