Non-Zero Error Method for Improving Output Voltage Regulation of Low-Resolution Digital Controllers for SMPS

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Abstract- **A simple method for achieving tight output voltage regulation in digitally controlled low-power dc-dc switch-mode power supplies with low-resolution digital pulse-width modulators (DPWM) is introduced. By utilizing a non-zero scheme for coding the output voltage error, an inherent quasi sigma-delta modulation effect improving effective DPWM resolution is obtained. The effectiveness of the method is experimentally verified on a 400 kHz, 5 V to 1.8 V, 5 W digitally-controlled buck converter. Using a 6-bit DPWM and the new coding scheme only, undesirable low-frequency limit-cycle oscillations (LCO), existing in conventional designs, are eliminated and tight output voltage regulation obtained.**

I. INTRODUCTION

Digital controllers for dc-dc low-power switched-mode power supplies (SMPS) used in battery powered devices, computers and consumer electronics have been attracting increasing interest over recent years. This is mostly due to numerous features they offer, including multi-mode operation, self-calibration, and design portability. However, compared to analog controllers, the existing digital systems still have significant disadvantages regarding the accuracy of the output voltage regulation. In voltage mode pulse-width modulation controllers, as the one shown in Fig. 1, the problems are caused by the quantization effects introduced by the analog-to-digital converter (ADC) and digital pulse-width modulator (DPWM).

Insufficient resolution of the DPWM, compared to that of the ADC, usually causes limit-cycle oscillations (LCO) of the output voltage [1]-[2] that compromise the voltage regulation. To minimize the LCO, in conventional controllers the resolution of the DPWM is increased so that the minimal increment of the output voltage due to the DPWM's quantization effect is smaller than the zero-error bin. The zero error bin is the quantization step of the ADC around the voltage reference, V_{ref} that is coded as zero error, i.e. e[n]=0. As shown in [1]-[2] the minimal resolution of the DPWM that results in no-LCO condition also depends on the converter topology, input and output voltage values as well as on the gain of the PID compensator at the frequency of oscillations. In modern high-frequency SMPS providing very low regulated voltages and tight regulation a very high resolution of the DPWM, often exceeding 12 bits, is required. The design of such a DPWM is a serious challenge [3]. Their complexity, silicon area needed for the implementation, and power consumption often make the digital controllers unsuitable for numerous cost-sensitive low-power applications.

To improve the resolution of the DPWM, dithering and Σ-Δ structures have been proposed [3]-[7]. In those systems the effective resolution of the DPWM is improved by specialized circuits that change the duty ratio over several switching cycles. As a result an average duty ratio value with the resolution higher than that of the original DPWM is obtained [3]–[7]. The averaging is automatically performed by *L* and *C*, the power stage filter components [3].

The main drawback of this approach is that the dithering and 1st order Σ-Δ modulators create low-frequency noise, also known as tones, negatively affecting output voltage regulation. To eliminate the noise, higher orders Σ-Δ structures that push the tones beyond the corner frequency of the filter can be used [7], but their implementation requires additional digital logic. In addition, in all of these structures, the size and complexity of the PID compensator, which depend on the number of bits used to represent duty ratio control value $d[n]$, remain as high as in non-dithering implementations.

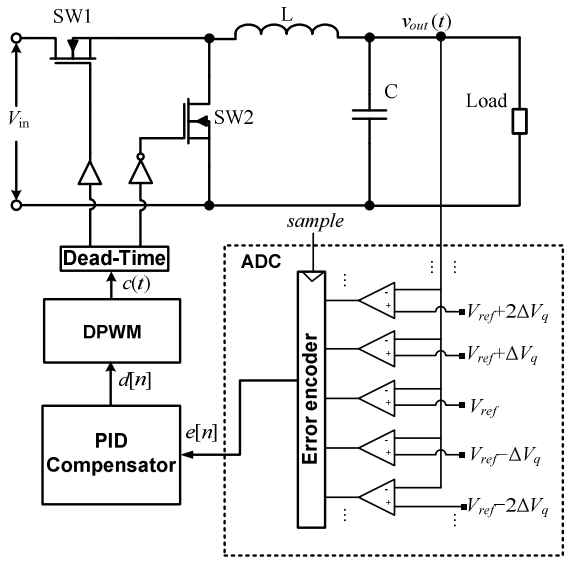

Fig. 1. A digitally controlled SMPS

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Moreover, even with the DPWM resolution sufficiently high for meeting the no-LCO conditions [1]-[2], LCO could still happen in practice [8]. The zero-error bin practically introduces a dead-zone in the feedback loop and causes open loop operation while the output voltage is inside the bin. As a consequence, the controller can start switching periodically between "open loop" and closed loop modes and a low frequency limit cycling can occur. These oscillations, caused by periodic excursions of the voltage outside the bin, usually happen at a frequency lower than the output stage corner frequency and cause significant disturbance of the output voltage.

In this paper, a very simple approach that provides tight output voltage regulation with a low-cost low-resolution DPWM and does not require any additional hardware is shown. In the digital controller of Fig. 1, a quasi Σ-Δ modulation effect is obtained by simply changing the way the digital equivalents of the error signal $e[n]$, produced by the ADC, are represented. Unlike in conventional controllers, the ADC never produces zero error causing high frequency oscillations of the DPWM's control variable $d[n]$, which improves effective DPWM resolution and consequently, output voltage regulation. The new coding scheme also allows the use of a simple PID producing $d[n]$ with the resolution equal to that of the simple DPWM.

In the following section the new non-zero error bin coding scheme and the principle of operation of the controller are described. In Section III we give guidelines for the design of the PID compensator and selection of the coder parameters. Section IV shows simulations and results obtained with an experimental prototype that verify the method's usefulness.

II. Non-Zero Error Coding Scheme And System Operation

The input-to-output characteristics of a conventional and a non-zero ADCs are shown in Fig. 2. It can be seen that in the system with the modified coding the zero-error bin is replaced with an ideal relay whose threshold, i.e. transition point, is at the voltage reference V_{ref}. The values of the analog input $v_{out}(t)$ (see Fig.1) in the close proximity of the threshold result in a digital error of amplitude δ, where, as described later, the amplitude is a design parameter for adjusting the voltage regulation. All other characteristics of the ADCs are practically the same. Both of them have equally-sized input voltage quantization steps ΔV_q, and the difference between the coded error steps for larger input voltage variations is the same.

This modification makes the controller behave similar to a relay, or quasi-stable system, experiencing limit cycle oscillations of the control variable $d[n]$ in steady state. If the frequency of these oscillations is significantly higher than the power stage corner frequency $f_0 = 1/(2\pi\sqrt{LC})$ they get attenuated and do not affect the output voltage but do improve output voltage regulation by eliminating the low-frequency LCO caused by zero-error bin. This is because of the PID

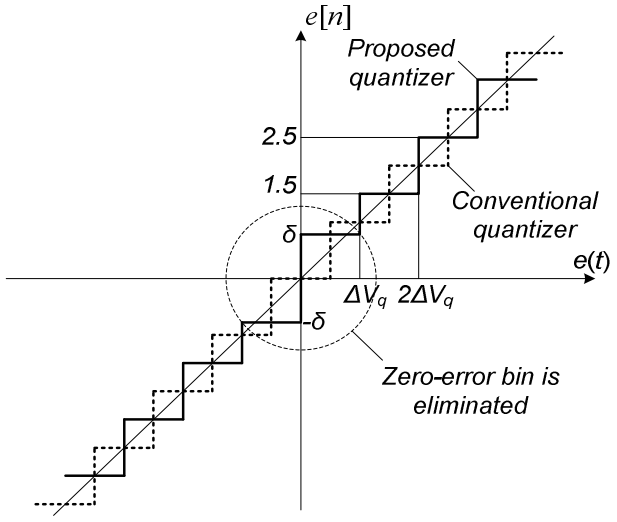


Fig. 2. Characteristics of A-D quantizers

compensator that is designed to have a pole at zero frequency. It causes frequent change of $d[n]$ to be such that their average value results in the output voltage exactly equal to V_{ref}, i.e. the average zero error value.

As shown in the following section, by selecting the parameters of the PID compensator and δ the LCO of $d[n]$ can be controlled such that their frequency is high and amplitude is small enough not to affect the output voltage regulation.

It should be noted that such control over the LCO parameters cannot be simply achieved with the conventionally used ADC with zero-error bin. As mentioned earlier, the zero-error bin makes the input signal travel in it for a longer time without being monitored. An error is detected only after the signal exceeds the bin making the LCO amplitude larger or at least equal to the bin size. To take this into account, no-LCO conditions relying on an enlargement of the zero-error bin only need to be reviewed and an additional condition limiting the maximum size of the bin introduced. In Section IV, the effect of the zero error bin and intermittent "open loop" system operation will be demonstrated through simulations and experimental results.

III. System Analysis And Design Considerations

To determine the frequency and amplitude of the duty ratio control variable's oscillations, and consequently control them, well-known tools developed for the relay system analysis are used [9]-[11]. In particular, for a predefined maximum magnitude of the output voltage oscillations a PID compensator is designed and δ selected such that the condition for the oscillations,

$$-1 = 1\angle 180° = N(A_{LCO})T(j\omega_{LCO}) \quad (1)$$

is satisfied, where $N(A_{LCO})$ is the gain of the relay (i.e. ADC without zero-error bin) at the LCO A_{LCO} is the amplitude of the output voltage oscillations, ω_{LCO} is their radial frequency, and $T(j\omega_{LCO})$ the complex gain of the remaining part of the system (the power stage and the remaining parts of the controller) at that frequency.

The nonlinear gain of the relay, describing the relation between the magnitudes of the ADC's input voltage and the duty ratio control variable oscillations, is modeled as

$$N(A_{LCO}) = \frac{4\delta}{\pi A_{LCO}} \tag{2}$$

using the describing functions method [8]-[10].

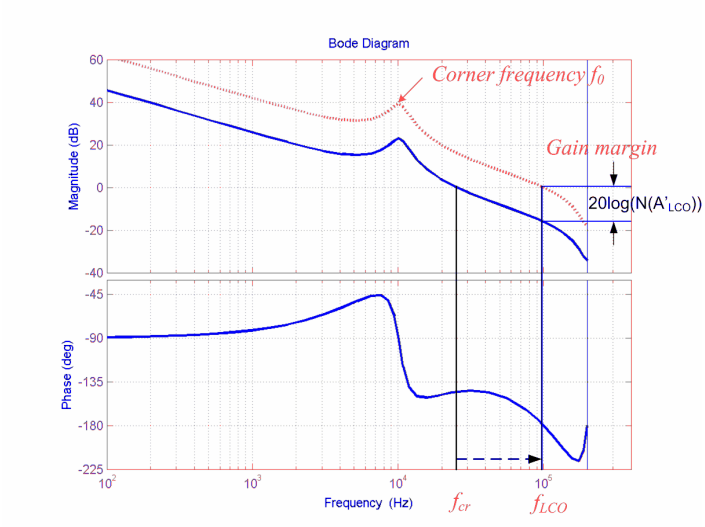


Fig. 3. Bode plots of the total loop gains. (solid): $T(j\omega)$; (dotted): $N(A_{LCO})T(j\omega)$.

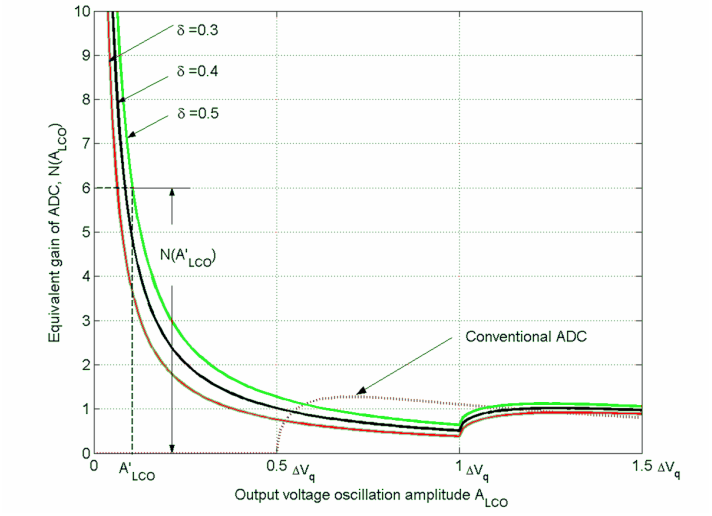


Fig. 4. Describing functions of the proposed A-D quantizer with different design parameter δ.

Taking into account the previous equations, a two-step procedure for selecting δ and the PID compensator can be given through a buck converter example.

In the first step, the frequency of LCO oscillations is set. Following the procedure shown in [11], a PID compensator having a pole at the origin and two zeroes at frequencies slightly lower than f_0 is designed, such that the desired crossover frequency f_{cr}, and phase margin are satisfied. In addition, by the same compensator the Bode plots of $T(j\omega)$, shown in Fig.3, are shaped so that the phase shift of 180° occurs at a frequency f_{LCO} significantly higher than the power stage corner frequency. Since the relay does not introduce any phase shift, the LCO will occur at f_{LCO} if the gain condition is satisfied.

The second step is the gain adjustment. For a predefined maximum amplitude of the converter output voltage oscillations, A'_{LCO}, δ is selected to provide the required gain $N(A'_{LCO})$ so that the condition given by (1) is satisfied:

$$\begin{aligned} 1 &= N(A'_{LCO})\,|T(j\omega_{LCO})| \\ 1 &= N(A'_{LCO})\left|C_{PID}(e^{j\omega_{LCO}T_{sw}})\right|\cdot\left|G(j\omega_{LCO})\right| \\ 1 &= \frac{\pi}{4}\frac{\delta}{A'_{LCO}}\left|C_{PID}(e^{j\omega_{LCO}T_{sw}})\right|\cdot\left|G(j\omega_{LCO})\right| \\ \Rightarrow \delta &= \frac{4A'_{LCO}}{\pi\left|C_{PID}(e^{j\omega_{LCO}T_{sw}})\right|\cdot\left|G(j\omega_{LCO})\right|} \end{aligned} \tag{3}$$

where $\left|C_{PID}(e^{j\omega_{LCO}T_{sw}})\right|$, $\left|G(j\omega_{LCO})\right|$ are the gains of digital PID compensator and power stage at LCO frequency respectively and T_{sw} the switching period.

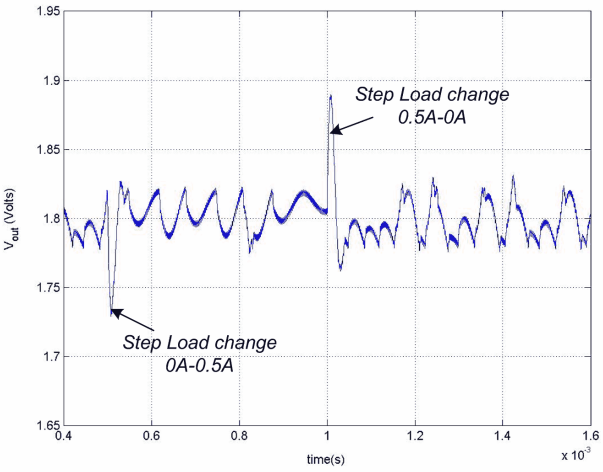
In other words, by changing the size of the relay output, $N(A'_{LCO})$ is set to be equal to the gain margin of the system, as shown in Fig. 3.

Fig. 4 shows how the gain of the ADC without zero-error bin, $N(A'_{LCO})$, depends on the amplitude of the output voltage oscillations for several values of δ. The gain dependence for a conventional ADC, with zero-error bin is also demonstrated. It can be seen that, unlike in the conventional case where the gain drops to zero, for an arbitrary small amplitude of the voltage oscillations, δ can be selected so that the desired gain $N(A'_{LCO})$ causing high-frequency oscillations is obtained.

In practice, the minimum value of the oscillations is small but limited with the hysteresis band of the comparator in ADC and the resolution of the DPWM. With a non-ideal comparator with hysteresis, the gain of the PID at f_{LCO} needs to be large enough to cause $d[n]$ to change frequently so a quick averaging resulting in improved regulation is obtained.

IV. Simulation and Experimental Results

Based on the system of Fig. 1, a Matlab/Simulink model and an experimental 5 V to 1.8 V, 5 W SMPS prototype operating at 400 kHz switching frequency were built. The power stage



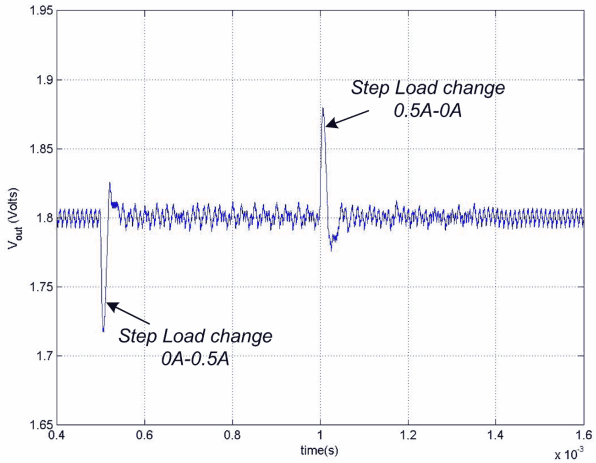
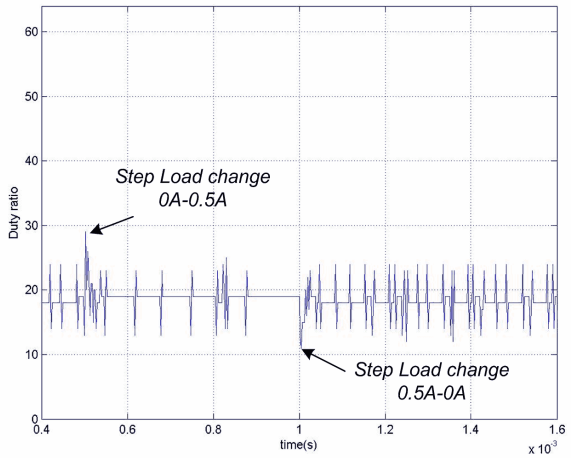


Fig. 5. Voltage regulation comparison in simulations. (Top): large LCO with conventional ADC; (Bottom): small LCO with non-zero ADC.



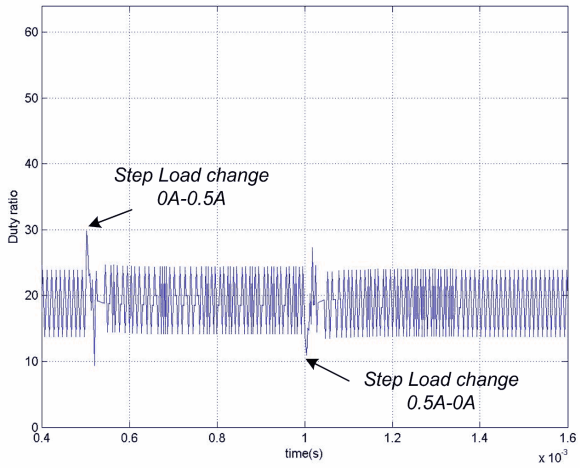


Fig. 6. Comparison of duty ratio signal in simulations. Top: conventional low-resolution controller; Bottom: the controller with non-zero error coding scheme.

filter components are L=8μH and C=30μF, resulting in approximately 10 kHz corner frequency. The characteristics of the controller utilizing the non-zero error coding scheme with ΔV_q=30mV, and a conventional one were compared. In both cases a 6-bit DPWM and a PID having equally low resolution were used.

A. Simulations

The voltage regulation and dynamic response comparisons of the two systems are shown in Fig. 5. It shows systems responses to 0.5 A load step changes. It can be seen that the dynamic response is not affected by the non-zero error coding scheme. However, the steady-state LCO amplitude is reduced from 50mV to 20mV, which is a 60 percent improvement.

Fig. 6 shows a comparison of the oscillations in duty ratio value for the both controllers. It can be seen that the new error coding scheme results in oscillations at much higher frequency (approximately 100 kHz), which can be completely attenuated by the power stage filter. On the other hand, the zero-error bin of the conventional controller slows down the frequency of oscillations and occasionally they fall bellow the corner frequency of the filter. This results in the intermittent output voltage oscillations.

B. Experimental Results

The experimental results are obtained with an FPGA-based prototype. The proposed ADC is implemented with off-shelf comparators having a 3mV hysteresis. The output voltage waveforms for the non-zero error and the conventional systems are shown in Fig. 7. Following the design guidelines of Section III, for the non-zero error controller, the PID compensator coefficients and δ are selected to result in the peak-to-peak amplitude of the output voltage oscillations no larger than 25 mV, i.e. A_{LCO}=12.5mV. A comparison with the output oscillations of the conventional controller shows that the new coding scheme eliminates low frequency noise and reduces the amplitude of the LCO by half. The results confirm effectiveness of the non-zero error coding scheme and show that a fairly good output voltage regulation can be achieved with a simple low-resolution DPWM.

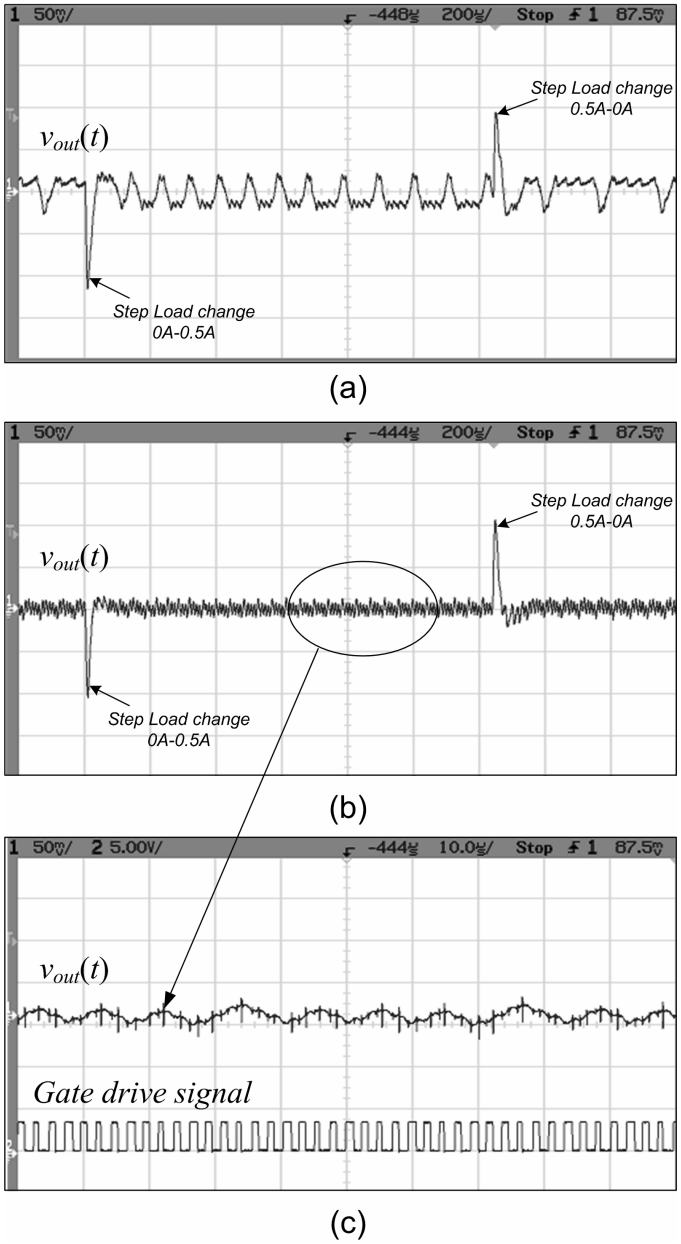


Fig. 7. Experimental results: (a) large LCO with conventional ADC ; (b) small LCO with non-zero ADC; (c) enlarged view of (b).

V. CONCLUSIONS

A method for improving voltage regulation in digitally controlled SMPS with a low resolution DPWM that does not need any additional hardware is introduced. It is shown that by eliminating zero-error bin from the ADC, the frequency of LCO can be increased beyond the corner frequency of the filter and the effective DPWM resolution improved through a quasi Σ-Δ modulation effect. The effectiveness of the method is verified with an experimental prototype.

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