Digitally-Controlled Steered-Inductor Buck Converter for Improving Heavy-to-Light Load Transient Response

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Abstract — **In this paper a novel digital controller and modified buck converter for improving heavy-to-light load transient response of low-power low-voltage dc-dc converters is introduced. The system is primarily designed for point-of-load (PoL) converters providing low regulated voltages for digital loads. In conventional buck topologies, the low output voltage, often below 1 V, severely limits the inductor current slew rate during the transients. To overcome this physical limitation, a modification is introduced whereby during heavy-to-light transients, the inductor current is, by the means of two extra switches, steered into the source and at the same time, the slew-rate of the current is significantly increased. The steering action is governed by a digital controller. The effectiveness of the system is verified on an FPGA-controlled, 12 V to 0.9 V, 10 W, experimental prototype. The results show that the steered-inductor digitally controlled buck converter has much shorter settling time and provides 2.8 times smaller overshoot than the conventional buck.**

I. INTRODUCTION

In point-of-load (PoL) converters supplying digital loads, such as digital audio and video signal processors, memory and other functional blocks of modern electronics, a fast response to load transients is of key importance. It reduces the possibility of system failures as well as errors in data processing and/or allows the power stage filtering components to be minimized.

Obtaining a fast response becomes especially challenging when heavy-to-light load steps occur in widely used buck converter-based PoL providing very low output voltages. Then, the reduction of the inductor current from the initial to the lower steady-state value is slow, causing significant output voltage overshoots and/or requiring a large output capacitance. For a buck converter regulating the output at V_{out} and having filtering inductance L, the maximum speed of the reduction is limited with the slew rate V_{out}/L [1]. In modern digital systems, supplied by voltages as low as 0.9 V, this slew rate is therefore low, and is to become even lower. According to [2], supply voltages of digital systems are expected to decrease to 0.7 V soon, and to drop to 0.5 V in the long term. As a consequence, in the conventional PoL, the size of the output capacitor suppressing voltage spikes is likely to increase, negatively affecting the system size and cost.

Several solutions have been proposed for augmenting the buck topology to improve transient response. In [3], parallel resistors are added to the inductor and the capacitor to bypass the energy storage elements during transients. Such a solution significantly improves the response but at the same time adds new losses. During heavy-to-light transients, excess energy is essentially "burned" through the resistors. The addition of extra conduction paths during transient [4], [5], though also effective, suffers from similar problems. Different inductances used in steady state and during transient [6]-[8] improve the response but often require specialized and costly inductors.

In this paper, we introduce a novel digital controller and a modified buck converter for improving heavy-to-light load transient response. Figure 1 shows the modified converter topology. During heavy-to-light load transients, the inductor voltage is increased and current steered away from the output capacitor into the source. The inductor current steering is performed with two extra switches, Q_3 and Q_4, through a multi-mode digital controller. As it will be shown in the following sections, the new topology significantly improves the load transient response for digital loads and is well suited for low-power PoL, where the introduction of two extra switches does not significantly affect the converter efficiency. It also allows the excess of energy created during transient to be in a large part recovered instead of completely wasted, which is important for systems going through frequent load transients. Section II of this paper explains the principle of operation of this system. Section III describes the

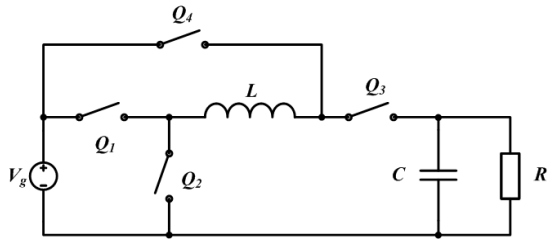

Fig. 1. Steered-inductor buck converter topology for improving heavy-to-light load transient response

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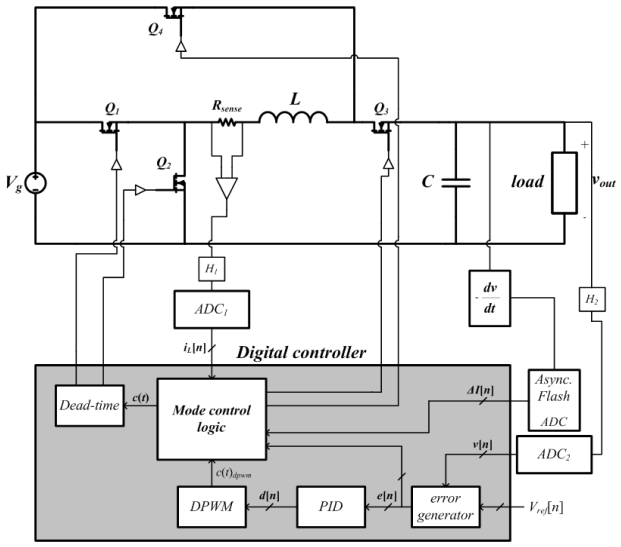


Fig. 2. Digitally controlled steered-inductor buck converter.

implementation of the controller and addresses practical design challenges. Experimental results demonstrating system operation are shown in Section IV.

II. Principle of Operation

The full system with the modified buck converter and digital controller is shown in Figure 2. In steady-state and during light-to-heavy transients, the system of Fig. 2 operates as a standard digitally controlled buck converter [9]-[13]. The output voltage is sampled by an analog-to-digital converter (ADC) and forwarded to the *error generator*, which produces an error $e[n]$ based on the value of the output voltage and the digital reference $V_{ref}[n]$. The error is fed into the *digital PID* compensator that produces a duty ratio command $d[n]$ for the digital pulse-width modulator (*DPWM*). The *mode control logic* also monitors $e[n]$. This block contains a programmable threshold value $e_{transient}$. As long as $e[n] > e_{transient}$, the converter is either in steady-state or going through a light-to-heavy load transient. Therefore, the *mode control logic* forwards the output of the *DPWM* to the *dead-time* circuit which controls non-overlapping times of switches Q_1 and Q_2, while keeping Q_3 on and Q_4 off. During this mode average inductor current is equal to that of the load and the converter can be depicted with the equivalent circuit shown in Fig. 3(a).

A. Heavy-to-light Load Transient Operation with Steered-Inductor Configuration

Once the error drops below the threshold, i.e. $e[n] < e_{transient}$, the *mode control logic* detects a heavy-to-light transient, suspends the *DPWM* and *PID*, turns off transistors Q_1, Q_3, and turns on Q_2 and Q_4. This results in the circuit topology of Fig. 3(b), the waveforms of which are shown in Fig. 4. Now, the inductor current that, at this point, is larger than the load current, is steered into the source preventing the output capacitor overcharge and consequent voltage overshoots. Note that in many practical systems this current can actually be steered into the capacitor of an input filter, which is usually placed between the buck converter and the source to minimize the influence of switching noise [1]. Figure 4 also shows that the change of the converter configuration creates two additional positive effects. First, it allows the initially created voltage peak that triggered the process to start decreasing with time constant $\tau = RC$, where R is the load resistance and C the output capacitance. The second is that the inductor discharge slew rate becomes proportional to the input voltage V_g, i.e.

$$\frac{di_L}{dt} = \frac{-V_g}{L}. \quad (1)$$

In the targeted applications, this rate is much higher than that of the of the conventional buck topology, i.e.

$$\frac{di_L}{dt} = \frac{-v_{out}}{L} \quad (2)$$

Taking into account that in numerous applications V_g is larger by around a factor of 10 than v_{out}, the improvement in the slew rate is quite significant.

After the current of the inductor drops to the new required steady-state level, the converter is returned to the configuration of Fig. 3(a).

III. Practical Implementation and Design Challenges

One of the main challenges in the controller implementation is the determination of the time instant when the converter should switch back from the transient mode into regular buck operation with lower output current. Another is the need to prevent the output voltage from possibly dropping to an unacceptably low level during the heavy-to-light transient.

The "steered-current" configuration of Fig. 3(b) must be maintained until the inductor current $i_L(t)$ reaches the new output value. To implement the system it would be possible to use two current sensors, one each for the inductor and load currents, however such a solution might not be practical for the targeted cost-sensitive applications.

Instead, as shown in Fig. 2, in this system only the inductor current is measured. During steady-state, $i_L(t)$ is sampled by an A/D converter via the sensing resistor R_{sense}, converted to a digital value $I_L[n]$, and then forwarded to the *mode control logic*. Since this block also monitors $e[n]$, it knows to sample $i_L(t)$ only once after the system has settled into-steady state, that is, only after $e[n] = 0$ consistently for at least three switching cycles.

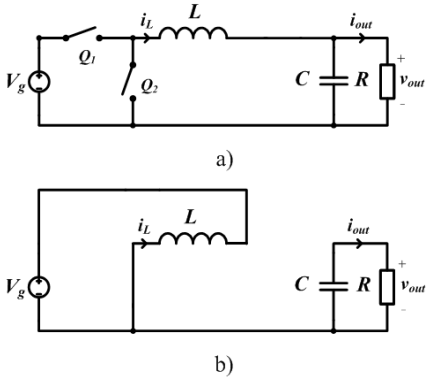
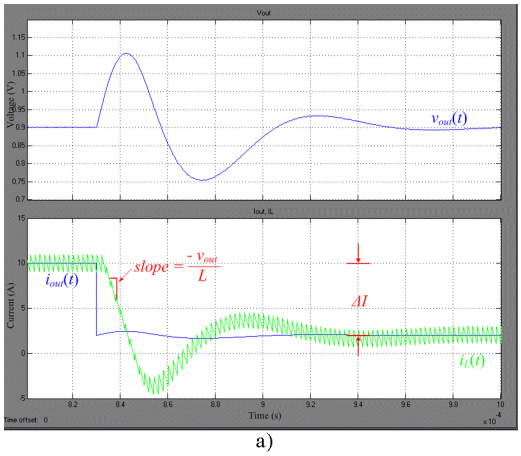
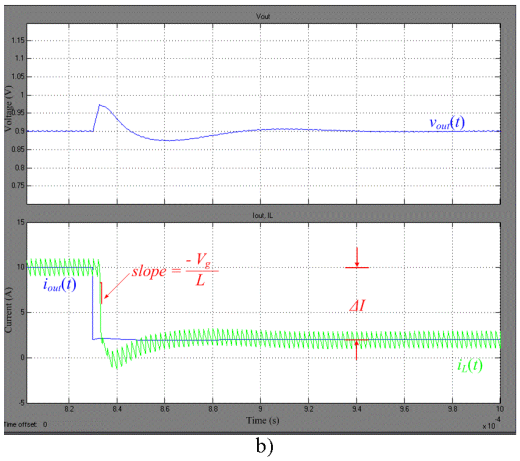


Fig. 3. The two modes of the steered-inductor buck converter (a) conventional operation; b) operation during heavy-to-light load transient



a)



b)

Fig. 4. Simulation results, transient response to a 10 A to 2 A load step change (ΔI = 8 A):
a) (above) with PID only b) (below) with inductor current steering

This is sufficient, since the average current will stay the same until the next load change. The result is a very slow A/D sampling rate which saves power compared to an A/D converter with a constant sampling frequency.

A. Determining the Load-step Change ΔI and the New Steady-state Inductor Current

The load change is determined through estimation of the capacitor current $i_C(t)$. In steady-state, the average value of $i_C(t)$ is zero, i.e. the inductor and load currents are the same. During a heavy-to-light transient, in the first instant, the load current suddenly drops while the inductor current $i_L(t)$ remains practically unchanged, causing a spike in the capacitor current. This deviation of the capacitor current, ΔI, is equal to the change in load current. The transient current waveforms are shown in Fig. 5.

In order to determine $i_C(t)$, and by extension ΔI, a capacitor current sensor is not necessary, since it is defined as

$$i_C(t) = C\frac{dv_C}{dt} \tag{3}$$

Therefore, the system of Fig. 2 uses an inverting differentiator which takes the capacitor voltage as input. The output of the differentiator, $-dv_c/dt$, is fed into an asynchronous flash A/D converter, shown in Fig. 6. Upon a heavy-to-light transient, the *mode control logic* generates the *trans_mode* signal that latches the flash A/D output and captures the load current change $\Delta I[n]$. This value is then sent to the mode control logic which calculates the new value for the inductor steady-state current, namely,

$$I_L[n]_{new} = I_L[n]_{old} - \Delta I[n], \tag{4}$$

where $I_L[n]_{old}$ is the previous steady-state inductor current value captured prior to the transient and $I_L[n]_{new}$ is what the inductor current should be when the transient is finished.

Also at this point, the sampling rate of the inductor current A/D is increased to 16 times the switching frequency, and the mode control logic monitors its output until the condition in (4) is satisfied. Once the new current level is reached the mode control logic turns off Q_4 and turns on Q_3 returning the converter to regular mode and activating the *PID* and *DPWM* again.

The mode control logic block itself is a very simple finite-state machine.

B. Preventing Drastic Output Voltage Dips during Heavy-to-light Transients

Another possible problem is the different discharge rate of the inductor current and the capacitor voltage. Depending on the values of L, C, and the load change, it is possible for the output voltage to dip to an unacceptably low level before the inductor current discharges to the value set by the mode control logic. Therefore, the mode control logic contains an additional safeguard, an error threshold e_{max}. If at any point during the heavy-to-light transient $e[n] > e_{max}$, the system exits the transient configuration and returns to conventional buck operation regardless of the value of $i_L(t)$. Although the resulting transient response in this case is not ideal, it is still better than the PID-only case. Even though the inductor current in such a situation has not reached the level defined by (4), it has nevertheless decreased by some amount at a much faster rate than in a regular buck. Despite the fact that the conventional controller then completes the response to transient, transient performance is still significantly better. Now the PID compensator is correcting a load-step that is much smaller than the one that initially occurred.

It should also be noted that the system can be further simplified by eliminating the current sensing circuit

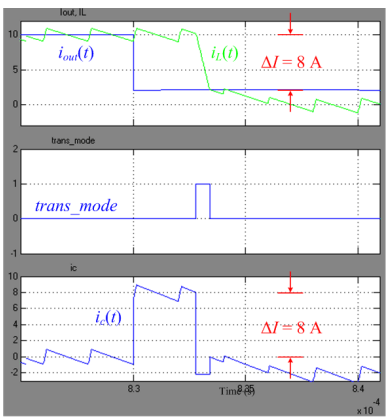


Fig. 5. The spike in capacitor current $i_c(t)$ during heavy-to-light transient (with current steering). The delay between the load step and the *trans_mode* signal is due to delay of the ADC

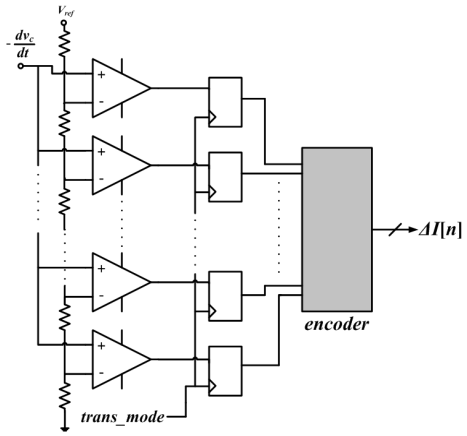


Fig. 6. Flash ADC used to determine ΔI

completely. This can be done by utilizing techniques for sensor-less current estimation as shown in [14], [15]. Therefore, ADC_1 and R_{sense} can be eliminated from the system of Fig. 2.

Furthermore, it is also possible to eliminate the differentiator circuit. By using the asynchronous flash ADC to monitor the output voltage, the current step ΔI can be obtained with the utilization of a continuous-time digital processor [16]-[17], whose application for obtaining optimal response with a conventional buck configuration is shown in [18]. Using this method to observe the output voltage deviation upon a heavy-to-light transient it is possible to determine the slope of the capacitor voltage, and then calculate the current change ΔI using equation (3). This allows for the removal of ADC_2 and the differentiator from the system shown in Fig. 2.

IV. Experimental Results

Based on the diagram of Fig. 2, an experimental prototype was built and tested. The 12 V-to-0.9 V, 10 W, power stage operates at the switching frequency of $f_{sw} = 500$ kHz, where $L = 0.9$ µH and $C = 400$ µF. The digital controller was implemented on an FPGA. To verify the effectiveness of the steered-inductor topology, its load transient response is compared with that of the system operating as a conventional buck controlled by a fast PID. The PID is constructed such that the system has the crossover frequency of 1/10 of f_{sw} and, during light-to-heavy load transients, is used for the both configurations. The system was designed with the minimum necessary capacitance to always maintain $0.75\ V < v_{out} < 1.05\ V$. This is inside the limits of modern digital loads. If a smaller deviation is required, the system can be easily redesigned.

A. Functional Verification

Fig. 7 shows the key waveforms of the steered inductor topology during an 8 A load step decrease. It can be seen that, when the transient is detected, the inductor current rapidly decreases to the new steady state value, and the converter returns into regular operating mode. The new steady state value is determined by the sensed change of the capacitor current. After the action is completed a small remaining deviation of the output voltage is compensated with the PID. This small deviation is caused by a loss of the capacitor charge, which can be taken into account and compensated with a more advanced control algorithm requiring more powerful hardware for implementation. Fig. 7 also shows the change in the states of switches Q_3 and Q_4.

Fig. 8 shows the output of the inverting differentiator during an 8 A load step decrease and the ΔI sampled by the flash ADC.

B. Transient Response Comparison

Effectiveness of the steered inductor system is demonstrated in Fig. 9 showing transient responses of the system operating as a conventional and a steered inductor buck for 8 A load changes. It can be seen that, due to a relatively high input voltage and the fast PID, the converter quickly recovers from a light-to-heavy load transient (in approximately 10 switching cycles). However, for the opposite transient, the conventional buck suffers from a large output voltage overshoot and long settling time. On the other side, the new steered inductor results in approximately 2.8 times smaller voltage overshoot and equally faster recovery time. Theoretically, with the new configuration it would be possible to achieve the response which is V_g/V_{out} times better than that of the conventional controller, but the system delays and finite value of the error detector threshold reduce the improvement.

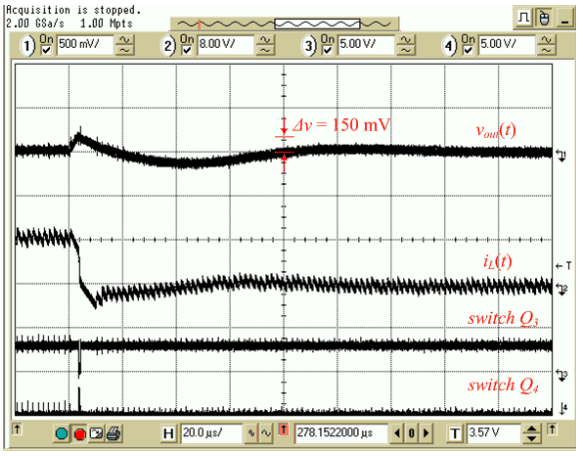


Fig. 7. Transient response with current steering to an 8 A load step decrease. Ch1: v_{out}, 500 mV/div; Ch2: i_L, 8 A/V, 8 V/div; Ch3: Q_3, 5 V/div; Ch4: Q_4, 5V/div; Time scale: 20 µs/div

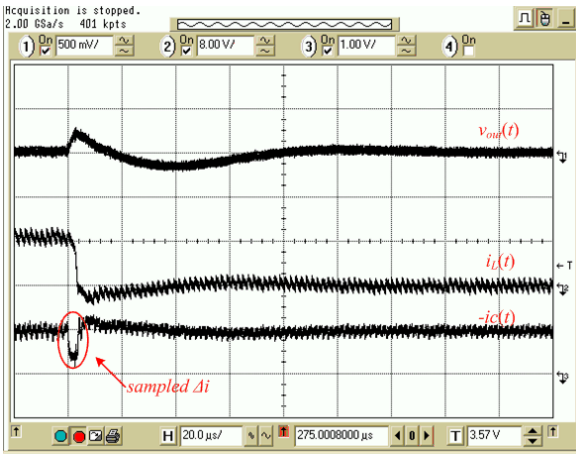


Fig. 8. Transient response with current steering to an 8 A load step decrease, showing the output of the inverting differentiator. Ch1: v_{out}, 500 mV/div; Ch2: i_L, 8 A/V, 8 V/div; Ch3: $-i_C$, 1 V/div; Time scale: 20 µs/div

V. Conclusions

A digitally-controlled modified buck converter topology for improving heavy-to-light load transient response of dc-dc converters with low output voltages is introduced. To eliminate voltage overshoots, and speed up the current slew rate caused by the physical limitations of the conventional buck, the inductor current is steered into the source during transients. A digital controller using information about the capacitor discharge rate is employed to determine the duration of the transient sequence. The effectiveness of the method is verified on an experimental prototype, which is compared to the traditional buck. About 2.8 times smaller overshoot and equally shorter recovery time are demonstrated.

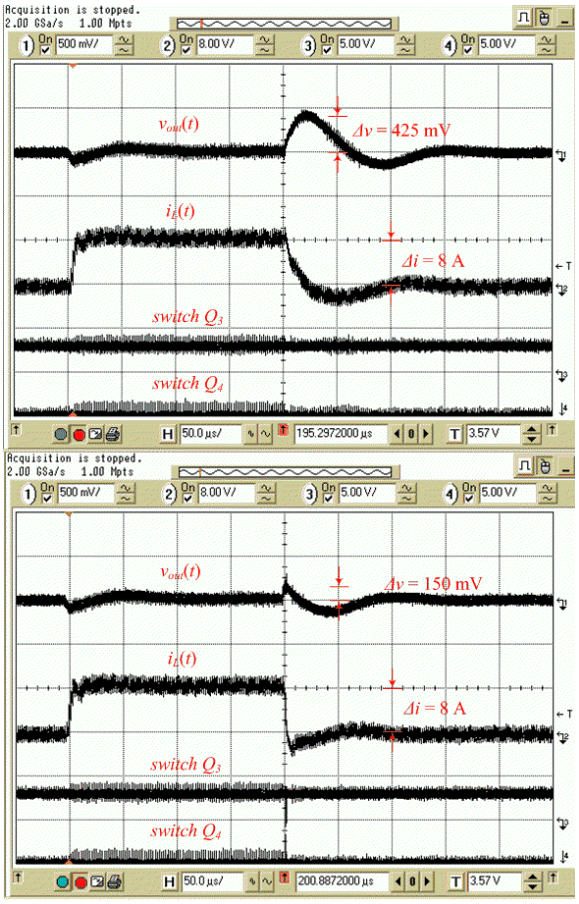


Fig. 9. Transient response to an 8 A load step change: (top) with PID only; (bottom) with inductor current steering. Ch1: v_{out}, 500 mV/div; Ch2: i_L, 8 A/V, 8 V/div; Ch3: Q_3, 5 V/div; Ch4: Q_4, 5V/div; Time scale: 50 µs/div

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