Plug-and-Play Digital Controllers for Scalable Low-Power SMPS

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***Abstract* – This paper describes a self-configured digital controller suitable for use in both single phase and multiphase converter topologies. In multiphase mode, the system operates in a decentralized fashion, where each phase has its own controller. To synchronize phases and minimize inductor current ripple, the controllers configure themselves during a two-step initialization procedure. First, the number of phases is detected via a simple communication protocol. Then, using a charge-based identification process, the *LC* products among phases are estimated in order to set the phase switching sequence, such that the current ripple is minimized. The operation of the system is demonstrated with a 5V/1.5V, 30W, 4-phase buck experimental prototype operating at a switching frequency of 800 kHz.**

I. INTRODUCTION

Scalable dc-dc converters [1], traditionally used in medium and high power systems only, are becoming an attractive solution for supplying computers, portable devices, and other loads consuming up to several hundreds watts of power.

Through paralleling, scalable converters can accomodate the requirements of low-power electronic loads, with power ratings that change over time. For example, each new microprocessor generation has a different current and voltage rating. With a modular design, the same controller can be used in many different applications, thereby reducing the costly and time consuming process of developing custom controllers. For example, a single module can be used as a cost-effective solution for supplying a functional blocks of a miniature battery powered electronic device. On the other hand, for a CPU, an interleaved converter can be created from several modules, reducing the output voltage ripple, and improving dynamic response as well as heat distribution [2].

Even though the advantages of scalable topologies over custom-made solutions are known, they have not been widely adopted in low-power switched-mode power supplies (SMPS). This is mostly due to practical implementation problems. Sophisticated controllers developed for higher power supplies [3]-[4] cannot be directly utilized in the targeted application. In these cost-sensitive systems the complexity of the conventional controllers usually outweighs all advantages of scalable topologies.

In order to optimize the performance of scalable SMPS, the controllers need to perform several fairly demanding tasks. Namely, to obtain stable and fast operation the compensator usually needs to be redesigned each time a new phase is added. Next, in interleaved operation, phase shifting needs to be performed [5]. Also, in order to minimize the influence of phase mismatches on the current ripple, it is highly desirable to perform phase sequencing. Solutions based on a dedicated supervisory unit or manual controller adjustments used in low-volume high power applications are not well suited for low-power high production supplies. Hence, in the applications of interest, seemingly more advanced auto-configuring controllers are preferable.

Recent publications show that fairly simple implementations of auto-tuning digital controllers for low-power dc-dc SMPS are possible [6]-[10]. To automatically adjust the compensator, these auto-tuning controllers can extract information from intentionally introduced oscillations, through limit cycling [6] or through relay operation of the system [7]. These auto-tuning controllers potentially provide only a part of the solution for regulating operation of scalable low-power converters. They do not address problems related to automatic phase shifting and sequencing, which are of the key importance for multiphase operation.

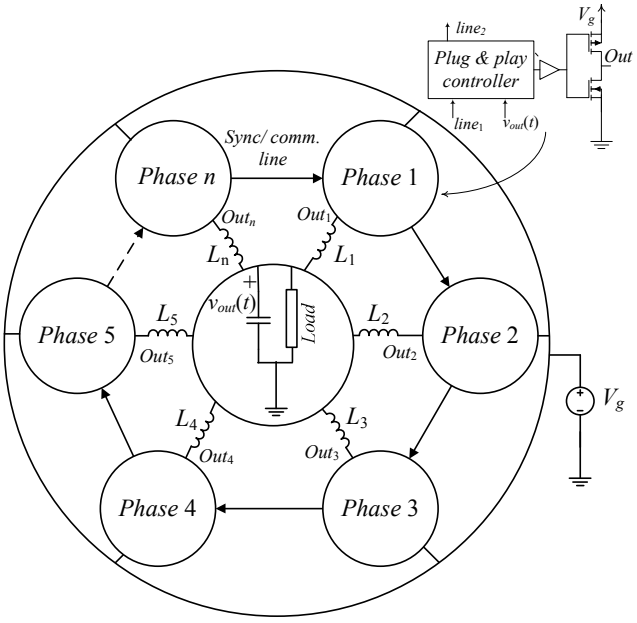

Figure 1. A multiphase dc-dc converter regulated by scalable plug-and-play digital controllers.

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In this paper we introduce auto-configuring, (i.e., plug-and-play) digital controllers (see Fig. 1) that perform automatic phase shifting and sequencing, and as such are suitable for designing low-power scalable SMPS. The controllers can be used individually in single phase systems, or in interleaved topologies with an arbitrary number of phases.

The next section describes the main principles of operation of the system. Section III provides details about the auto-configuration procedures that are performed during initialization. Section IV describes the experimental setup and presents results verifying the implementation, followed by a conclusion.

II. System Overview

The operation of the *n*-phase interleaved SMPS of Fig.1 is regulated by *n* identical controllers operating in a masterless fashion. To synchronize operation, the controllers are linked through a one-wire synchronization and communication line that can operate in two modes, depending on the state of the communication switch S_1, shown in Fig. 2 When the switch is open, the controllers are connected in a series. As described in the following section, this mode is active only during one portion of the system identification process, which is performed before start-up. By closing the switch, the line turns into a communication bus that is used at all other times. The bus passes phase synchronization signals as well as data obtained through the system identification and subsequent auto-configuration.

Fig. 2 illustrates the structure of the plug-and-play digital controller. It is a modification of the conventional single phase voltage mode architecture. An error signal $e[n]$ produced by a windowed analog-to-digital converter (ADC) is processed by the compensator creating a control variable $d[n]$ for a *dual-output digital pulse-width modulator* (DPWM). In addition to producing a pulse width modulated signal $c(t)$, used for controlling the duty ratio of the power stage, it also creates a synchronization signal $ps(t)$ for the timing of the next phase in the sequence. For example, if during the phase detection process *n* phases are detected, $ps(t)$ is a signal whose duration is T_s/n, where $T_s = 1/f_s$ is the switching period.

The duty ratio for $ps(t)$ is provided by the *phase detector*, through the digital control signal $p[n]$. During initialization the phase detector sets the scalable controllers in a ring configuration, to determine the number of phases in the given system. Once the phase detection process is completed, this block closes switch S_1 to allow bus communication.

The *LC estimator and sequencer* block has multiple roles. Using a capacitor charge-based detection process it identifies the relative ratios of the phase inductor values. Based on the identification results and the results obtained from other phases, it sets its own position in the switching sequence of the entire structure. In other words, through this process, the phases are ordered in a way that minimizes the output current ripple. The identification results are also used to pass the $ps(t)$ signal to the next stage, which is not necessarily the neighboring phase. In the next phase the signal is used as a clock (*clk*), synchronizing the operation of the system.

III. Identification and Auto-Configuration

The system begins with a two-step initialization process that allows each phase to count the number of phases and estimate the relative inductances. After initialization, regular operation begins. This section describes the communication process, the details of the phase detection mechanism, the *LC* product estimation and sequencing procedure, and the regular operation of the system.

Of particular importance for the auto-configuration process is the two-mode communication system and its protocol. During bus mode, phases that are not transmitting data at a given time output a high impedance (Z) signal to the bus. Only the phase that is currently transmitting data may pull the bus low. The controllers are designed in such a way that multiple phases will never transmit data onto the bus simultaneously. In series mode, the $line_1$ and $line_2$ ports of Fig. 2 are not connected. Rather, the data sent from a given phase is only read by the next phase in the ring.

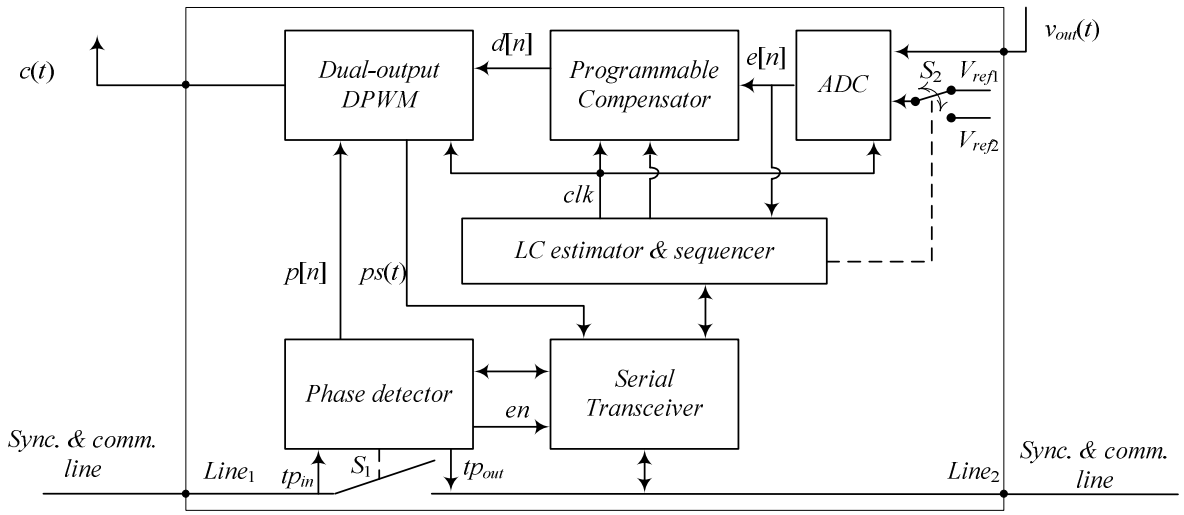

Figure 2. Block diagram of the plug-and-play digital controller.

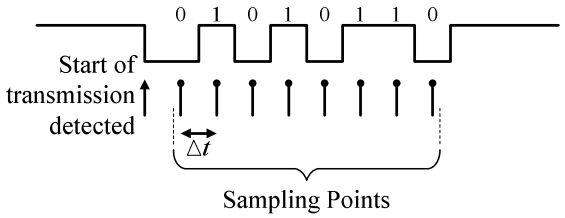

Figure 3. Diagram of the signal and timing for the communication protocol in bus mode. Each transmission consists of the bus being pulled low, followed by 8 serial bits of data.

Series mode is used in the first stage of the initialization procedure, while bus mode is used in the remaining stages.

The transmission and receiving process is illustrated in Fig. 3. First, the transmitting phase pulls down the bus line to indicate the start of a transmission. Next, using delay cells, the transmitting phase outputs the values of each bit one at a time. The receiving phases detect the start of the transmission, and using similar delay cells, sample the bus line at the appropriate times. 8 bits are sent during each serial transmission. Similar single wire serial protocols such as [9] have proven to be reliable in sending data at high baud rates. Using this protocol, only two communication pins are required per phase, independent of the number of phases used. This protocol was selected in order to promote scalability. With a traditional multiphase approach, the master controller must communicate with each phase separately. Therefore, the pin requirements of the chip grow as the number of phases increases. In this approach, only two pins per phase are required for communication, regardless of the number of phases.

The system begins with a two-step initialization process that allows each phase to count the number of phases and measure the relative inductances. After initialization, regular operation begins. This section describes the details of the phase detection mechanism, the relative inductance estimation procedure, and the regular operation of the system.

A. Phase Detection

In this stage, all power switches are disabled. During initialization, none of the phases have any knowledge about the total number of phases present in the system. A phase detection procedure is used to count the number of phases.

During the phase detection procedure, the communication protocol operates in series mode, where a phase's output signal can only be seen by the next phase in the ring. This is done so that each of the phases can be counted one at a time.

The phase detection procedure (see Fig. 4) begins with an initial phase, which is selected through a random process. The initial phase sends a value of 1 to the next phase in the ring. The next phase reads this value, stores it in a register, increments it by one, and sends this value to the next phase in the ring. This process continues until the initial phase receives a transmission from the final phase in the ring. This value corresponds to the total number of phases in the system. After a sufficient period of time, all phases switch the communication method into bus mode and the initial phase transmits the number of phases across the bus.

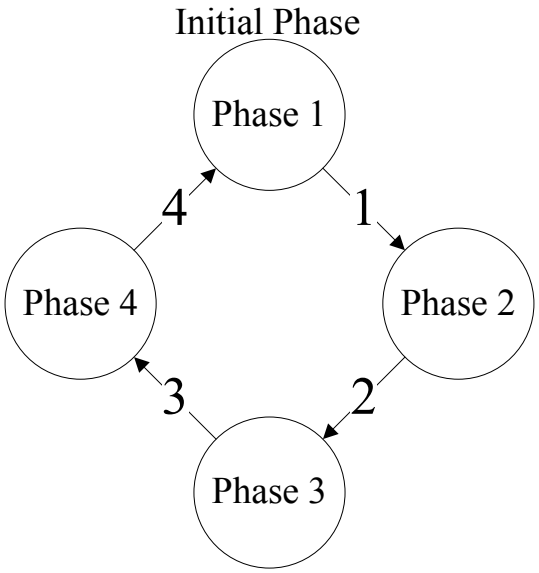

Figure 4. The phase identification and counting procedure with four phases.

At this point, each phase reads the number of phases and also knows its own order in the ring. The phase detector calculates $p[n]$, proportional to the time period by which the switching signals should be shifted for interleaved operation. For n phases and a switching frequency f_s, this period is equal to $1/(nf_s)$ The next step in the initialization procedure may now begin

B. LC Estimation and Sequencing

The inductance in each phase greatly influences the operation of a multiphase power supply. Due to non-idealities in production, an inductance may vary from its nominal value [12]. Non-idealities in the inductor values can mitigate the advantage of ripple cancellation achieved from ideal multiphase converters. [13] suggests a method of measuring the inductor current ripple in each individual phase during start-up, and reordering the phases in such a way that the ripple is reduced even in the presence of inductor non-idealities. The idea is to order the phases such that phases with similar current ripples are placed 180° apart from each other. In this way, similar variances in ripple between two phases can cancel each other out, which results in a reduction in total current ripple.

An algorithm similar to the one presented in [13] is employed here. The algorithm has been adapted for the masterless case. Also, this implementation does not require current sensors, which add to the cost and size of a SMPS system.

This process entails each phase charging and discharging the output capacitance before regular operation begins, and measuring the charge time. The load should not be connected during this time because the voltage is lower than the rated value. Therefore, this process works under the assumption that a Power-Good signal is present. This means that the load is not connected to the power supply until a sufficient voltage has been established. This feature is very common in many applications, such as CPU's. For example, [14] employs a Power-Good signal.

During initialization, the phases each take turns independently charging the output capacitor, while the other phases are switched off, with the load disconnected. The currently active phase switches at a low duty cycle and charges the output voltage to a specified value well below the rated output value. This is accomplished by using V_{ref1} to achieve a reduced output voltage (see Fig. 2). A low duty cycle value is used to avoid a large inrush current that could potentially damage the power stage components. Once the specified value is reached, the output voltage is discharged until no energy remains in the inductor or capacitor. The time taken to charge the output voltage to the specified value is measured, and this value is transmitted to the other phases using the communication bus. The remaining phases repeat this process one at a time, such that the charge times of all phases are known. The phases perform this task in the order they were assigned during the phase detection procedure. For a given capacitance, a larger inductance will result in a longer charge time. Even though the numerical inductance values cannot easily be determined in this fashion, their charge times can be compared.

The charge time in each of the phases is used to minimize the output voltage ripple. As shown in [13], the ripple in each phase of a multiphase converter depends mainly on the inductance value. If the inductances among phases vary from one another, the ripple size will vary as well. The size of the ripple in a given phase is inversely proportional to its inductance value.

The phases are ordered in such a way that phases with similar estimated values are placed 180° apart. Each phase masterlessly determines its unique order in the switching sequence by comparing its charge time to those of the other phases.

C. Regular Operation

Once each phase determines the number of phases in the system and its switching sequence order, regular operation may begin. During regular operation, the communication protocol operates in bus mode. The phase ordered first in the previous step begins the process of regular operation. It immediately begins its switching cycle.

The DPWM then performs the timing operations necessary to designate when the next phase should begin its switching cycle. With n phases, the next phases begin $1/(nf_s)$ after the start of the current phase's switching cycle, where f_s is the switching frequency. At this point in time, the first phase sends a pulse over the bus. The second phase then starts its switching cycle. Since each phase has a unique order in the sequence, only once phase will begin its switching period. After a period of $1/(nf_s)$, the second phase sends a signal across the bus to indicate that the third phase's switching cycle should begin, and so on. Each phase constantly monitors the bus to determine when it should begin its next switching cycle.

It is worthwhile to note that the system's transient response could be improved by employing a charge initialization process similar to the relative inductance estimation process and utilizing information about the LC product. This, as well as knowledge of the number of phases, could be used to estimate the dynamic characteristics of the system.

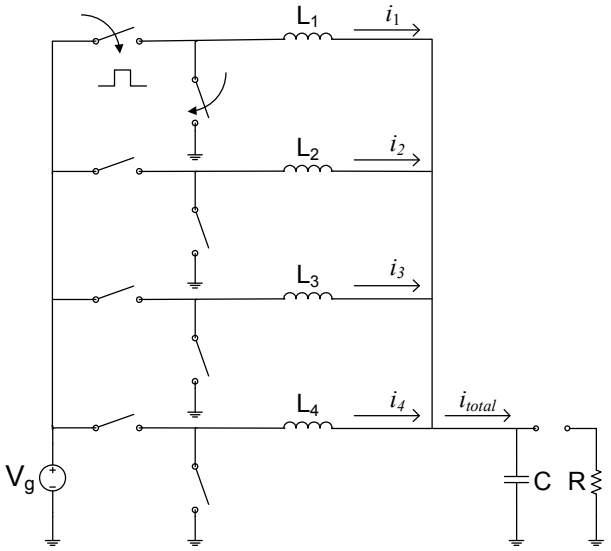

Figure 5. The charging and discharging process for estimating LC products of each phase.

IV. Experimental Verification

Based on the diagrams shown in Figs. 1 and 2, an experimental setup was developed to verify the feasibility of the proposed system. The setup includes an Altera DE2 FPGA development board and 4 power stages Individual phases are can be easily added or removed with a plug-in interface. The rated input voltage is 5V and the reference output voltage is 1.5V. The system operates at a switching frequency of 800 kHz. The system is designed to work with a nominal inductance of 0.75µH per phase. However, in order to demonstrate the effectiveness of the phase ordering procedure, the inductances of two of the phases have been reduced to 0.5µH, while the inductances of the other two phases have been increased to 1.0µH.

The results demonstrated here show both the operation of the system with pre-defined phase sequencing and with the auto-reconfiguring algorithm shown in this paper.

Initially, the phase counting process occurs, as described in section III. Next, the relative inductance estimation process begins, as shown in Figs. 6 and 7. During this process, each phase charges the output to approximately 400mV and then discharges the capacitor, and charge times are measured. This process is followed by the phase sequencing procedure, and finally the system starts up.

Fig. 7, shows a zoomed version of the charging process for two different inductor values.. It can be seen that a significant difference in charge times exist, allowing proper sequencing to occur. Figs. 9 and Fig. 10 show the corresponding inductor current ripples of these phases, and the total current ripple of a system that did not go through auto-configuration shown in Fig. 10 It can be seen that, due to the mismatch of the ripples only a minor improvement in current ripple, compared to that of Fig. 9 is achieved.

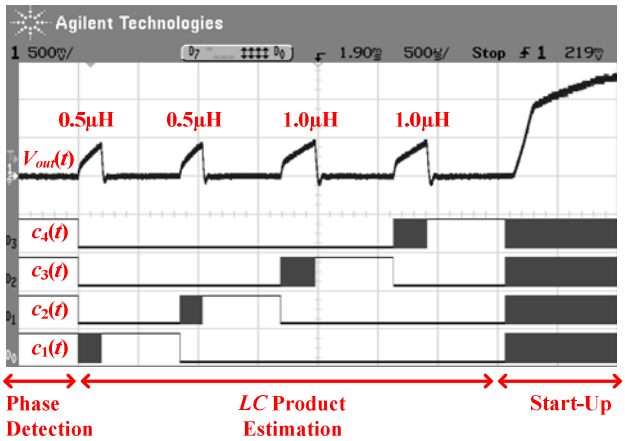

Figure 6. The initialization process, which includes the phase detection procedure and the *LC* product estimation and sequencing.

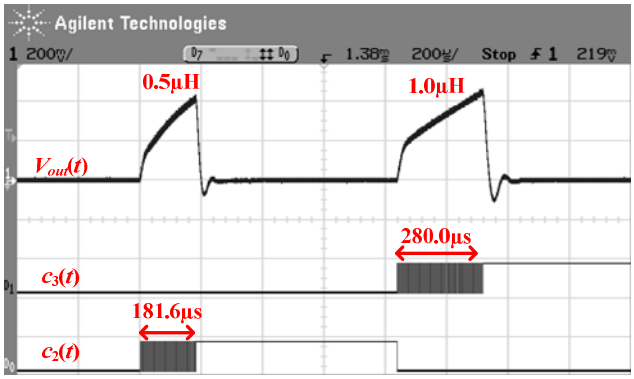

Figure 7. A comparison of the charge times for a 0.5µH phase and a 1.0µH phase.

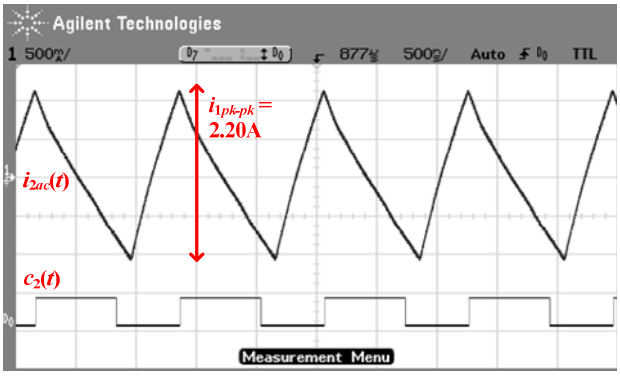

Figure 8. The steady-state ac current ripple of phase 2 (0.5µH).

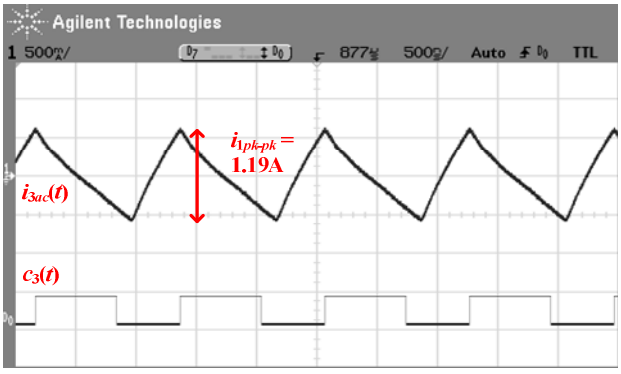

Figure 9. The steady-state ac current ripple of phase 3 (1.0µH).

Fig. 12, on the other hand, shows the case when phase

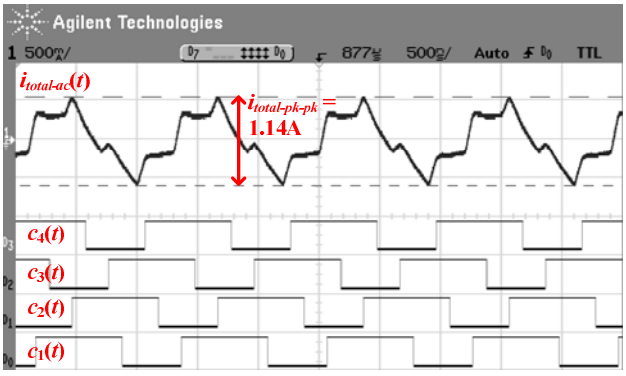

Figure 10. The steady-state total ac current ripple with unoptimized phase ordering.

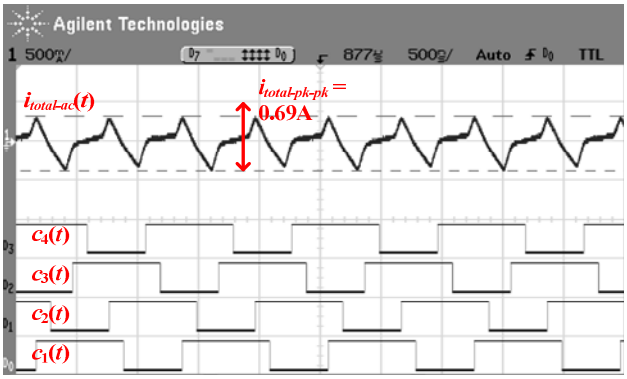

Figure 11. The steady-state total ac current ripple with optimized phase ordering.

ordering is implemented and phases with similar estimated inductances are spaced 180° apart. It can be seen that the auto-reconfiguration results in a 39% reduction of current ripple, potentially allowing for proportional reduction in the sizing of the output filter capacitor.

V. Conclusion

The digital plug-and-play controllers presented in this paper offers a solution for designing scalable low-power dc-dc SMPS. They automatically identify the number of phases, difference in inductance values, and consequently reconfigure the system such that the current ripple is minimized. The identification process is performed through a charge-based algorithm that does not require costly current sensing circuits. The effectiveness of the system is demonstrated on an experimental setup, showing that the auto-reconfiguration significantly reduces current ripple.

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