A 1V Buck Converter IC with Hybrid Current-Mode Control and a Charge-Pump DAC

Olivier Trescases *, Nabeel Rahman *, Aleksandar Prodić, Wai Tung Ng
University of Toronto, Department of Electrical and Computer Engineering
10 King's College Road, Toronto, ON, M5S 3G4, Canada

***Abstract*— This paper presents an integrated dc-dc converter with an output voltage of 1 V for portable applications. A hybrid peak current-mode control-scheme is demonstrated, where the voltage-loop compensation is achieved in the digital domain, while the current-regulation loop has a more traditional analog implementation. The main contribution of this work is the novel DAC architecture, which was developed specifically to achieve fast transient-response without needing clock frequencies beyond f_s, or expensive signal processing. Unlike the previous approach, based on an adaptive $\Delta\Sigma$ DAC, the charge-pump (CP) DAC is capable of rapidly increasing the current-command in a single-cycle during load-steps. In addition to a low steady-state current-consumption of 3 μA, the CP-DAC has a guaranteed monotonic transfer characteristic and simplifies the overall system architecture. The resulting system solution achieves dynamic response comparable to state-of-the-art analog current-mode solutions, without using a power-hungry controller, or quantizing the inductor current. A custom IC, which was fabricated in a 0.18 μm CMOS process with 5 V compatible transistors, achieves a response-time of 4 μs at f_s = 3 MHz and V_{out} = 1 V, for a 200 mA load-step. The active area of the controller is only 0.077 mm^2, and the total controller current-draw, which is heavily dominated by the on-chip senseFET current-sensor, is below 0.5 % of the load current at I_{out}= 50 mA.**

I. Introduction

Peak current-mode control (CPM) provides inherent cycle-by-cycle current-limiting and simplified loop dynamics, which allows simple and robust compensation of the control-loop. Previous work [1], [2] has reported a mixed-signal, or hybrid current-mode scheme for low-power (sub 1-W) dc-dc converters, where voltage-loop compensation is carried out in the digital domain, while the current-regulation loop has a traditional analog implementation. Using this configuration, a DAC is required at the interface of the two loops, in order to generate an analog current command. This approach results in flexible digital compensation without the need for sampling the inductor current, and also without requiring a high-frequency digital pulse-width modulator, unlike fully digital techniques [3]–[5].

In [2], a noise-shaping ($\Delta\Sigma$) DAC was used to meet the stringent resolution requirements, but it was shown that the low-pass reconstruction filter in the DAC introduces an undesirable pole in the system transfer function. This pole limits the control bandwidth and overall regulation performance. An adaptive control scheme was developed to address this issue [2], where the DAC over-sampling rate and filter corner frequency are varied in real-time to achieve both low steady-state power consumption and fast transient response. In this work, a simple low-power DAC architecture was applied to the hybrid scheme for a synchronous buck converter IC, as shown in Fig. 1. The IC includes the control circuits, as well as a segmented power-stage [6] for improving light-load efficiency. In this work, the aim is to eliminate the main shortcomings of the previous $\Delta\Sigma$ DAC approach, namely the bandwidth restriction imposed by the DAC's low-pass filter, while at the same time generating a high resolution voltage reference for the current-loop. In addition, the demonstrated architecture does not require expensive digital signal processing or high-frequency clocks beyond the switching frequency, f_s.

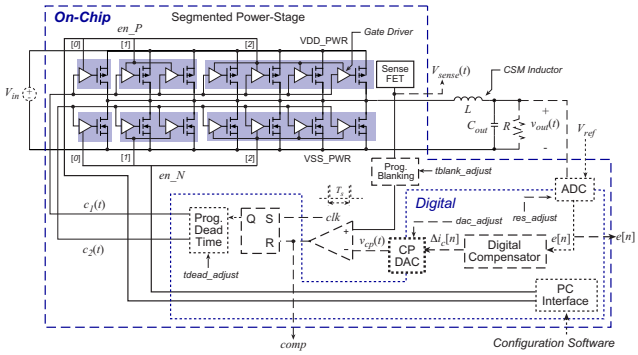


Fig. 1. Simplified architecture of the integrated dc-dc converter with a hybrid CPM control scheme and the novel DAC.

This paper is organized as follows. The limit-cycle phenomenon, which may occur in hybrid peak current-mode control, is examined in Section II, leading to minimum resolution requirements on the DAC. The proposed low-power DAC architecture for linking the voltage and current loops is presented in Section III and experimental results for the silicon prototype are reported in Section IV.

II. Minimum DAC Resolution: DC Limit-Cycle Condition

The two quantizers (the DAC and the ADC) in the feedback loop make hybrid CPM prone to limit-cycle oscillations, a phenomenon which is well understood in digital voltage-mode controllers [7], [8]. In this Section, the analysis method presented in [7] is extended for the hybrid CPM. The DC output voltage change caused by changing the DAC input by one LSB, ΔV_{dac}, is given by

$$\Delta V_{dac} = \frac{G_{vc}(s=0)}{K_s} \cdot \frac{V_r}{2^M} = \frac{G_{vc0}}{K_s} \cdot \frac{V_r}{2^M} \qquad (1)$$

* Olivier Trescases is currently with the High-Integration Group in the Automotive Power Department, Infineon Technologies AG Siemenstrasse 2, Villach, A9500, Austria.
Nabeel Rahman is currently working for On Semiconductor 5005 E.Mcdowell Road, Pheonix, AZ, USA.

978-1-4244-1668-4/08/$25.00 ©2008 IEEE

where M is the DAC resolution, K_s is the current-sensing gain, V_r is the DAC reference voltage and G_{vc0} is the CPM dc control-to-output gain. The DC condition to avoid limit-cycles and the resulting minimum DAC resolution are given by (2) and (3), respectively.

$$\Delta V_{dac} = \frac{G_{vc0}}{K_s} \cdot \frac{V_r}{2^M} < \Delta V_{adc} \quad (2)$$

$$M > \left\lceil \log_2 \left(\frac{V_r}{\Delta V_{adc} K_s} \cdot G_{vc0} \right) \right\rceil \quad (3)$$

Without slope compensation, the peak inductor current is ideally equal to the current command $i_c[n]$, which gives $I_{load} + \frac{\Delta i_L}{2} = i_c$. Eliminating Δi_L and using $I_{load} = v_{out}/R_{load}$ gives the following quadratic equation:

$$\frac{-1}{2Lf_s V_{in}} v_{out}^2 + \left(\frac{1}{R_{load}} + \frac{1}{2Lf_s} \right) v_{out} - I_c = 0 \quad (4)$$

The current-loop gain, G_{vc0} is obtained by solving (4) for v_{out} and differentiating the result with respect to i_c:

$$G_{vc0} = \frac{\partial v_{out}}{\partial i_c} = \left(\left(\frac{1}{R_{load}} + \frac{1}{2Lf_s} \right)^2 - \frac{2I_c}{Lf_s V_{in}} \right)^{-\frac{1}{2}} \quad (5)$$

The highest and worst-case gain occurs for $I_{load} = 0$, $R_{load} \to \infty$ and $I_c = \Delta i_L/2$. Eliminating I_c in (5) gives

$$G_{vc0}(R_{load} \to \infty) = \frac{2Lf_s}{\sqrt{1 - 4\frac{V_{out}}{V_{in}} \left(1 - \frac{V_{out}}{V_{in}}\right)}} \quad (6)$$

By combining (6) and (3), the worst-case minimum DAC resolution is given by

$$M > \left\lceil \log_2 \left(\frac{V_r}{\Delta V_{adc} K_s} \cdot \frac{2Lf_s}{\sqrt{1 - 4\frac{V_{out}}{V_{in}} \left(1 - \frac{V_{out}}{V_{in}}\right)}} \right) \right\rceil \quad (7)$$

The output voltage versus current command, obtained from solving (4), is shown in Fig. 2(a) for different values of R_{load} and for the parameters given in Table I. The current-loop gain from (5) is plotted in Fig. 2(b). In both cases, the duty-cycle limit of $D = 0.5$ is shown by the dashed line, beyond which the current loop is inherently unstable.

The M predicted by (7), which is only valid if slope compensation is not used, is quite conservative, since the system may be designed to operate in pulse-frequency modulation (PFM) or discontinuous current-mode (DCM) at light-loads. In that case, the gain G_{vc0} in (2) should be calculated from (5) at the maximum load resistance $R_{load,max}$, leading to a lower value for M compared to (7). The result is shown in Fig. 3, for the parameters of Table I. The high control-to-output gain in CPM results in a higher resolution requirement for the DAC, compared to the DPWM in voltage-mode control. It can be seen, that unlike voltage-mode control in continuous-conduction mode (CCM), the minimum resolution is highly load dependent. The resolution requirements in DCM mode are analyzed in [9]. The presence of limit-cycle oscillations in the

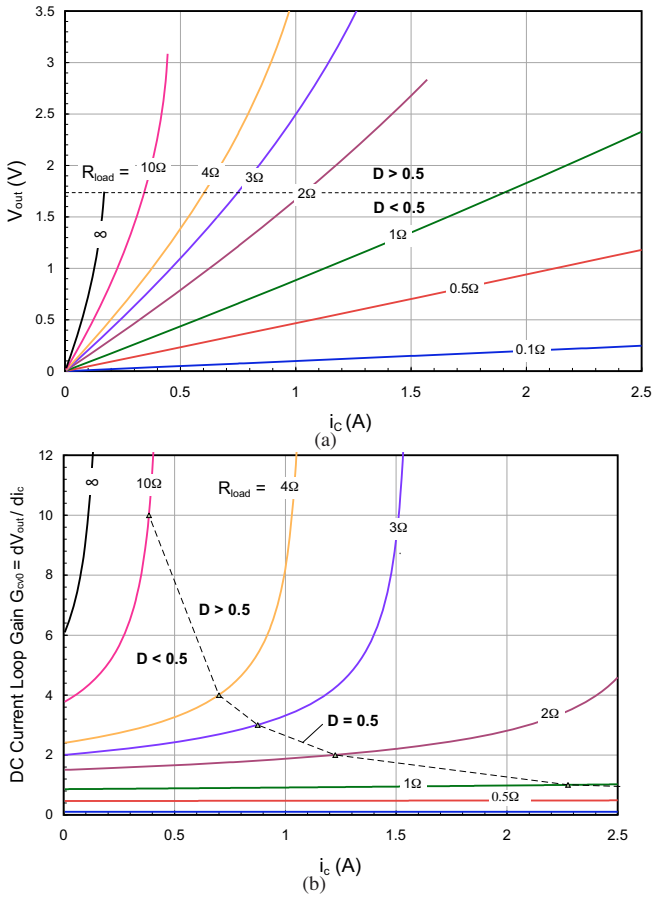


Fig. 2. (a) Output voltage versus current-command and (b) small-signal gain for different values of R_{load}.

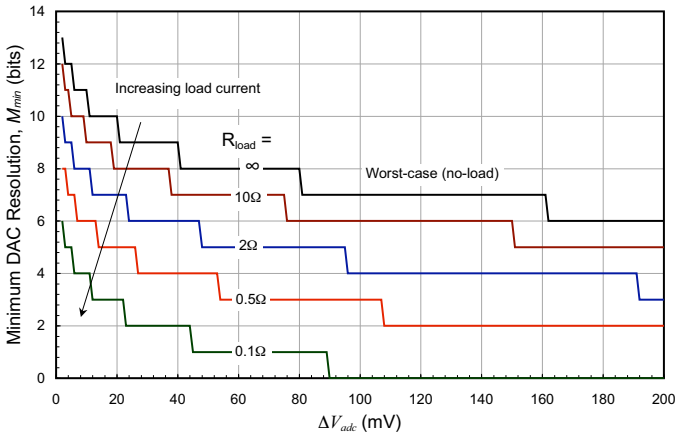


Fig. 3. Minimum DAC resolution for different values of R_{load}.

inductor current is confirmed experimentally in the load-step response of Fig. 4(a). For a fixed DAC resolution, reducing the sensing gain K_s by 2.5× leads to visible limit-cycle oscillations in Fig. 4(b), while the response-time is reduced

due to the increase in the DC current-loop gain G_{v0}.

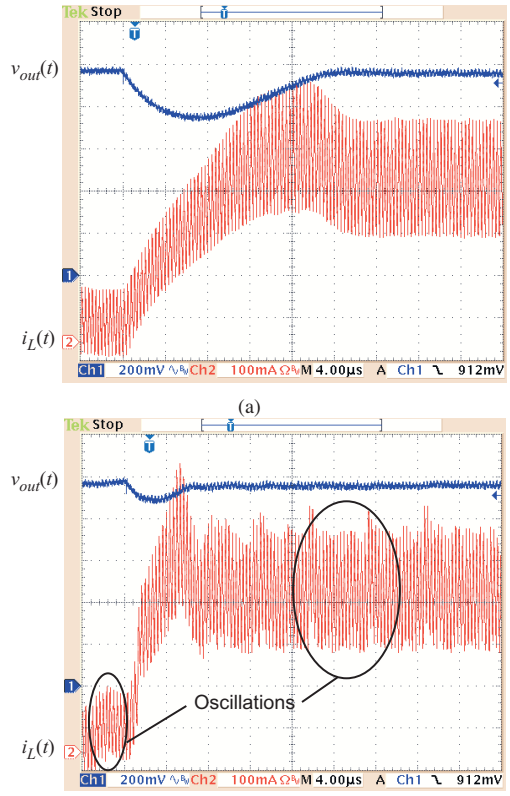


Fig. 4. Load-step response showing the effect of decreasing K_s by 2.5× from (a) to (b).

III. Low-Power Charge-Pump DAC

In CPM, the buck converter can be approximated by a first-order system at low frequencies [10] and a simple digital compensator can be used for the voltage loop, where the difference equation is given by

$$\Delta i_c[n] = i_c[n] - i_c[n-1] = C_0 e[n] - C_1 e[n-1] \quad (8)$$

where $e[n]$ is the digital error and $C_0 - 1$ are the compensation coefficients. A specialized DAC architecture was developed by using the differential nature of (8), where the input to the DAC consists only of the *change* in the current command, $\Delta i_c[n]$.

The CP-DAC functions as a delay-to-voltage converter, as shown in Fig. 5. The analog current-command, $v_{cp}(t)$ is stored on the charge-pump capacitor C_{cp}, hence the actual digital current command $i_c[n]$ is not explicitly stored in the digital domain. The 8-bit differential current-command $\Delta i_c[n]$ is decoded into three components by the CP-DAC decoder block: a sign-bit, *sign*, a 4-bit delay select code, *DT<3:0>* and a 4-bit current-select code *I_SEL<3:0>*. The switches M_1 and M_4 are activated by the charge-pump logic block for a duration of Δt_{dac}. The transistors M_2 and M_3 mirror the current generated in the programmable current-sink. For a given differential current-command $\Delta i_c[n]$, the change in $v_{cp}(t)$ is given by

$$\Delta V_{cp} = \pm \frac{I_{cp} \Delta t_{dac}}{C_{cp}} = \frac{(I\_SEL \cdot I_{cp0})(DT \cdot \Delta t_{dac0})}{C_{cp}} \quad (9)$$

where the control parameters I_{cp} and Δt_{dac} are proportional to *I_SEL<3:0>* and *DT<3:0>*, respectively.

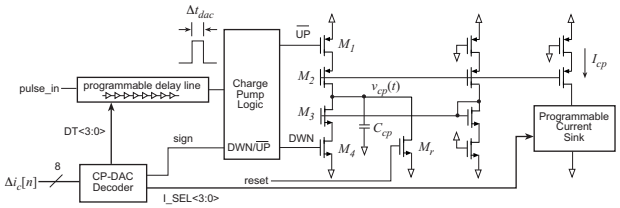


Fig. 5. Charge-pump DAC architecture.

The minimum charge-pump time-interval and current are denoted Δt_{dac0} and I_{cp0}, respectively. The value of Δt_{dac0} is fixed by the delay-line bias current, while I_{cp0} can be adjusted digitally to tune the DAC's gain. The CP-DAC decoder's digital input/output characteristic that results in a linear relationship between $\Delta i_c[n]$ and ΔV_{cp} is shown in Fig. 6(a). Only one of the four current branches selected by *I_SEL<3:0>* is used at a time. The resulting product of *I_SEL<3:0>* and *DT<3:0>* is linear, as shown in Fig. 6(b). The staircase-like function has a quantization error which grows with $|\Delta i_c[n]|$, thereby introducing a slight non-linearity into the system. This quantization error has a very limited effect on the system's dynamic behavior, since the error is inherently reduced as $|\Delta i_c[n]|$ approaches zero, and $v_{out}(t)$ approaches the zero-error bin. The CP-DAC architecture also has a guaranteed monotonic characteristic, since the sign of $\Delta i_c[n]$ determines the polarity of the change in $v_{cp}(t)$. Using an 8-bit, 2's complement representation for $\Delta i_c[n]$, this simple decoding scheme allows $|\Delta V_{cp}|$ to range from $I_{cp0} \cdot \Delta t_{dac0}$ to $15 \times 8 = 120 \times I_{cp0} \cdot \Delta t_{dac0}$.

One of the most attractive feature of the CP-DAC is its ability to achieve small changes in $v_{cp}(t)$, without resorting to high-resolution digital hardware. The limit-cycle expression from (2) can be re-written for the CP-DAC:

$$\Delta V_{cp,min} = I_{cp0} \cdot \Delta t_{dac0} < \frac{\Delta V_{adc} K_s}{G_{vc0}} \quad (10)$$

The condition given by (10) provides a guideline for choosing I_{cp0} and Δt_{dac0}, for a given ADC quantization of ΔV_{adc}, and current-loop gain G_{vc0} from (6).

The simulated step-response for the closed-loop system is shown in Fig. 7. The accurate system model was generated in Simulink, based on the extracted parameters of the power-stage and the mixed-signal blocks, as well as the finite precision of the digital registers in the PI compensator. Matlab/Simulink was used to model the power-stage components. The output voltage is regulated back into the zero-error bin within 4 μs for a load-step of 50-250 mA. The differential current-command

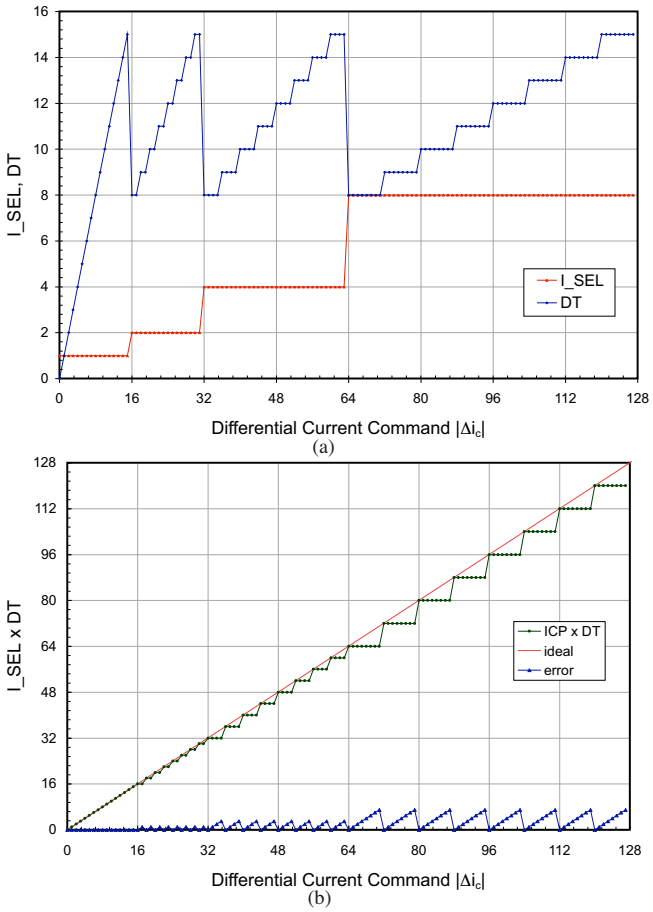


Fig. 6. (a) Input/output characteristic of the CP-DAC decoder; (b) Product of *I_SEL<3:0>×DT<3:0>*.

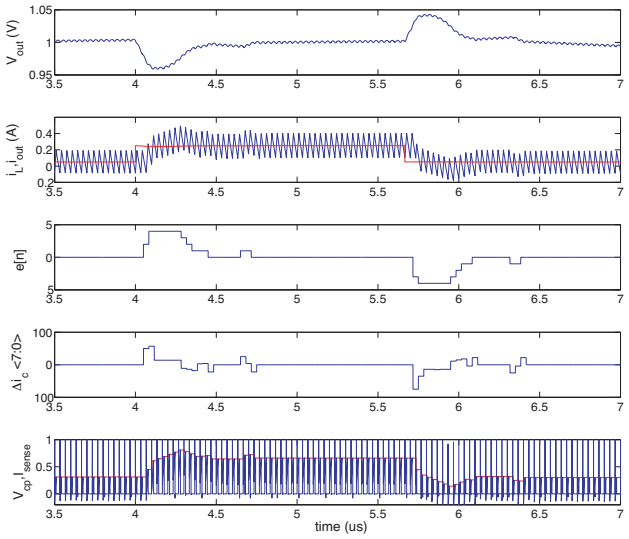
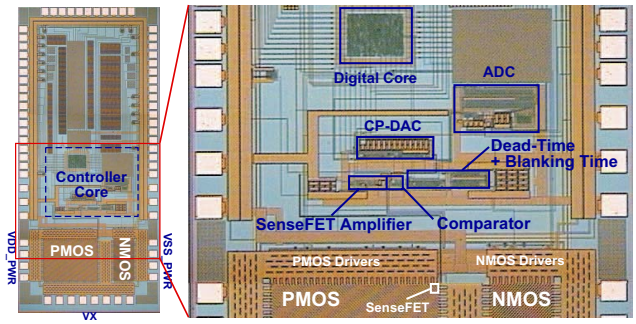


Fig. 7. Simulated response of the closed-loop system for a 50-250 mA load step.



(a)

Fig. 8. Die photo of the hybrid CPM IC fabricated in a 0.18 μm CMOS process.

($\Delta i_c[n]$) waveform shows that the CP-DAC immediately adjusts the peak inductor current following the load-step. The system parameters are summarized in Table I.

IV. Experimental Results

The converter shown in Fig. 1 includes a segmented power-stage similar to [11] for improved light-load efficiency. It was fabricated in a 0.18 μm CMOS process with 5 V transistors, which are sufficient to accommodate the single-cell Lithium-Ion voltage range of 2.7 V to 4.2 V. The chip micrograph is shown in Fig. 8. The die measures 2.7 $\times$ 1.25 mm^2, while the total active area for the controller (excluding the power-stage) is only 0.077 mm^2. The total controller current-draw, which is dominated by the on-chip senseFET current-sensor, is below 250 μA at I_{out}= 50 mA.

A. Charge-Pump DAC Measurement

The CP-DAC output, $v_{cp}(t)$ is a sensitive analog node that is not accessible off-chip. The DAC was characterized by connecting an external ramp to the $V_{sense}(t)$ node, while measuring the pulse-width of the comparator output. After discharging or pre-charging C_{cp}, the CP-DAC digital input was held constant at $\Delta i_c[n]$. This causes the comparator output pulse-width to increase or decrease every cycle, depending on the sign of $\Delta i_c[n]$. The ideal waveforms are shown in Fig. 9(a), where ΔV_{cp} can be estimated using (11) for $V_{ramp} >> \Delta V_{cp}$.

TABLE I
System Specifications

Specification	Value	Units
Input Voltage, V_{in}	2.7-4.2	V
CMOS Process (HV)	0.18	μm
Output Voltage, V_{out}	1	V
Rated Load, I_{load}	0.5	A
Filter, L	1	μH
Filter, C_{out}	4.7	μF
Switching Frequency, f_s	3	MHz
ADC Error Bin (zero error), ΔV_{adc}	13	mV
ADC Error Bin (other bins), ΔV_{adc}	6	mV
DAC resolution, ΔV_{dac}	2.2	mV
Settling Time	< 4	μs

The measured comparator output is shown in Fig. 9(b) for $\Delta i_c[n] < 0$.

$$\Delta V_{cp} \approx \frac{V_{ramp}}{f_{ramp} t_{sat}} \tag{11}$$

The measured values for ΔV_{cp} versus *DT<3:0>*, based on (11) are shown in Fig. 10(a). The minimum value of ΔV_{cp} = 2.11 mV occurs at *DT<3:0>*=0001, *ICP<3:0>*=0001 and for the tuning parameter*DT_TUNE<3:0>*=1111. If a full-range flash DAC architecture were used to achieve the same ΔV_{cp}, a resolution of 10 bits would be required with V_r = 1.8 V. The extracted ΔV_{cp} has a linear relationship with *ICP<3:0>*, as shown in Fig. 10(b). As mentioned in Section III, the CP-DAC has a guaranteed monotonic behaviour. The leakage on the charge-pump capacitor, due to capacitive coupling, was investigated by pre-charging $v_{cp}(t)$ and setting *ICP<3:0>=DT<3:0>*=0; The resulting extracted $v_{cp}(t)$ is shown in Fig. 11 for two different pre-charge values. In both cases, $v_{cp}(t)$ drops by only $\approx$ 50 μV per clock cycle. The compensator is easily capable of compensating for this effect by periodically increasing $v_{cp}(t)$ when the accumulated leakage causes $v_{out}(t)$ to exit the zero-error bin.

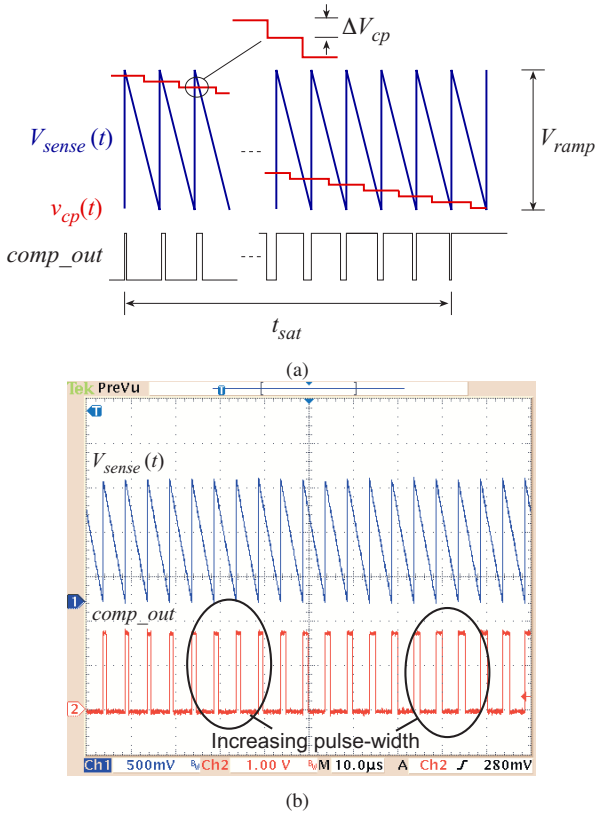


Fig. 9. (a) Characterization of the CP-DAC. (b) Measured ramp-down of the CP-DAC output.

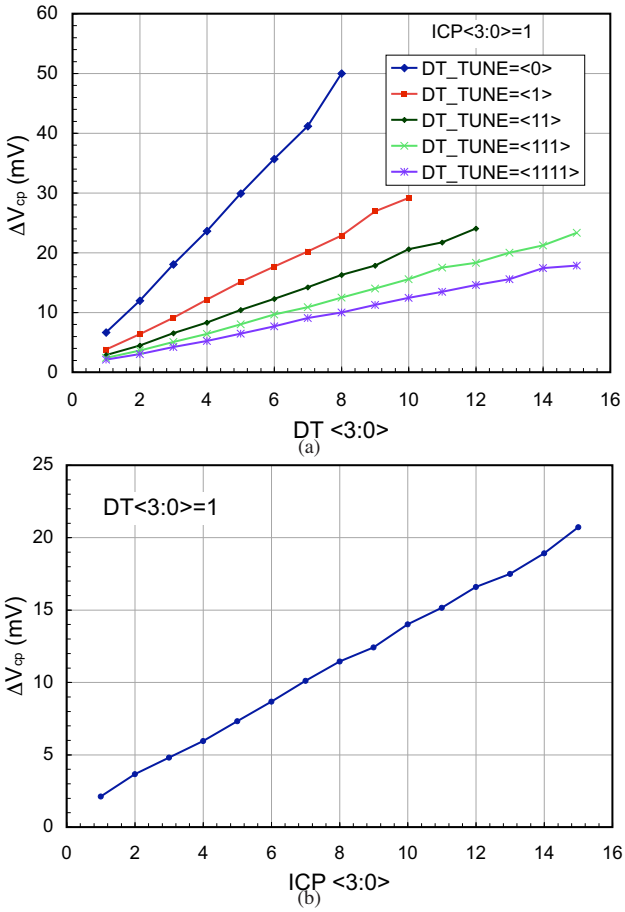


Fig. 10. Measured (a) ΔV_{cp} versus *DT<3:0>* for different tuning values of *DT_TUNE<3:0>*. (b) ΔV_{cp} versus *ICP<3:0>*.

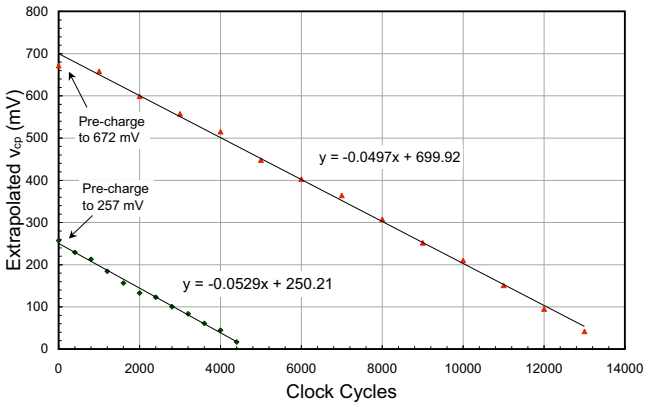


Fig. 11. Measured leakage of $v_{cp}(t)$ due to charge coupling. The extracted slope is -50 μV/clock cycle.

B. Analog-to-Digital Converter

The on-chip delay-line ADC quantizes the difference between $v_{out}(t)$ and V_{ref}, with a digital error range of -4< $e[n]$ <4. The delay-line ADC [12]–[14] has several advantages over the comparator-based FLASH ADCs. These include improved noise-immunity due to inherent averaging, lack of sample-and-hold requirement, flexible choice of conversion-time and predominantly digital architecture [15]. The ADC used in this work was originally implemented in [16], for a

voltage-mode controller application.

The measured and over-lapped transfer characteristic of the ADC is shown in Fig. 12 for different values of V_{ref}. The ADC functions correctly for V_{ref} down to 0.2 V. The ADC has two resolution settings, where the size of the quantization bins (apart from the zero-error bin) can be controlled. The zero-error voltage bin ΔV_{adc} varies from 13 mV to 15 mV for 0.2 V $< V_{ref} <$ 1.8 V, while the other voltage bins correspond to 6 mV. An average conversion time of 162 ns is achieved, with less then 2 % variation over the reference voltage range.

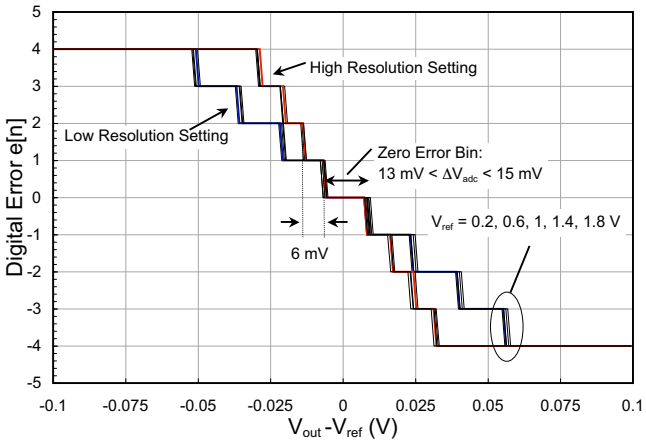


Fig. 12. Measured and overlapped ADC characteristics for 0.2 V $< V_{ref} <$ 1.8 V, for both ADC resolution settings.

C. Power-Stage

The segmented power-stage shown in Fig. 1 includes a pMOS high-side switch and an nMOS low-side switch. Each switch is divided into 7 identical segments, with dedicated gate-drivers whose inputs are connected in a binary weighted fashion. The power-stage uses a hybrid-waffle layout pattern, where the source and drain cells are arranged in checker-board structure with the associated routing channels (drain and source) oriented at 45 degrees, as in the standard waffle-type layout [17], [18]. The main difference lies in the use of a cell-pitch that intentionally exceeds the minimum spacing required to fit a single diffusion contact, as shown in Fig. 13, where the cell pitch is exaggerated. This flexible choice of cell pitch W_c allows the relative area allocation for contact and active area to be optimized. The power-stage characteristics are given in Table II. The efficiency of the power-stage was measured at f_s = 4 MHz and with L = 2 μH, for comparison with the 1st generation power-stage in [11]. The result is shown in Fig. 14. The efficiency is shown for different values of the 3-bit segment enable codes en_P and en_N. The peak efficiency for different input voltages is shown in Table II. The real-time control of the segmented power-stage for efficiency optimization is beyond the scope of this paper. The techniques described in [11] can easily be adapted for current-mode control.

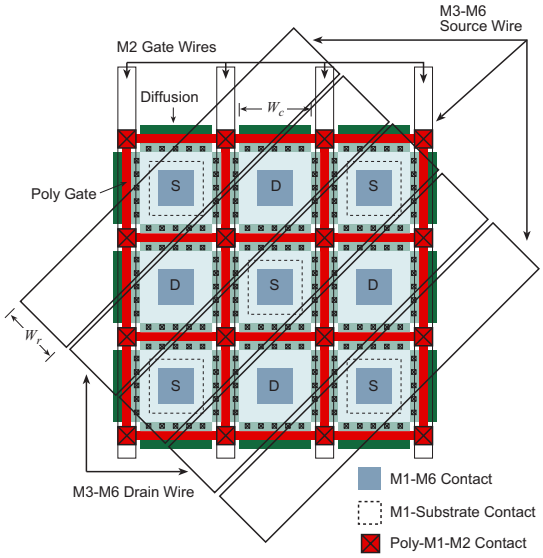


Fig. 13. Illustration of the basic cell for the power MOSFET hybrid-waffle layout structure.

TABLE II
POWER-STAGE PERFORMANCE

	Switch		Units	Condition
	pMOS	nMOS		(V_{in} = 3.6 V) (V_{out} = 1.8 V)
CMOS Process	0.18 μm HV			
Breakdown Voltage	>5		V	
Layout Pattern	Hybrid Waffle			
Total Width, W	34.6	13	mm	
Drawn Length, L	0.5	0.6	μm	
Active Area, A	0.200	0.074	mm^2	
R_{ch}	208	152	mΩ	Simulated
Q_g	213	78.2	pC	Simulated I_D = 500 mA
FOM$_1$	44.3	11.88	nC·mΩ	$Q_{gate} \cdot R_{ch}$
R_{on}	366	310	mΩ	Measured Packaged
P_{gate}	3.43	1.56	mW	Measured
				f_s = 4MHz
Specific R_{on}	73.2	22.94	mΩ mm^2	Packaged
FOM$_3$	0.314	0.121	pJ·mΩ	$\frac{P_g}{f_s} \cdot R_{on}$
Peak Efficiency, η	91.3		%	V_{in} = 2.7 V
	88.8		%	V_{in} = 3.6 V
	87.8		%	V_{in} = 4.2 V

D. Closed-Loop Response

The closed-loop system's response to a 45 mA - 250 mA load-step at V_{out} = 1 V, f_s = 3 MHz is shown in Fig. 15. The controller has a fast settling-time of t_{res} = 4 μs and a voltage deviation of only $\Delta V_{res} <$ 50 mV at f_s = 3 MHz. This transient behavior is nearly identical to the system simulation shown in Fig. 7. The rapid control of the inductor current is apparent from $V_{sense}(t)$ waveform, which is the output of the on-chip high-bandwidth current-sensor.

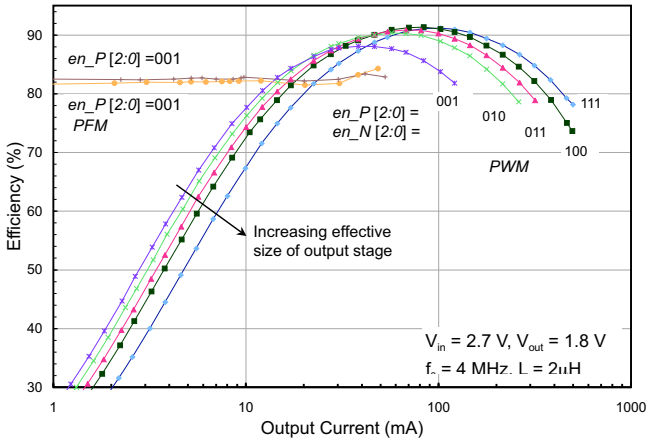


Fig. 14. Measured efficiency versus load current at V_{in} = 2.7 V, with different segment enable codes and modes.

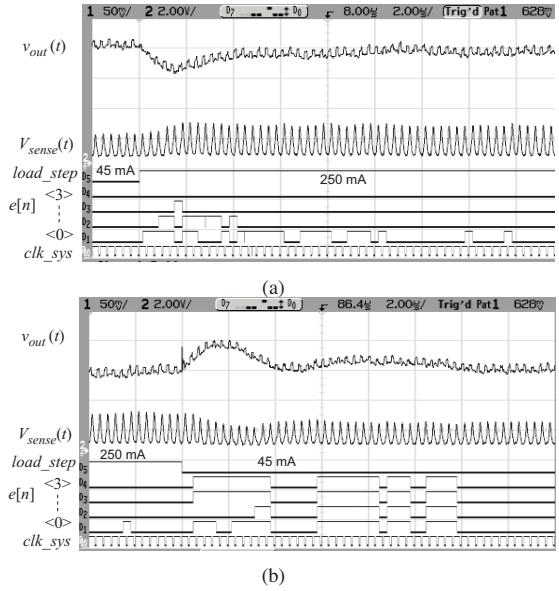


Fig. 15. (a) Light-to-heavy and (b) heavy-to-light load-step response. Ch-1: $v_{out}(t)$, 50 mV/div. Ch-2: $V_{sense}(t)$, 2V/div. Time scale: 2 μs/div.

V. Conclusion

A silicon implementation of hybrid peak current-mode control was described. The main contribution of this work is the novel DAC architecture, which was developed specifically to achieve fast transient-response without needing clock frequencies beyond f_s, or expensive signal processing. The charge-pump (CP) DAC is capable of rapidly increasing the current-command in a single-cycle during load-steps. The proposed DAC is essentially idle during steady-state and hence has minimal power-consumption. The hybrid architecture architecture is compatible to more advanced digital compensation schemes for the voltage loop, leading to improved transient response. Further work is required to incorporate slope-compensation for increasing the operating range.

VI. Acknowledgments

The authors would like to thank NSERC, CMC, Auto21, U of T open fellowship, and Fuji Electric Advanced Technology Co. Ltd. for their support. Haruhiko Nishio, Masahiro Sasaki, Tetsuya Kawashima and Guowen Wei provided valuable support, technical guidance and dedication throughout the project. Zdravko Lukić developed the original ADC design that was adapted for this work.

References

[1] S. Saggini and M. Ghioni, "An innovative digital control architecture for low-voltage high-current DC-DC converters with tight load regulation," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 210–218, January 2004.

[2] O. Trescases, Z. Lukić, W.-T. Ng, and A. Prodić, "A low power mixed-signal current-mode DC-DC converter using a one-bit delta sigma DAC," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2006, pp. 700–704.

[3] H. Peng and D. Maksimović, "Digital current-mode controller for DC-DC converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2005, pp. 899–905.

[4] S. Chattopadhyay and S. Das, "A digital current-mode control technique for dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1718–1726, 2006.

[5] Y.-S. Jung, "Small-signal model-based design of digital currrent-mode control," *IEEE Proceedings on Electric Power Applications*, vol. 152, no. 4, 2005.

[6] R. Williams, W. Grabowski, A. Cowell, M. Darwish, and J. Berwick, "The dual-gate W-switched power MOSFET: a new concept for improving light load efficiency in DC/DC converters," in *Proc. IEEE International Symposium on Power Semiconductor Devices & ICs*, 1997, pp. 193–196.

[7] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Transactions on Power Electronic Circuits*, vol. 18, pp. 301–308, Jan 2003.

[8] H. Peng, A. Prodić, E. Alarcon, and D. Maksimović, "Modeling of quantization effects in digitally controlled DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208–209, 2007.

[9] J. Chen, M. Ribeiro, R. Payseo, D. Zhou, and J. Smith, "DPWM time resolution requirements for digitally controlled DC-DC converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2006, pp. 1127–1132.

[10] C. Deisch, "Simple switching control method changes power converter into a current source," in *Proc. IEEE Power Electronics Specialists Conference*, 1978, pp. 300–306.

[11] O. Trescases, W.-T. Ng, H. Nishio, E. Masaharum, and T. Kawashima, "A digitally controlled DC-DC converter module with a segmented output stage for optimized efficiency," in *Proc. IEEE International Symposium on Power Semiconductor Devices & ICs*, 2006, pp. 409–413.

[12] B. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, Jan 2003.

[13] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4-μA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," in *IEEE Journal of Solid-State Circuits*, vol. 39, 2004, pp. 2342–2348.

[14] M. Vincent and D. Maksimovic, "Matched delay-line voltage converter," US Patent 6958721, Oct. 2005.

[15] A. Parayandeh, "Programmable application specific ADC for digitally controlled switch-mode power supplies," Master's thesis, University of Toronto, 2006.

[16] Z. Lukić, "Sigma-delta controllers for 12 MHz DC-DC switch-mode power supplies," Master's thesis, University of Toronto, 2006.

[17] W. Wu, S. Lam, and M. Chan, "A wide-band T/R switch using enhanced compact waffle MOSFETs," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 287–289, 2006.

[18] S. Nassif-Khalil, S. Honarkhah, and C. Salama, "Low voltage CMOS compatible power MOSFET for on-chip DC/DC converters," in *Proc. IEEE International Symposium on Power Semiconductor Devices & ICs*, 2000, pp. 43–46.