Digitally Controlled Low-Power DC-DC Converter with Instantaneous On-Line Efficiency Optimization

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Abstract-**This paper introduces a digital controller and a segmented power stage that dynamically change mode of operation to maximize power processing efficiency when highly dynamic loads are supplied. The controller operates as a mixed-signal peak current program mode voltage regulator, where a digital current reference is created and used for the efficiency optimization. The losses of the power stage are minimized by combining power stage segmentation and gate swing variation. Based on the current reference, in each switching cycle, the optimal number of power switch segments and gate drive voltages are set through a sequence controller and a novel dual-output switch-capacitor circuit. The effectiveness of the system is verified on a 1.8 V, 5 W, 1 MHz buck converter prototype. The results show that the on-line optimization raises and flattens the efficiency curve and that, for dynamic loads, improves energy utilization by up to 20%.**

I. INTRODUCTION

Emerging digital controllers for low-power high-frequency switch-mode power supplies (SMPS) [1-10] enable wider use of efficiency optimization techniques. These techniques usually minimize converter losses under light and medium loads, as well as under other suboptimal conditions, where the efficiency of a converter is below its peak value. This efficiency improvement is especially important in portable applications, where the source of energy is limited, and the supplied devices operate in suboptimal regions over a long time [9].

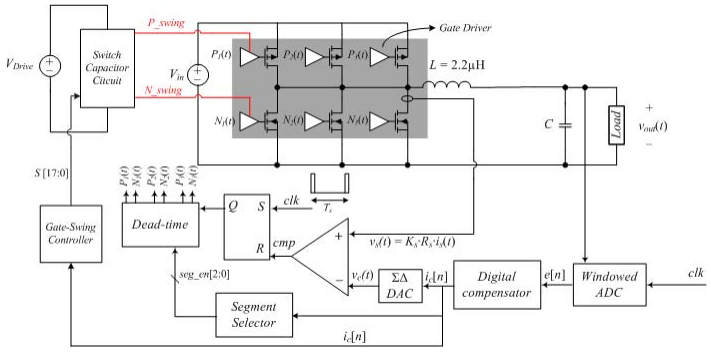


Fig.1.: Digitally controlled buck converter with instantaneous efficiency optimization.

In comparison with commonly used analog controllers, digital systems are better suited for the implementation of most efficiency optimization techniques. This is because these techniques often require flexible controllers that can dynamically change parameters such as switching frequency [11], non-overlapping times [12] or/and perform switching between pulse-frequency and pulse-width modes of operation [21]. Furthermore, some techniques also involve modification and dynamic reconfiguration of the power stage [13] and gate drive circuit [19]. To minimize the sum of conduction and switching losses using segmentation techniques in the power stage,[9]-[11], a power MOSFET and its gate driver are divided into smaller segments operating in parallel, as shown in Fig.1, and the number of active segments is dynamically changed, depending on the load conditions in the circuit. In the gate swing scaling techniques [19] by varying transistor's gate drive voltage, a trade off between its *Ron* resistance and the gate charge is performed in such a way that, for a given operating conditions, the total losses are minimized. Recent publications show implementation of most of previously mentioned techniques with digital controllers [8]-[12]. The controllers estimate the steady-state operating point and, accordingly, adjust the SMPS operation such that the efficiency is maximized.

Since the optimization algorithms rely on a relatively slow estimation, the benefit of these methods becomes limited in situations when the load changes frequently. Examples include numerous electronic loads such as signal processors, graphical cards, and displays. Their dynamic load behavior causes the SMPS to operate in suboptimal region most of the time.

Even more, in some cases, the optimization methods can become counterproductive resulting in efficiency degradation caused by the hardware overhead needed for the optimizer implementation. To minimize the reaction time of the optimizers, load predictive systems for digital loads were proposed [9]. By communicating with the load and analyzing its processed data stream, the system predicts the load current and, consequently, adjusts the power stage parameters.

The predictive optimizers significantly improve the efficiency under dynamic loads but still result in suboptimal operation, due to systems delay and often unknown relation between the processed data stream and the current data taken

by the load. The primary objective of this paper is to present a digitally controlled SMPS that provides instantaneous efficiency optimization, and as such is well suited for operation with highly dynamic load. The SMPS of Fig.1 does not require communication with the load nor any prior knowledge about its behavior. Based on the inherently available information about the peak current value, in each switching cycle, the system sets the mode of operation such that the sum of conduction and switching losses is minimized.

II. System Description and Principle of Operation

Fig.1 shows the architecture of the system implemented in this work. The controller operates as a modification of mixed-signal peak current programmed mode controller [15]-[18], where the voltage loop is digital and the internal current loop is implemented in analog manner. The output voltage error is measured and converted into its digital equivalent $e[n]$ with a windowed analog-to-digital converter (ADC) [16]. Based on the error signal, a digital compensator creates current reference $i_c[n]$. This value is passed to a simple ΣΔ digital-to-analog converter (DAC) [16], which sets the limit for the peak inductor current during each switching cycle and is also used in the optimization process.

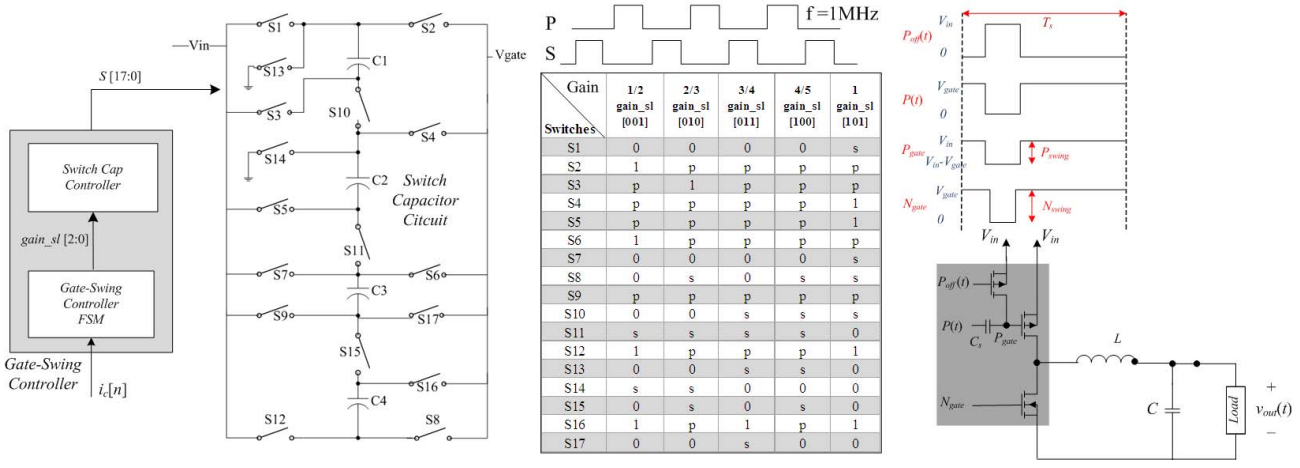
Three unique modifications of this structure are described in the following sections and illustrated in Figs. 1 and 2.

A. Power Stage

In this converter, benefits of two known optimization techniques are combined to obtain a fairly simple implementation and high efficiency over the full range of operation. As it is described in the following section, to obtain high efficiency over the full range using segmentation only, a relatively large number of segments or a binary scaling of the transistors is required [8]. The consequence is that, in on-chip implementation, a fairly complicated layout of the transistors and gate drive circuit increasing overall size of the power stage is needed. Even a bigger problem is that the parasitic components of the layout can cause significant delays of some segments, unequal current distribution during switching transients, and consequent current breakdown of the circuit under heavy load conditions [13]. On the other side, the sole implementation of the gate swing technique is not optimal either. It will require only one large pair of power switchers, but the obstacle is that a relatively large and powerful variable supply voltage circuit is needed to provide sufficient gate charge for the power MOSFETs. In the implementation shown in this paper, the benefits of both methods are utilized. As shown in Fig.1, the power stage is created of only three segments and the gate voltage of one segment is varied. As a result the power stage implementation is significantly simplified and, at the same time, the use of a small gate-voltage supply circuit is allowed. At heavier loads two or three transistors of the segmented stage are active. At lighter loads only one transistor is active and its gate voltage is modified.

B. Dual output switch-capacitor (SC) circuit

To implement the gate-voltage swing optimization method, a solution that allows changing the gate-drive voltage, V_{gate} , in a certain range without degrading efficiency is required . To maximize the efficiency, we propose a switch-capacitor (SC) circuit that only operates at certain discrete voltages, and supplies the smallest segment in the power-stage. Fig.2.b shows the circuit diagram of the SC circuit and the switch-configurations for generating different gate-drive voltages. The SC circuit is controlled by the gate swing controller block shown in Fig2.a, which consists of the *gate swing controller FSM* (Finite-State-Machine) and the *switch cap Controller* blocks. Based on the value of $i_c[n]$ the FSM block sets a 3-bit *gain_sl* signal that is used by the *switch cap Controller* block to select the respective combination of switches $S[17:0]$. In



Switches \ Gain	1/2 gain_sl [001]	2/3 gain_sl [010]	3/4 gain_sl [011]	4/5 gain_sl [100]	1 gain_sl [101]
S1	0	0	0	0	s
S2	1	p	p	p	p
S3	p	1	p	p	p
S4	p	p	p	p	1
S5	p	p	p	p	1
S6	1	p	p	p	p
S7	0	0	0	0	s
S8	0	s	0	s	s
S9	p	p	p	p	p
S10	0	0	s	s	s
S11	s	s	s	s	0
S12	1	p	p	p	1
S13	0	0	s	s	0
S14	s	s	0	0	0
S15	0	s	0	s	0
S16	1	p	1	p	1
S17	0	0	s	0	0

Fig.2 from left (a) Gate-Swing Controller Architecture (b) Switch-Capacitor Circuit diagram and switch-configurations for generating different gate-drive voltages , c) circuit modifications and waveforms for simultaneous gate-voltage swing scaling on both power MOSFETs.

order to adjust the gate voltage swing simultaneously on both MOSFETs , generally a separate switch-capacitor circuit is required for the PMOS transistor increasing the size and cost of the power stage considerably. To avoid this, a single switch-capacitor circuit is used in this work by modifying the power-stage as shown in Fig 2.c. As the associated waveforms show, an additional PMOS transistor Q_1 is used, to pull P_{gate} to V_{in} and turn the PMOS switch off during the second subinterval. During the first subinterval the gate-driver signal $P(t)$ with voltage swing of V_{gate}, is ac-coupled to the gate of the PMOS switch using capacitor C_x, therefore adjusting the gate voltage swing to V_{in} - V_{gate} as desired. The dual output switch-capacitor circuit proposed in this work allows for gate voltage swing scaling of both PMOS and NMOS power switches without requiring a large circuit therefore reducing the size and cost of the SMPS.

C. *Controller*

The controller implementation of Fig.1 significantly differs from traditional steady-state estimator-based controllers [10]. In this case, the current reference $i_c[n]$ is used not only for the output voltage regulation, but also as the signal for governing on-line optimization. Based on $i_c[n]$ value *gate swing controller* and *segment selector* configure the power stage so that for a given peak current the total losses are minimized.

III. Efficiency Optimization and Mode Selection Criteria

This section briefly reviews losses in power MOSFETs and describes criteria used for the efficiency optimization The dominant sources of losses in high frequency SMPS are gate-drive and conduction losses associated with power MOSFETs[10-14]. The conduction loss can be approximated with the following equation [10,14]

$$P_{cond} = i^2_{rms,P} \times R_{dson,P} + i^2_{rms,N} \times R_{dson,N} \qquad (1)$$

Where $R_{dson,P}$ and $R_{dson,N}$ are PMOS and NMOS on-resistances respectively. Ignoring the interconnect resistance, the R_{dson} of a segmented power stage having equally sized transistors can be modeled as

$$R_{dson} = \frac{R_{ds0}}{K(V_g - V_{th})} \qquad (2)$$

where R_{ds0} is defined by process parameters and width of one segment, K is number of segments in power stage, V_g is the gate-voltage swing of the MOSFET and V_{th} is the device threshold voltage. The gate drive losses can be described with the following equation [14]

$$P_g = K(Q_{g,N} + Q_{g,P})V_g f_s = K(C_{g,N} + C_{g,P})V_g^2 f_s \qquad (3)$$

,where $C_{g,P}$ and $C_{g,N}$ are PMOS and NMOS gate capacitances associated with charging and discharging the MOSFETs in one segment. For a given process technology the product of gate charge and on-resistance is fixed. Therefore to improve efficiency over the load range, the number of segments in the power stage and the gate drive voltage can be changed to continuously optimize the trade-off between the conduction losses and gate drive losses. To determine the optimal operating sequence, for each load condition, the efficiency of the system is modeled and shown in Fig.3. As discussed above, the trade-off between the gate-drive and conduction losses can be optimized by changing the gate voltage swing and number of segments at different output currents, as shown in Figs.3.a and 3.b. For the load current range of 100mA-1A, Fig3.a gives the current threshold values for scaling the gate-voltage swings in order to optimize the efficiency as shown in Fig3.c. For the load current range above 1A , Fig3.b gives the current threshold values for adjusting the number of segment in order to achieve the optimized curve shown in Fig3.c. The threshold values are stored in gate-swing and segment controllers. Fig3.c demonstrates that combining both efficiency techniques will result in a far better efficiency improvement over the entire load range.

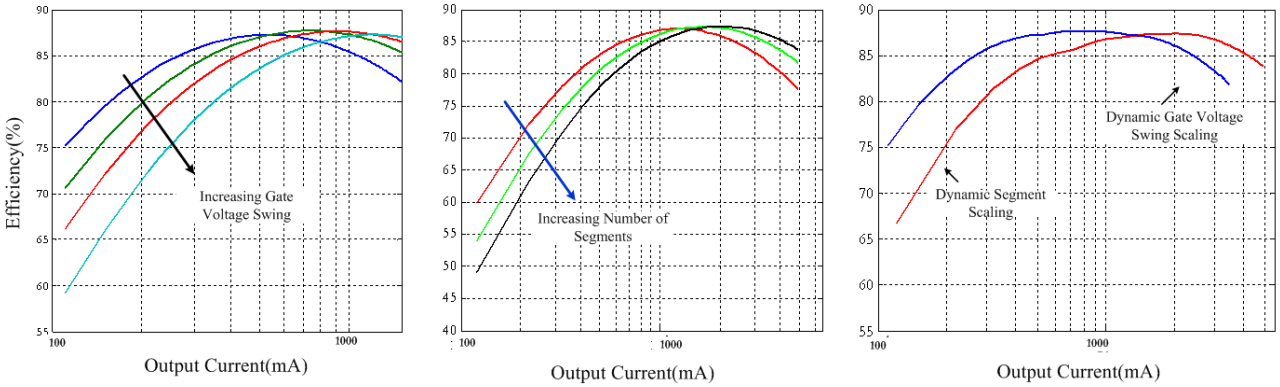


Fig3. a) Efficiency curves as the gate-voltage swing increases, b) Efficiency curves as the number of segments increase c)Efficiency optimization that can be achieved by the combination of two methods.

IV. Experimental Results

Based on the block diagram of Fig.1 an experimental system was build. The 5V-1.8V, 3 W converter consists of three segments with L = 2.2 µH, C = 47 µF, and f_{sw} = 1 MHz. The ADC and programmable reference voltage were implemented on an application specific integrated circuit and previously discussed in [16]. The controller including the ΣΔ DAC is implemented on an FPGA board with the exception of ΣΔ DAC filter and the comparator.

To verify the effectiveness of the system, two sets of experiments are performed. The efficiency of the optimized power stage is compared with the non-optimized power stage as well as with a stage utilizing steady-state estimation-based optimizer [10].

A. *Steady state efficiency improvements*

Fig.4 shows the steady-state efficiency improvements achieved with using the optimization method discussed in this

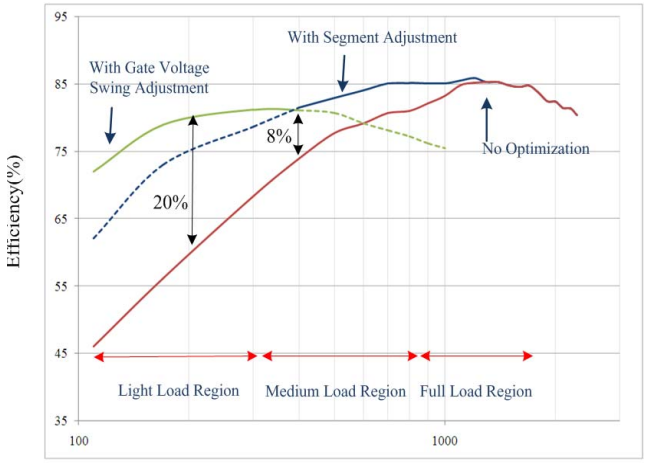


Fig.4. : Efficiency improvements with the optimization controller presented here.

paper. In the light load region, compared to the non-optimized operation the efficiency is improved by as much as 20% using gate-voltage swing scaling. Additionally, in the medium range, where segments adjustment is implemented, the efficiency is improved by 8%. Fig.4. also shows that combing the two methods described in this paper results in improved efficiency compared to implementing only one method.

B. *Dynamic Behavior*

Fig.5 shows the dynamic response of the converter with segmented operation. Upon a load transient, the controller adjusts the segment configuration signal *seg_en*[*n*] in accordance with the change of the current reference $i_c[n]$, shown at the output of Σ-Δ DAC as $v_c(t)$. Fig.6 shows the transient response of the converter with gate-swing scaling operation. As the load changes from 500mA to 1A, the gate

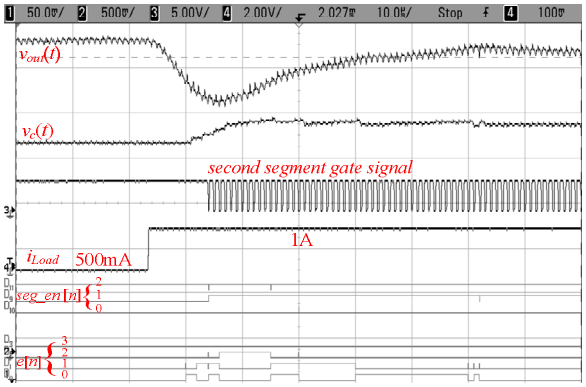


Fig.5: Dynamic response with segmented operation. Ch1: Output converter voltage (50mV/div); Ch2: analog current command (500mV/div); Ch3: Second Segment gate signal (5V/div) ; Ch4: load step command; D0-D3: ADC error e[n]; D9-D11: Segment Enable signal; Time scale is 10µs/div.

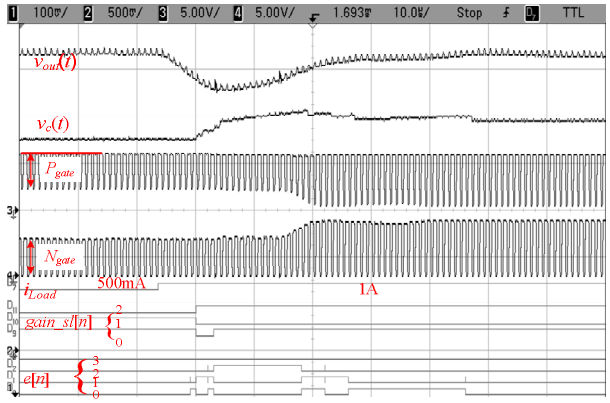


Fig.6.: Dynamic response with gate-swing scaling operation. Ch1: Output converter voltage (100mV/div); Ch2: analog current command; (500mV/div); Ch3: PMOS gate-swing voltage (5V/div) ; Ch4: NMOS gate-swing voltage(5V/div); D7: load step; D0-D3: ADC error, e[n];D9-D11:SC gain select signal; Time scale is 10µs/div.

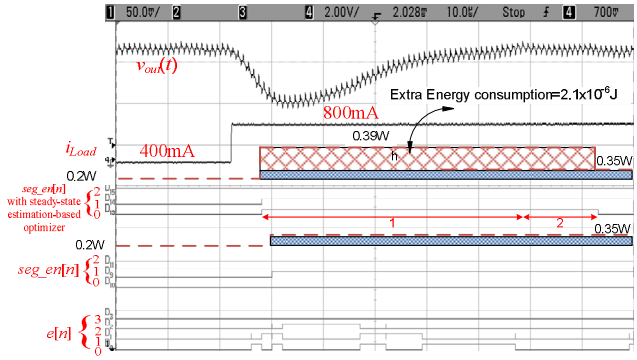


Fig.7.: Dynamic response with estimation-based optimizer and instantaneous online optimizer. Ch1: Output converter voltage (50mV/div); Ch2: load step command. D0-D3: ADC error, e[n];D9-D11: Segment Enable signal for instantaneous optimizer; D13-D15: Segment Enable signal for steady-state estimation-based optimizer ;

swing controller updates the *gain_sl* from 011 to 100 and finally 101, thereby increasing the gate voltage swing dynamically to offset the effect of increased conduction losses in power MOSFETs. Fig 7 compares the dynamic response of

the converter under two different cases, with the optimization controller presented in this work and with steady-state estimation-based optimizer [10]. The operation of this estimation-based optimizer is described as follows. Upon detecting a load transient all segments are turned on to avoid

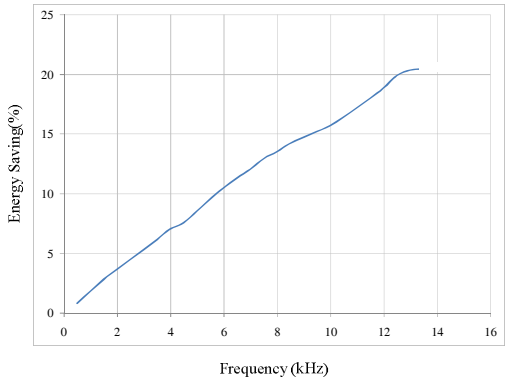


Fig.8. : Energy savings with instantaneous online optimizer versus estimation-based optimizer

over-stressing the power MOSFETs for the worst case scenario, the controller remains in this state until steady-state error $e[n] = 0$ is detected (period 1). The controller then counts for few cycles while $e[n] = 0$ (period 2) and adjusts the segments for the new load current value. If the load current is less than maximum, during this time, the steady-state optimizer operates in a sub-optimal mode. This is because of increased switching losses due to active operation of all the segments. On the other side, the new instantaneous optimizer sets the optimal segment configuration for the instantaneous current.

Figure 7 compares the measured losses for the two configurations. The results show that the steady-state estimation-based optimizer will result in extra energy consumption during transients, which depends on the frequency of the load change. The energy consumption under both methods is measured at different load step frequencies. Figure 8 shows that dynamic optimization controller results in 20% peak energy savings at 14 kHz load change frequency.

V. Conclusion

In this paper a digital controller is introduced that dynamically changes mode of operation in a segmented power stage to maximize power processing efficiency when highly dynamic loads are supplied. The controller operates as a mixed-signal peak current program mode voltage regulator, where a digital current reference is created and used for the efficiency optimization. The losses are minimized by combining two methods. Based on the current reference, in each switching cycle, the optimal number of power switch segments and gate drive voltages are set through the controller and a dual-output switch-capacitor circuit. A prototype system was build to verify the effectiveness of the system. The results show that the on-line optimization improves efficiency by as much as 20% in light load region and 8% in medium load and that, for dynamic loads, improves energy utilization by up to 20 %.

References

[1] A.V. Peterchev, J. Xiao and S.R. Sanders, "Architecture and limplementation of a digital VRM controller," ," *IEEE Transactions on Power Electronics.,* Volume: 18, Issue: 1, Jan. 2003 Pages: 356 – 364

[2] N. Rahman, A. Parayandeh, K. Wang, A. Prodic " Multimode Digital SMPS Controller IC for Low-Power Management", *Proc. IEEE ISCAS Conf.* May 2006, pp. 5327-5330.

[3] B. Patella, A. Prodic, A. Zirger, D. Maksimovic, "High-frequency digital controller PWM controller IC for DC-DC converters," *IEEE Transactions on Power Electronics*, , vol. 18, pp. 438-446, January 2003

[4] E. O'Malley and K. Rinne, "A programmable digital pulse width modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 MHz," in *Proc. IEEE APEC Conf.*, 2004, pp. 53–59.

[5] Z. Zhao, A. Prodić, "Limit-Cycle Oscillations Based Auto-Tuning System for Digitally Controlled DC-DC Power Supplies," *IEEE Transactions on Power Electronics*, November 2007, Vol.24, Issue 6, pp. 2211-2222.

[6] Z. Zhao, V. Smolyakov, and A. Prodic, "Continuous-time digital signal processing based controller for high-frequency DC-DC converters," in *Proc. IEEE APEC Conf*, 2007, pp. 557–562.

[7] Z. Lukić, A.Prodić, "Universal and Fault-Tolerant Multiphase Digital PWM Controller IC for High-Frequency DC-DC Converters," in in *Proc. IEEE APEC Conf*, 2007, March 2007.

[8] Z. Lukić, Z. Zhao, A.Prodić, and D. Goder "Digital Controller for Multi-Phase DC-DC Converters with Logarithmic Current Sharing ," in *Proc. IEEE PESC*, 2007, June 2007. [2] J. Clerk Maxwell, *A Treatise on Electricity and Magnetism,* 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[9] O. Trescases, G. Wei, A. Prodić, W.T. Ng, K. Takasuka, T. Sugimoto, and H. Nishio "A Digital Predictive On-Line Energy Optimization Scheme for DC-DC Converters," in *Proc. IEEE APEC Conf*, March 2007.

[10] O. Trescases, W. Ng, H. Nishio, E. Masaharum, and T. Kawashima, "A digitally controlled DC-DC converter module with a segmented output stage for optimized efficiency," in *Proceedings, IEEE International Symposium on Power Semiconductor Devices & ICs*, pp 409-413, 2006.

[11] J. Xiao, A. Peterchev, J. Zhang, S.R. Sanders, "A 4-µA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *IEEE Jour. Solid-State Circ.* Vol. 39, pp. 2342-2348, Dec. 2004.

[12] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead-times in DC-DC converters with synchronous rectifiers," in *Proceedings, IEEE Applied Power Electronics Conference and Exposition*, pp. 911–917, 2005.

[13] S. Musuniri and P. Chapman, "Improvement of light load efficiency usinf width-switching scheme for CMOS transistors," *Power Electronics Letters*, vol. 3, no. 3, pp. 105–110, 2005.

[14] M. Mulligan, B. Broach, and T. Lee, "A constant frequency method for improving light-load efficiency in synchronous buck converters," *Power Electronics Letters*, vol. 3, pp. 24–29, March 2005.

[15] O. Trescases, Z. Luki´c, W.-T. Ng, and A. Prodi´c, "A low power mixed-signal currentmode DC-DC converter using a one-bit delta sigma DAC," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2006, pp. 700–704.

[16] A. Parayandeh, A. Prodić, "Programmable Analog-to-Digital Converter for Low-Power DC-DC SMPS," *IEEE Transactions on Power Electronics*, January 2008, Vol.23, Issue 1, pp. 500-505.

[17] H. Peng and D. Maksimović, "Overload protection in digitally controlled DC-DC converters," in *Proc. IEEE Power Electronics Specialist Conf.*, Jun. 2006, pp. 1 – 6.

[18] O. Trescases , N. Rahman, A. Prodić, W.-T. Ng, "A 1V buck Converter IC with Hybrid Current-Mode Control and a Charge Pump DAC", in *Proc. IEEE Power Electronics Specialist Conf.*, Jun. 2008

[19] V.Kursun, S.G. Narendra, V.K.De, and E.G Friedman, " Low-voltage-swing monolithic dc-dc conversion," *IEEE Transactions on Circuits and Systems-II:Express Briefs,* vol.51, no. 5, pp.241-248, May 2004

[20] J. Kotowski, W. J. McIntyre, J. P. Parry, United States Patent 6,055,168, Apr.25, 2000.