ESR Zero Estimation and Auto-compensation in Digitally Controlled Buck Converters

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***Abstract* - A method for estimating and compensating the zero introduced by the capacitor equivalent series resistance (ESR) in the buck converter transfer function is introduced. The method is well-suited for practical implementation with digital controllers. The ESR zero is estimated by online measurement of the output voltage ripple and the power stage corner frequency. Accordingly, the coefficients of the PID compensator are updated to avoid potential stability problems. Theoretical basis of the identification and the compensator design are presented. The method is experimentally verified on a 12V-to-1.5V, 500 kHz, 10W buck converter prototype.**

I. INTRODUCTION

In a dc-dc buck converter, the output capacitor equivalent series resistance (ESR) introduces a left-hand plane zero in the transfer function [1, 2]. It is well known that the zero influences the total loop response. Hence, it is highly desirable that the zero is identified and that its influence is minimized, through compensator design, such that the desired control bandwidth [2] is achieved. Otherwise, the system could suffer from overly aggressive or slow response, related to insufficient phase margin, noise problems, or even instability. In numerous applications the accurate value of the ESR is often unknown. This is because various types of capacitors having different ESR values are usually combined and their parameters change with external influences, such as temperature and aging. Therefore, in order to meet the regulation requirements, the application engineers usually have to go through an iterative process, to configure the analog compensation networks.

Recent publications [3-11] show that digital controller implementation could potentially provide a solution to the problem. In the previous art [6-10] component variations of the power stage are identified online and the compensator is tuned accordingly, to improve dynamic response. In that work, the tuning is based on the identification of the power stage corner frequency [7, 8] or on the suppression of the load disturbance [9], without considering the impact of the capacitor ESR zero. In [10], a sophisticated PID type compensator is designed, based on a complete frequency spectrum analysis that includes the effects of the ESR zero. However, this method requires open-loop operation and a large number of computations, i.e. a powerful processing unit.

In this paper, we introduce a practical method for online ESR zero identification and a complementary compensator design method. The method is based on a digital controller implementation shown in Fig. 1. The system consists of an auto-tuning digital controller [7] and a new identification block, whose task is online estimation of the capacitor ESR zero value. The estimation is based on the output voltage switching ripple measurements at a reduced switching frequency as well on the estimation of the power stage's LC product value. Based on the results of the estimation, the PID compensator is automatically redesigned, to take into account the ESR zero effect. The proposed method ensures a consistent control bandwidth across the wide variations of the capacitor ESR values.

The paper is organized as follows. In the next section, the proposed ESR zero identification method and system are presented. The PID design procedure with ESR zero compensation is then demonstrated in Section III. Experimental results verifying the effectiveness of the method are shown in Section IV. Finally, the conclusions are given in Section V.

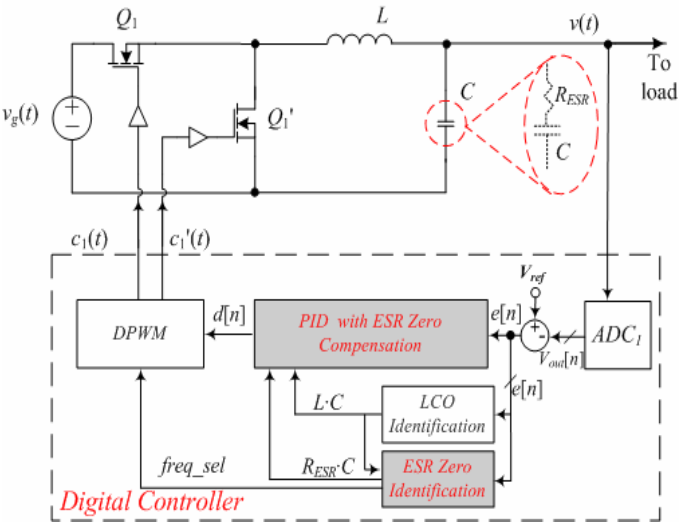

Fig. 1. A digitally controlled buck converter with ESR zero auto-compensation

II. ESR ZERO IDENTIFICATION

The theoretical background for the proposed identification method can be given through the following analysis.

A buck converter shown in Fig.1 has the following control-to-output transfer function [7, 8]:

$$G(s)=\frac{v_o(s)}{d(s)}=V_{in}\cdot\frac{1+s\tau_{ESR}}{1+2\frac{\xi}{\omega_0}s+\frac{s^2}{\omega_0^2}} \quad (1)$$

Where $\xi=\frac{(R_{dson}+R_{ESL}+R_{ESR})}{2}\sqrt{\frac{C}{L}}$, $\omega_0=\frac{1}{\sqrt{LC}}$, and $f_{ESR}=\frac{1}{2\pi\tau_{ESR}}=\frac{1}{2\pi R_{ESR}C}$ is the ESR zero frequency.

The output voltage ripple is closely correlated with R_{ESR} and it can be approximated as:

$$\Delta V_{rip}=\sqrt{(\Delta V_{ESR}^2+\Delta V_C^2)} \quad (2)$$

Equation (2) consists of two parts. The first part is contribution to the ripple due to the voltage drop across R_{ESR}, ΔV_{ESR} ; The second part, by the change of the capacitor charge ΔV_C . These two components can be expressed as follows:

$$\Delta V_{ESR}=R_{ESR}\cdot\Delta I=R_{ESR}\frac{V_g-V}{L}DT_s \quad (3)$$

$$\Delta V_C=\frac{\int_t^{t+T_s}\Delta I d\tau}{4C}=\frac{(V_g-V)DT_s^2}{8LC} \quad (4)$$

where D is the steady state duty-ratio, I is the inductor current ripple, and T_s is the switching period.

Equation (2) is obtained from phasor analysis where the two ripple components, ΔV_{ESR} and ΔV_C , are to have a phase difference of 90°. When the ESR contribution to the ripple is significantly larger than that of the charge, the approximation $\Delta V_{rip}\approx\Delta V_{ESR}$, can be adopted and R_{ESR} calculated from (3). Then, the ESR zero time constant becomes:

$$R_{ESR}\cdot C=\frac{LC\cdot\Delta V_{rip}}{(V_g-V)DT_s}=\frac{1}{2\pi f_{ESR}} \quad (5)$$

In this study, equation (5) is used to perform the ESR zero calculation. The condition for ΔV_{ESR} to dominate in (2) can be derived from equation (3) and (4) where it is clear that the requirement is for the ratio of $\frac{\Delta V_{ESR}}{\Delta V_C}$ to be much greater than 1. By combining (3) and (4), this condition can be further expressed in terms of switching frequency f_s and output capacitance value, as follows:

$$\frac{\Delta V_{ESR}}{\Delta V_C}=8R_{ESR}\cdot Cf_s=\frac{4f_s}{\pi f_{ESR}}>>1 \quad (6)$$

This equation indicates that for the switching frequencies significantly higher than f_{ESR} the voltage ripple is dominated by the ESR component. In most converters this condition is easily satisfied. In fact, at the critical condition $\frac{\Delta V_{ESR}}{\Delta V_C}=1$, τ_{ESR} estimate can be at most 2 times as large as its real value, i.e. estimated f_{ESR} 1/2 times as large as $\frac{4f_s}{\pi}$ or $\frac{f_s}{2}$ for simplicity. As the estimated f_{ESR} decreases below 1/2 f_s, the estimation accuracy increases. Therefore, 1/2 f_s is used as the upper limit for f_{ESR} estimation in this study.

A. System Operation

As it is shown in (5), the calculation of ESR zero's time constant depends on two measurable quantities, the output voltage ripple ΔV_{rip} and the power stage LC product.

In a digital controller, the output voltage ripple information can be obtained from the ADC by sampling two times in a switching cycle. However, this will require a fast ADC with a conversion time less than ½ T_s, which is usually not available in the original design. Here, in order to capture the output voltage ripple with the existing ADC in the regulator of Fig.1, during the ESR zero identification phase the switching frequency is reduced by half allowing the output voltage to be sampled twice per switch cycle. Thus, based on the analysis in section *A*, the method identifies the ESR zero at frequencies up to 1/4 f_s, limited by the Nyquist rate. Nonetheless, the zeros located beyond 1/4 f_s will have little impact on the loop dynamic since they are likely to fall out of the common control bandwidth of (1/20 1/10) f_s.

As shown in Fig. 2, two consecutive error samples e_1 and e_2 are obtained from the ADC during an *N*-cycle long ESR identification phase. From the difference between the samples, $e=e_2-e_1$, the output voltage ripple, ΔV_{rip} is estimated as $\Delta V_{rip}=2(1-D)\cdot\Delta e$. Then, the time constant τ_{ESR} is calculated from (5) using the information about power stage LC product obtained from limit-cycling oscillations [7].

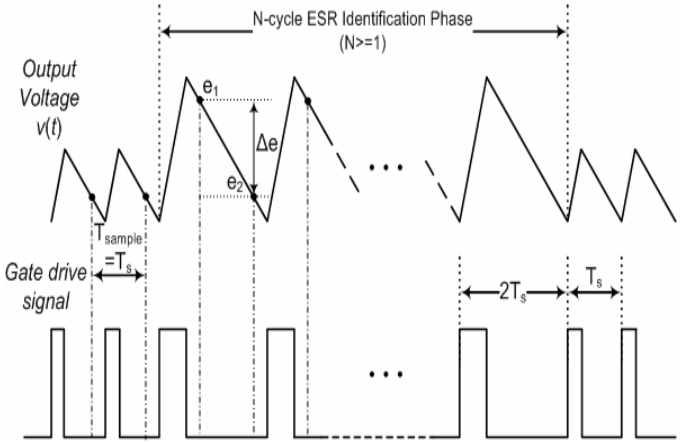

Fig. 2. Illustration of ESR zero identification test

The quantization error of the ADC can also affect the identification accuracy. As shown in (5), a high accuracy of the ESR zero time constant estimation is obtained when the ESR ripple is large and vice versa. Therefore, an ADC quantization step less than or, at least, equal to the ESR ripple component at ¼ f_s, which is the higher bound of the identifiable zero frequency, is needed for the system described here . This value can be found from (5) and expressed as:

$$\frac{LC \cdot q_{ADC}}{(V_g - V)DT_s} = \frac{1}{2\pi(\frac{1}{4}f_s)}$$
$$q_{ADC} = \frac{(V_g - V)DT_s^2}{2\pi LC} \quad (7)$$

It can be seen that the selected ADC quantization step approximately equals to the voltage ripple component ΔV_C of ideal capacitor in (5).

III. Digital PID Design with ESR Zero Cancellation

The discrete-time PID that compensates for the ESR zero has the following form:

$$PID(z) = PID_{std}(z) \cdot \frac{kz}{z-d}$$
$$= \frac{az^2+bz+c}{(z-1)z} \cdot \frac{kz}{z-d} = \frac{k(az^2+bz+c)}{(z-1)(z-d)} \quad (8)$$

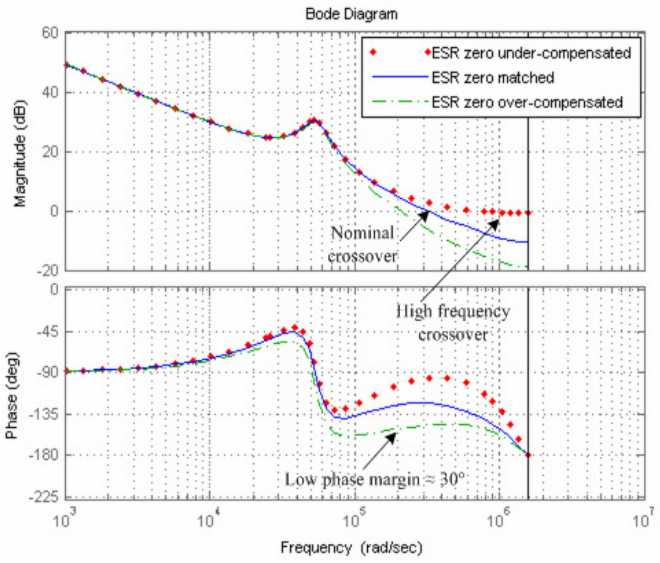

Fig. 3. Bode plot comparison of loop transfer functions PID(z)*G(z) using different ESR zero compensation parameters. Red: d=0; Blue: d=0.5 (matched with the ESR zero); Green: d=0.77;

It is designed such that a pole at the identified ESR zero, $z=d$, is added to $PID_{std}(z)$, which stand for standard PID designed

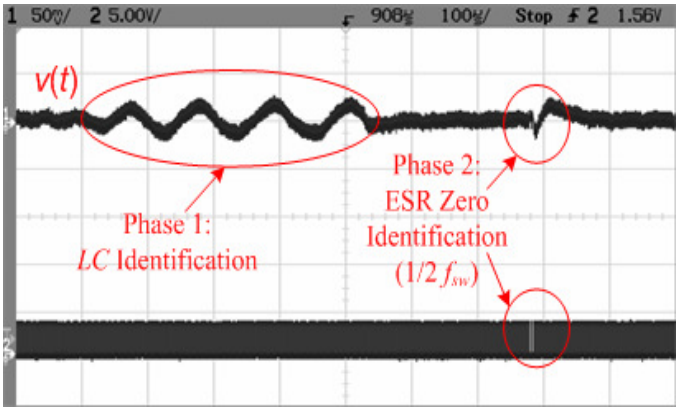

Fig. 4. An example of the ESR zero identification test

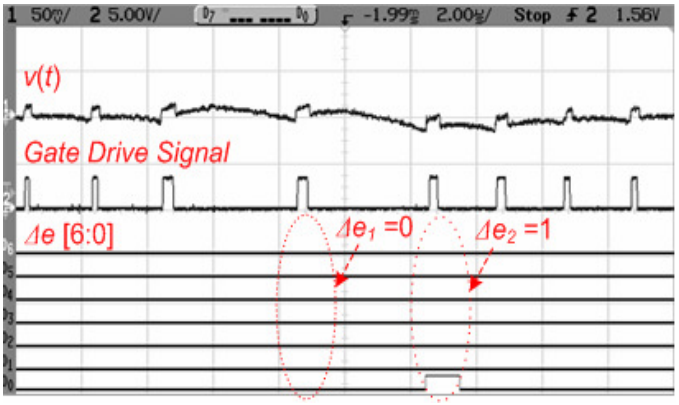

Fig. 5. Enlarged view of Phase 2 in Fig. 4

using conventional methods presented in [6],[7], and [11]. Because the $PID_{std}(z)$ has a pole at z=0(or at 1) this is equivalent to introducing a lead-lag filter: $\frac{k \cdot z}{z-d}$. Note that the total loop gain needs to remain the same to maintain the specified bandwidth. Therefore, the dc gain of the introduced filter is selected to be equal to 1. Thus, at dc frequency, i.e. $z=1$, we have $\frac{k}{1-d}=1$ or $k=1-d$.

The transformation of the ESR zero to the discrete domain is performed using pole matching equivalence [12], i.e. $d = e^{-\omega_{ESR}T_s} = e^{-T_s/R_{ESR}C}$. Again, a look-up table is employed to perform this transformation, as a low-cost solution.

The effect of the introduced filter is shown in Fig. 3, where a comparison of the loop frequency response using three different PID compensators is shown. A design that does not take into account ESR zero, one with its overestimation, and the matching design previously described are compared. As we can see, the over-compensated PID, decreases the phase margin and causes stability problems. On the other hand, the under-compensated PID, caused by a wrong estimation of the ESR zero frequency, reduces the gain margin and makes the system noise-sensitive at high frequency. Only the proposed

well-matched PID design ensures stability and achieves the desired bandwidth.

IV. Experimental Results

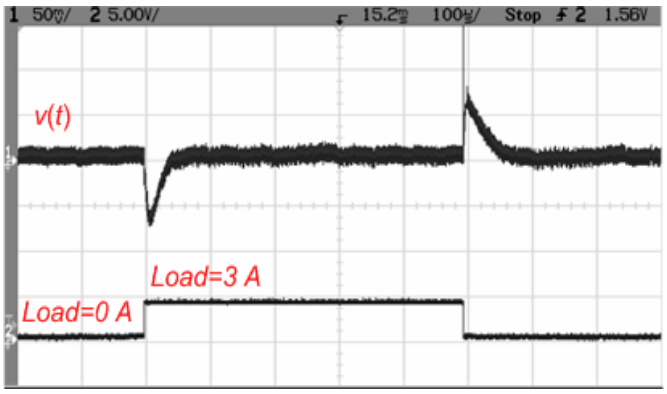

Fig. 6. Load transient response with ESR zero well-compensated PID

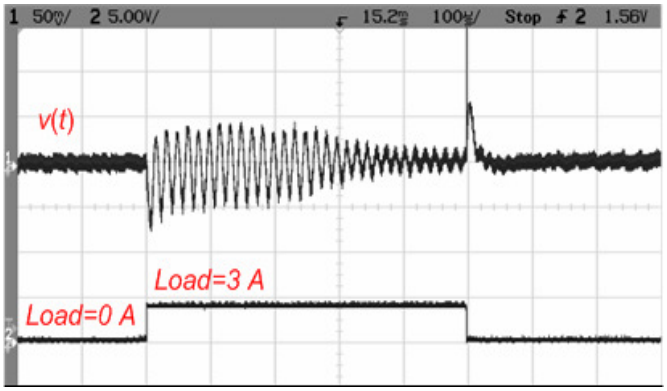

Fig. 7. Load transient response with ESR zero over-compensated PID

An FPGA based prototype has been built around a 12V-to-1.5V 500 kHz 10W buck converter. The ADC has a resolution of 4mV. A complete system identification test is shown in Fig 4. In phase 1, the power stage *LC* frequency is acquired from intentionally introduced limit-cycle oscillation [7], [8]. In the following phase, the ESR zero is identified from the voltage ripple measurement. For two cycles, the switching frequency is reduced to a half of its regular value, as described in Section II. The sudden change in switching frequency introduces a small sub-transient that does not significantly affect regulation. An enlarged view of phase 2 is shown in Fig. 5.

In the case of Figs. 4 and 5, the measurements of a small voltage ripple, Δe_1=0 and Δe_2=1, are obtained. An ESR zero frequency of 700 kHz is then calculated from (3) using the averaged value of Δe. This frequency is much higher than the identification limit, i.e. 1/4 f_s = 125 kHz. ESR zero beyond this upper limit and is not taken into consideration, since for the proposed compensator design it does not have a significant influence on the loop response. Thus, a standard PID compensator with d=0 is used to provide stable transient response with a control bandwidth of 50 kHz. The load transient response of this compensator is shown in Fig. 6.

On the contrary, if a PID compensator that overestimates a

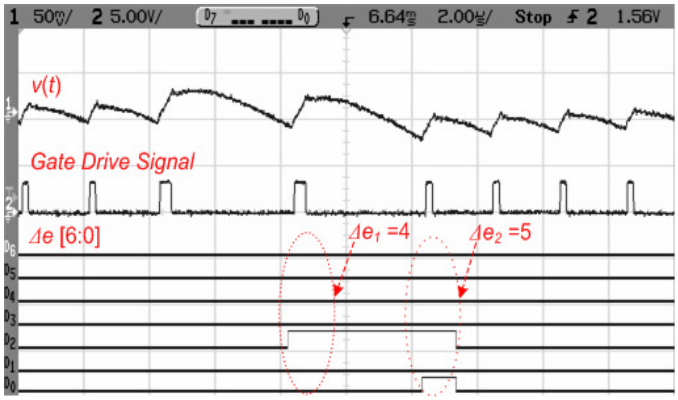

Fig. 8. ESR zero identification Phase 2 (large ESR case)

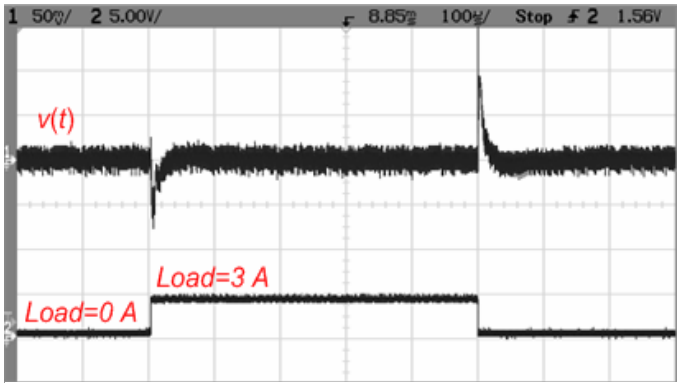

Fig. 9. Load transient response with ESR zero well-compensated PID (for the large ESR case)

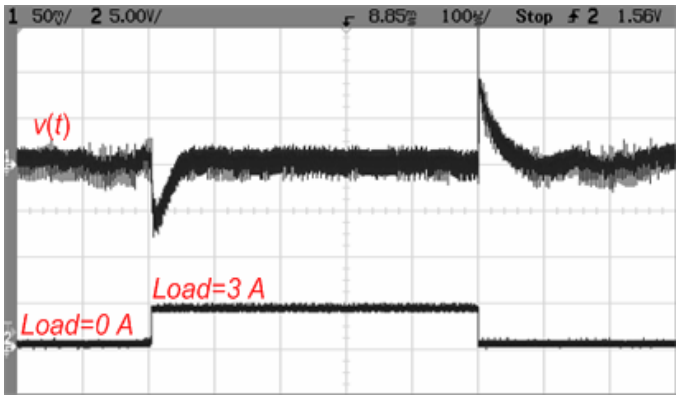

Fig. 10. Load transient response with ESR zero under-compensated PID (for the large ESR case)

low frequency ESR zero, with d=0.25, was used, without performing the ESR zero identification, the system would become unstable. This is because the over-compensated PID reduces the phase margin as shown in Fig. 3. This scenario is tested on the setup and the results shown in Fig. 7 confirm the possible instability problem.

In another scenario, with an output capacitor that has a large ESR, i.e. low frequency ESR zero, is used. Consequently, a larger output ripples, e_1=4 and e_2=5, are measured, as shown in Fig. 8 and a PID is constructed accordingly with self-calibrated d=0.15, it delivers a satisfactory response shown in Fig 9. However, as can be seen in Fig. 10, when the standard PID with d=0 for small ESR compensation is used the system becomes very sensitive to noise. Experimental results confirm that the proposed ESR identification and compensation are effective in ensuring system stability and a well-controlled bandwidth.

V. CONCLUSION

A practical method for online capacitor ESR zero identification and compensation is proposed for a digitally controlled buck converter. It utilizes output voltage ripple measurement as well as the knowledge of the *LC* product to derive the ESR zero value. A PID compensator with ESR zero compensation capability is then designed based on the results of the identification. Experimental results show that the proposed system ensures the desired control bandwidth for a wide range of capacitors used and also avoids potential stability problems associated with unknown or uncertain ESR zero.

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