Self-Tuning Sensorless Digital Current-Mode Controller with Accurate Current Sharing for Multi-Phase DC-DC Converters

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***Abstract* – A sensorless multi-phase average current-program mode controller with an accurate self-tuning current estimator is introduced. Based on the values of the duty ratio, and the input and output voltages, the estimator calculates the average inductor current of each phase in a multi-phase dc-dc converter. The averaged values are calculated over one switching cycle. The estimator employs a phase-by-phase self calibration scheme. During the calibration, regulators of all currents but one are "frozen" and a small load step is intentionally introduced, by a test current sink. Based on the response, the parameters of the active phase are automatically adjusted such that accurate estimation and equal current sharing are achieved. Experiments with a 12 V-to-1.5 V, 60 W, 500 kHz, two-phase buck converter verify that the controller ensures fast estimation and, at the full load, a current sharing error of less than 5%.**

I. Introduction

Multi-phase dc-dc switch-mode power supplies (SMPS) [1-4] are common in modern electronic devices such as personal computers, servers, telecommunication equipment, and consumer electronics. Compared to traditional single phase topologies, these parallel structures show several advantages. These include better heat distribution, faster dynamic response, smaller voltage and current ripple, all of which result in a significant reduction of the overall size of the power supply.

One of the main challenges in the full utilization of the multi-phase converter topologies advantages is to ensure desired current sharing [4-13] between the phases. Even if all phases are comprised of the same components, mismatches in their actual values can result in serious problems. Some of the phases could take significantly larger currents than others and result in current-stress related system failures [3], [14].

To eliminate the current sharing problem, analog current sensing circuits are commonly employed [15-17]. They often require costly implementations, which, in some cases, can outweigh the advantages of multi-phase operation. In addition, the analog sensing solutions are sensitive to external influences such as temperature and aging and are not suitable for integration with emerging digital systems that show superior performance and flexibility.

The controller architecture proposed in this paper provides a solution for equal or non-uniform current sharing in multi-phase topologies and is well suited for integration in digital systems.

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II. System Operation

As shown in Fig.1, the new system is fully-digital, except for the analog-to-digital converters (ADC). It comprises of a multi-phase current estimator that calculates the current of each phase and a multi-phase average current-programmed mode controller, which regulates the output voltage indirectly, by generating the references for the phase currents.

The controller operates as follows: Based on the error between the output voltage and its reference, $e[n]$, a PID compensator creates $i_{tot}[n]$, a digital value proportional to the total current of all phases, i.e. to the load current. The $i_{tot}[n]$ is then passed to *Current Sharing Logic* that sets digital references for the currents of all N phases, $i_{ref1}[n]$ to $i_{refN}[n]$. Depending on the converter topology, the references can be set to be the same, for equal current sharing, or they can have different values allowing regulation of converters with non-uniform sharing [4], [13]. The block labeled *Multi-Phase*

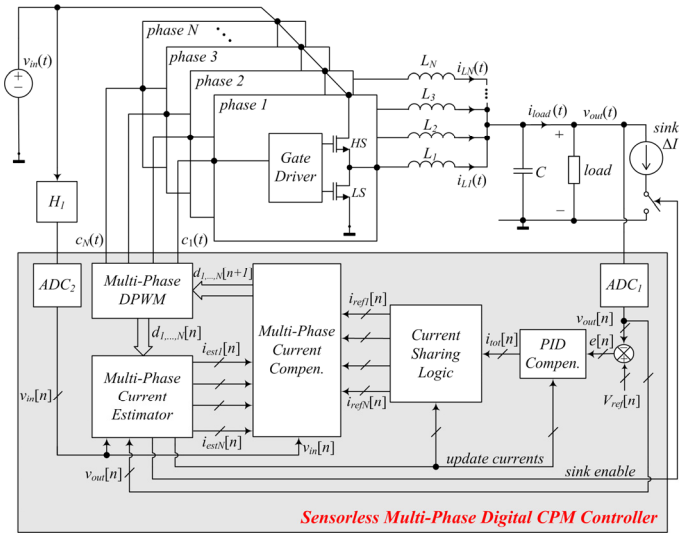

Fig. 1. A self-tuning sensorless digital current-mode controller regulating the operation of a multi-phase buck converter

Current Compensator compares estimated currents with their references, and, accordingly, creates control signals for a multi-phase digital pulse-width modulator (DPWM) [18].

To calculate averaged inductor current over one switching cycle, the auto-tuning multi-phase estimator uses information about input and output voltage values as well as that of the duty ratio. The tuning of the estimator is performed using a phase-by-phase self-calibration procedure. During steady-state, the current references for all phases but one, which is under calibration, are "frozen". Then, a small and known load current step is introduced, by a current sink, and the response of the active phase is observed. By comparing the estimated current step in that phase and the expected one, this self-tuning estimator adjusts its own parameters, to match the values of the currents.

III. ESTIMATOR

The multi-phase current estimator operates on the same principle as the fully-digital system described in [19]. The main difference is that the previous solution is designed for single-phase converters only and, in its original form, is not suitable for the multi-phase operation.

To describe the system, first, operation of the single phase system is briefly reviewed. Then, the new multi-phase estimator solution is presented.

As shown in Fig.2, the single-phase system of [19] is a digital equivalent of the well-known analog *RC* current estimator [20]. The analog *RC* filter, which provides voltage proportional to the inductor current:

$$V_{sense1}(s) = I_{L1}(s)\cdot R_{L1}\cdot\frac{1+s\cdot\frac{L_1}{R_{L1}}}{1+s\cdot R_{f1}C_{f1}} = I_{L1}(s)\cdot R_{L1}\cdot\frac{1+s\cdot\tau_{L1}}{1+s\cdot\tau_{f1}}, \quad (1)$$

where L_1 and R_{L1} are the inductance and its equivalent series resistance, respectively, and R_{f1} and C_{f1} are the filter components. When the filter parameters are selected such that $\tau_{f1} = R_{f1}\cdot C_{f1} = L_1/R_{L1} = \tau_{L1}$, i.e. the time constants of the filter and that of the power stage inductor are the same, the capacitor voltage becomes a scaled and undistorted version of the inductor current.

The conventional *RC*-based analog estimators often

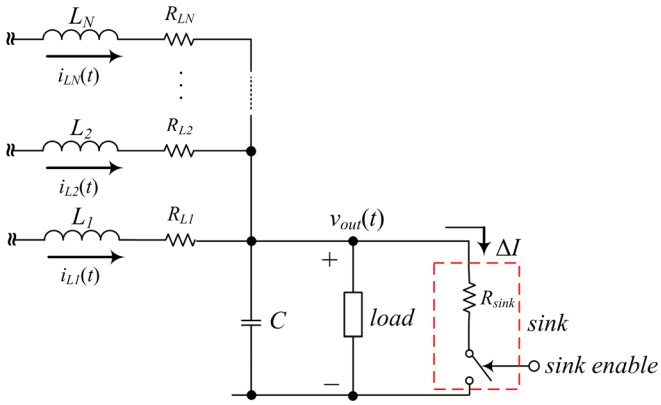

Fig. 3. Current sink circuit used for calibration of the multi-phase current estimator in the controller architecture

introduce a significant error [21]. This problem is a result of a mismatch in time constants, caused by variations of filter and converter parameters, which are affected by external influences and change with operating conditions. The replacement of the analog components with a self-tunable digital equivalent [19] allows on-line compensation for the time constant variations. The digital filter calibration is done with the help of a current sink. It introduces a small and known load step that is compared to the estimator response and, based on the difference, tuning is performed, such that the time constants are equal.

A. Multi-phase digital current estimator

The calibration process used in single phase topologies [19] cannot be directly applied for multi-phase systems. While in the single-phase case, the load step introduced by the current sink must be equal to the inductor current, in multi-phase systems, it is not the case. From Figs. 3 and 4 it can be seen that the current step can be shared between the phases in many different ways, depending on the mismatch in power stage component values.

To solve this problem, a multi-phase average current-program mode controller is used and a phase-by-phase calibration process, based on "freezing" all phases but one, described in the previous section, is implemented. As a result only the current in the active phase increases and the increment

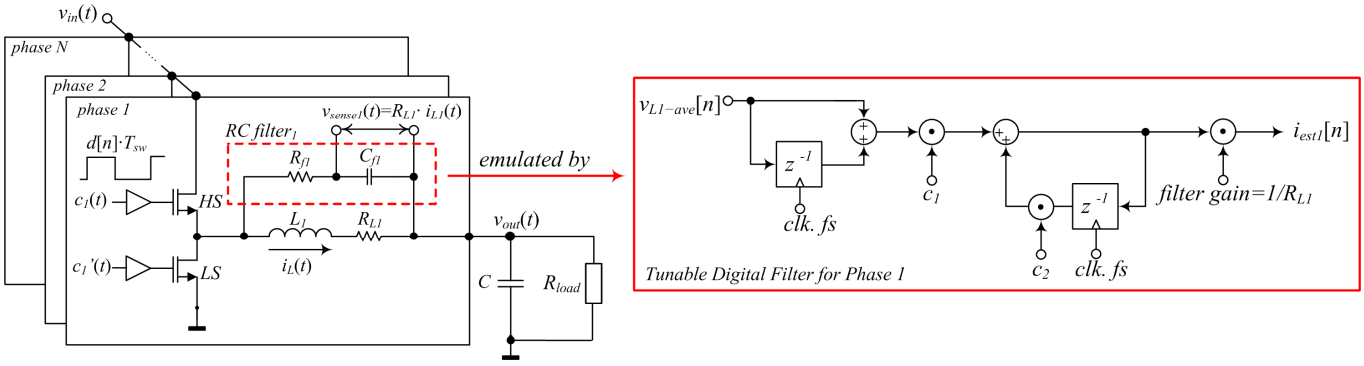

Fig. 2. An analog *RC* filter used for inductor current estimation is replaced by a digital IIR filter equivalent

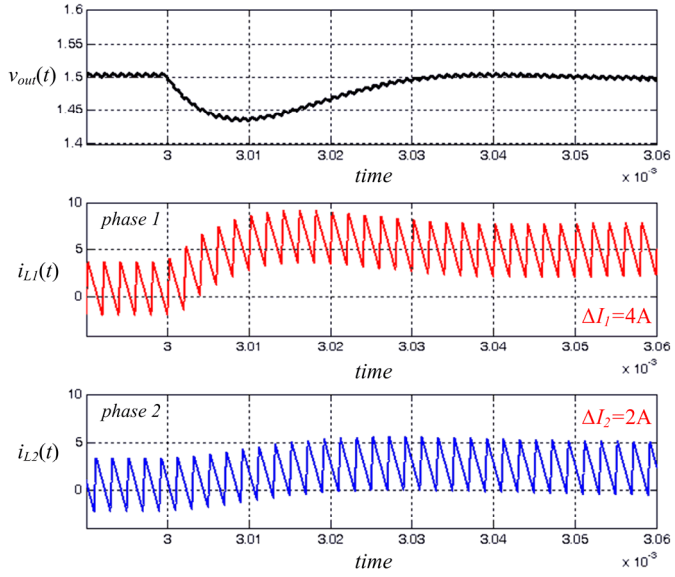

Fig.4. Simulation result of the calibration step applied to a two-phase buck converter regulated by a voltage mode controller

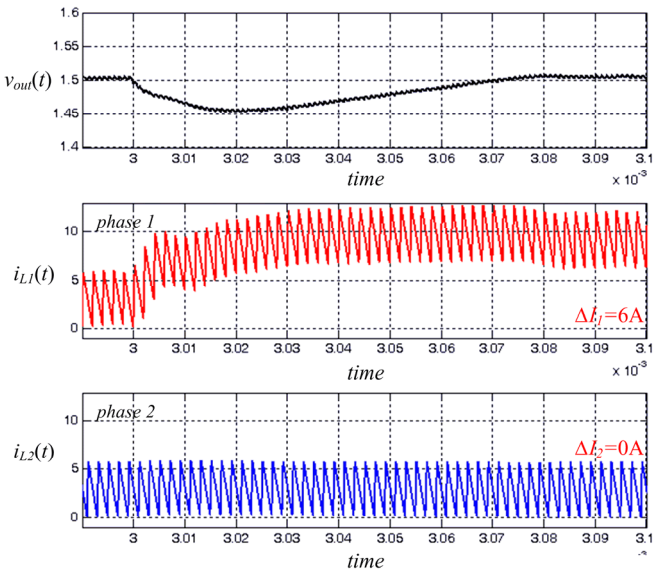

Fig.5. Simulation result of the calibration step applied to a two-phase buck converter with a "frozen" current reference for the second phase

is equal to that of the test current sink, as shown in Fig.5.

IV. Multi-phase Current Loop Compensator

The multi-phase current loop compensator of Fig.1 regulates currents of all phases. Based on the reference and estimated current values, as well as on the input voltage, it calculates separate duty ratio control signals for each of the phases. For an *N*-phase converter, the compensator consists of *N* single phase structures as shown in Fig.6.

To calculate the duty-ratio control signal $d[n]$ such that the estimated phase current follows the reference $i_{refi}[n]$, the phase compensator applies a dead-beat algorithm [22],[23]. The compensator operation can be described by looking at Fig. 7 showing inductor current and its reference when a change in the reference has occurred. In order to compensate for the error, labeled with the shadowed area, the duty-cycle $d[n+1]$ is changed. The change Δd is selected such that the average value of the inductor current in the next switching cycle is equal to the reference. The shadowed area, and corresponding change in the duty ratio, for a buck topology, can be calculated as follows:

$$A = \frac{V_{in}}{L} \cdot \Delta d \cdot T_{sw} \cdot \left(1 - d[n] - \Delta d\right) \cdot T_{sw} + \frac{1}{2} \cdot \frac{V_{in}}{L} \cdot \left(\Delta d \cdot T_{sw}\right)^2, \quad (2)$$

where V_{in} and V_{out} are the input and output voltages of the converter, L is the inductance of the power stage, and the switching period is $T_{sw} = 1/f_{sw}$. For a limited bandwidth of the voltage loop, i.e. for small Δd and Δi_{ref} , the shadowed area A can be approximated as:

$$A = \frac{V_{in}}{L} \cdot \Delta d \cdot T_{sw} \cdot \left(1 - d[n]\right) \cdot T_{sw}. \quad (3)$$

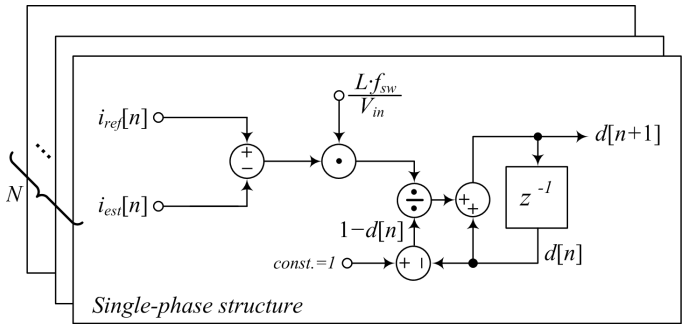

Fig. 6. The block diagram of multi-phase current loop compensator

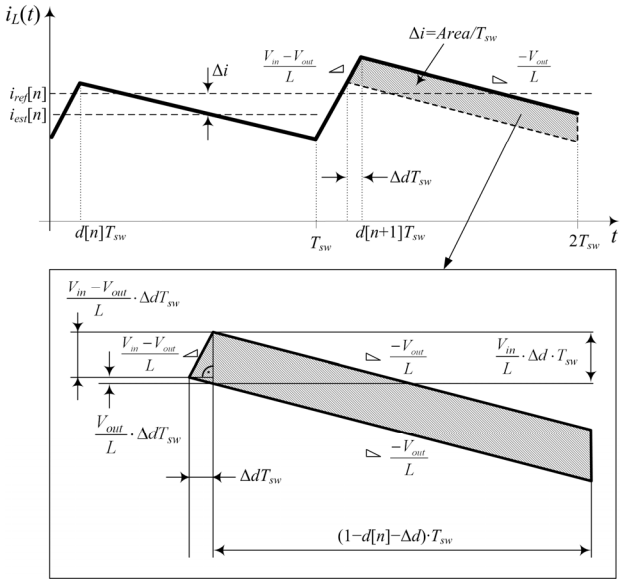

Fig. 7. Inductor current waveform during two consecutive switching cycles

From Fig.7, it can be seen that the increment in the current value resulting in the dead beat operation is

$$\Delta i = \frac{A}{T_{sw}} = \frac{V_{in}}{L} \cdot \Delta d \cdot T_{sw} \cdot (1 - d[n]). \quad (4)$$

Based on (3) and (4), the new duty ratio $d[n+1]$ can be calculated as:

$$d[n+1] = d[n] + \Delta d = d[n] + \frac{i_{ref}[n] - i_{est}[n]}{V_{in} \cdot (1 - d[n])} \cdot L \cdot f_{sw}. \quad (5)$$

V. Experimental Systems and Results

To verify functionality, 12V-to-1.5V, 60 W, two dual-phase prototypes were built, based on the diagram of Fig.1. The first prototype was designed to provide equal current sharing of 20 A per phase. The second prototype utilizes non-uniform current distribution (27 A and 13A) optimizing light-to-medium load efficiency [4,13]. All digital parts of the controller were implemented with an FPGA board. The input and output voltages are measured with ADCs sampling at f_{sw} and 1/8 f_{sw}, respectively. To display digital signals of the multi-phase estimator, its outputs are sent to digital-to-analog converters.

The functionality of the controller for the both topologies was tested first and the accuracy of the estimation was assessed. Then, the load transient response of the system was observed.

A. Calibration of Multi-phase Current Estimator and Equal Current Sharing

Figure 8 shows operation of the system designed for equal current sharing for two consecutive 30 A load transients and the calibration procedure with a 2 A test current sink. Initially the multi-phase current estimator is not calibrated, and a significant discrepancy between the phase currents occurs. Then, in between the 30 A transients the previously described phase-by-phase calibration procedure, involving the current

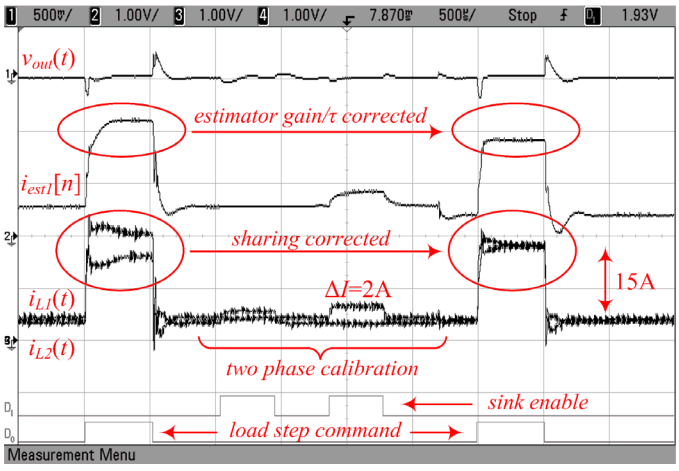

Fig.8. The system operation – Ch1: Output converter voltage (500mV/div); Ch2: estimated inductor current $i_{est1}[n]$ – 10 A/V; Ch3 and Ch4: measured inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ – 10 A/V; D0-D1- load step command and sink enable. Time scale is 500µs/div.

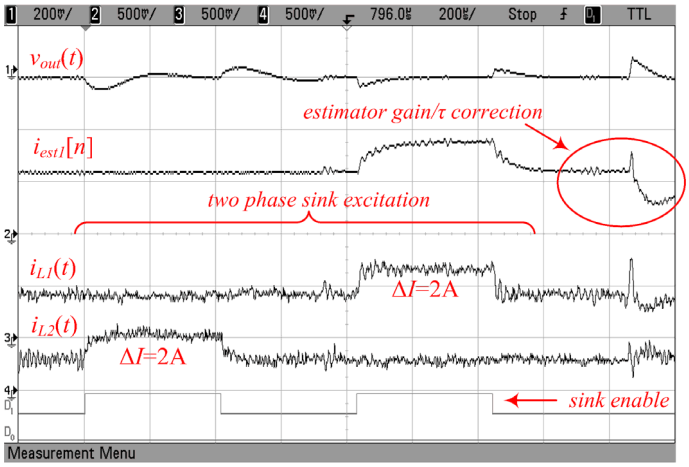

Fig.9. The two-phase calibration procedure – Ch1: Output converter voltage (200mV/div); Ch2: estimated inductor current $i_{est1}[n]$ – 10 A/V; Ch3 and Ch4: measured inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ – 10 A/V; D0-D1- load step command and sink enable. Time scale is 200µs/div.

sink, is applied. It can be seen that the calibration significantly reduces the estimation errors, and consequently, significantly improves the accuracy of the current sharing. Fig.9 shows a magnified view of the calibration procedure. It can be seen that, during the calibration, the current of one phase is "frozen" and only the active phase, which is under calibration, reacts to the disturbance caused by the test sink. After the load steps, introduced by the test sink, the gain and time constant of the filters are calibrated to the correct value.

B. Non-uniform Current Sharing

To obtain non-equal current sharing of 21 A and 7.5 A, the controller of Fig.1 is programmed such that the $i_{tot}[n]$ is divided between two phases as $i_{ref1}[n]=2/3 \cdot i_{tot}[n]$ and $i_{ref2}[n]=1/3 \cdot i_{tot}[n]$.

As shown in Fig 10, for such a setting, the inductor current

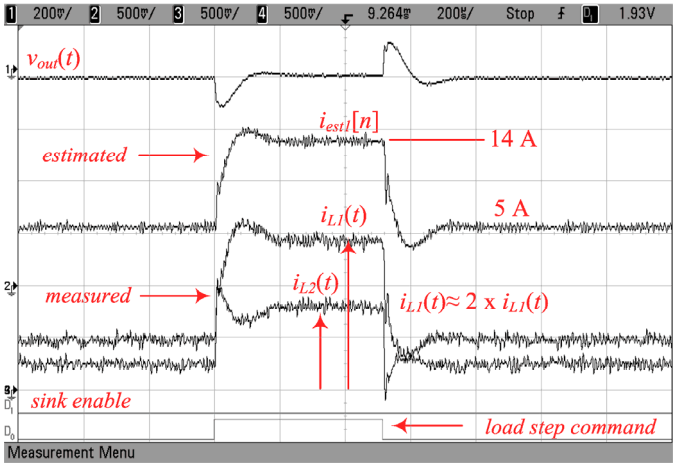

Fig.10. Non-uniform current sharing scheme – Ch1: Output converter voltage (200mV/div); Ch2: estimated inductor current $i_{est1}[n]$ – 10 A/V; Ch3 and Ch4: measured inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ – 10 A/V; D0 – load step command. Time scale is 200µs/div.

of the $i_{L1}(t)$ becomes twice as large as $i_{L2}(t)$ and this ratio is maintained throughout the load transients.

C. Accuracy of Current Sharing

For both experimental setups, test current steps of a 10% of the maximum phase currents were used. For such steps, an error smaller than 5% in current sharing is observed. It should be noted that by selecting a larger test steps the estimation error can be further reduced.

D. Load Transient Response

The response of the controller to a load step of 30A with the calibrated current estimator is shown in Fig.11. It can be seen that the system reaches steady state in less than 25 µs, which for the given switching frequency, is comparable to analog solutions. The figure also shows a good matching between measured current $i_{L1}(t)$ and its estimate $i_{est1}[n]$.

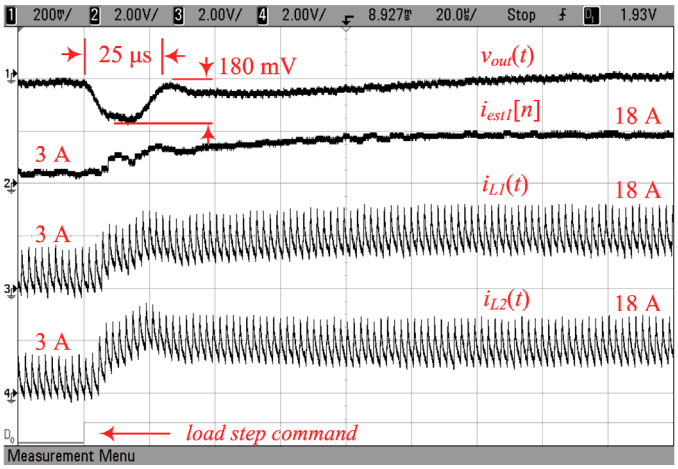

Fig.11. The load transient response between 6A and 36A – Ch1: Output converter voltage (200mV/div); Ch2: estimated inductor current $i_{est1}[n]$ – 10 A/V; Ch3 and Ch4: measured inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ – 10 A/V; D0 – load step command. Time scale is

VI. Conclusion

A sensorless multi-phase digital current-mode controller with a self-tuning estimator is introduced. The estimator is a digital equivalent of the well-known analog *RC* based solution. To minimize the estimation errors, due to parameter uncertainties, and provide equal current sharing, the system uses a known test load step and employs a phase-by-phase calibration procedure, where all phases but one, are frozen during a brief test step action. The effectiveness of the system was demonstrated on multi-phase experimental prototypes with uniform and non-uniform current sharing. It was shown that, for a load step rated at 10% of the phase current an error in current sharing smaller than 5% can be achieved.

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