Digitally Controlled Low-Power DC-DC Converter with Segmented Output Stage and Gate Charge Based Instantaneous Efficiency Optimization

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***Abstract* -- This paper introduces a digital controller and a segmented power stage that dynamically change mode of operation to maximize power processing efficiency when highly dynamic loads are supplied. The controller operates as a mixed-signal peak current program mode voltage regulator, where a digital current reference is created and used for the efficiency optimization. The losses of the power stage are minimized by combining two methods. Based on the current reference, in each switching cycle, the optimal number of power switch segments and the gate voltage swing level for power MOSFETS are set through a sequence controller and a gate voltage scaling circuit. A 1.8 V, 5 W, 1 MHz buck converter prototype is built. The results verify the operation of the system and show that on-line optimization raises and flattens the efficiency curve by as much as 18%**

I. INTRODUCTION

In portable applications where the source of energy is limited, sustaining long battery-powered operation is a major challenge. Addressing this challenge is an important constraint in design of the dc-dc converter that is used to deliver power from the battery to the portable device. DC-DC converters are generally designed with optimum efficiency over a limited range of load currents. However the current drawn by the digital load in portable devices is a function of processing digital signal and is constantly varying. As a consequence the dc-dc converter operates with sub-optimal efficiency over a long period[1-2]. To extend the battery operation will therefore require the designer to seek efficiency optimization techniques that minimize converter losses under suboptimal conditions, where the efficiency of the converter is below its peak value.

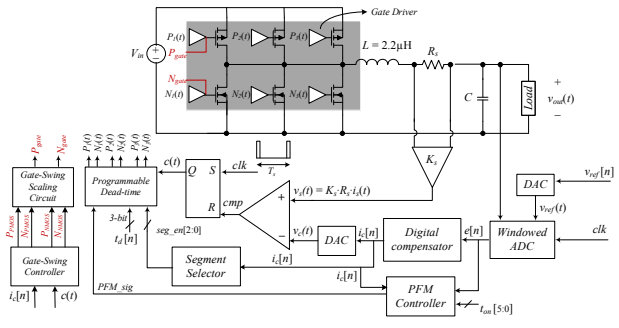


Fig.1.: Digitally controlled buck converter with instantaneous efficiency optimization.

Most of these efficiency optimization techniques rely on flexible digital controllers that can dynamically change parameters such as switching frequency[4], non-overlapping dead-times[5] or/and perform switching between pulse-frequency and pulse-width modes of operation[4]. In particular digital controllers have enabled wider use of efficiency optimization techniques that adjust the peak efficiency based on the load current in order to reduce losses over a larger load range. Two common techniques involve dynamically adjusting the number of power stage segments[1] and power MOSFET gate voltage[6]. Both of these techniques improve efficiency for a given operating condition by reducing the sum of conduction losses and the gate-voltage switching losses. These techniques have been implemented with digital controllers recently as shown in [1-3,5-7]. After the load transient occurs, the controller estimates the steady-state operating point and consequently adjusts the SMPS parameters to improve efficiency. Since the optimization occurs only in steady-state, the benefit of these methods becomes limited in portable electronics where the current drawn by the digital load changes frequently based on processing digital signal or different applications. Additionally since the dynamic load behavior causes the SMPS to operate in suboptimal region most of the time the optimization methods can become counterproductive resulting in efficiency degradation caused by the hardware overhead needed for the optimizer implementation. In [3] we presented a digitally controlled SMPS that provides instantaneous efficiency optimization, and as such is well suited for operation with highly dynamic loads. Based on the inherently available information about the peak current value, in each switching cycle, the system sets the mode of operation such that the sum of conduction and switching losses is minimized. The system presented in [3] uses a novel dual output switch-capacitor circuit to scale the gate-drive voltage. To implement the switch-capacitor circuit with multiple voltage levels, larger number of switches in addition to a large capacitor is required. This increases the size and cost of the power stage significantly resulting in a system that is not feasible for on-chip implementation. Furthermore, the losses on the switch-capacitor circuit mitigate the benefits of gate-drive voltage scaling in reducing total losses. The objective of this paper is to show a digitally controlled SMPS with

instantaneous efficiency optimization, shown in Fig.1, that does not use a secondary power supply for scaling gate voltage swing. The circuit technique used here is based on the method presented in [7]. However unlike [7], the implementation presented here is fully digital and does not require any passive components. Furthermore [7] does not propose a method for dynamically adjusting the gate voltage swing level as the load current changes. This can be achieved based on the readily available information in digital controller as shown in this work. Finally the controller presented here extends the operation of the system in [3] by dynamically switching to PFM mode at very light load conditions.

II. System Description and Principle of Operation

The system of Fig.1 operates as a modification of mixed-signal peak current program mode controller [8], where the voltage loop is digital and the internal current loop is implemented in an analog manner. The output voltage error is measured and converted into its digital equivalent $e[n]$ with a windowed analog-to-digital converter (ADC)[9]. Based on the error signal, a digital compensator creates the current reference $i_c[n]$. This value is passed to a simple ΣΔ digital-to-analog converter (DAC) [8], which sets the limit for the peak inductor current during each switching cycle and is also used in the optimization process. Using an analog comparator eliminates the need for an inductor current ADC used in fully digital CPM controller architecture such as shown in[10]. This hybrid approach results in more power and area efficient implementation of the controller. It has been shown in previous publications [9-11,13-14] that all the digital blocks in controller of Fig.1 can be implemented on chip with low power consumption and small area. The architecture shown in Fig.1 has been modified to allow implementation of efficiency optimization techniques based on segmentation and gate-voltage swing scaling. These modifications are discussed in the following sections and shown in Fig.1 and Fig.2.

A. Combined Efficiency Optimization Techniques

In the system shown in Fig.1, benefits of two known optimization techniques are combined to obtain a fairly simple implementation and high efficiency over the full range of operation. To obtain a high efficiency over the full range using segmentation only, a relatively large number of segments or a binary scaling of the transistors is required. This results in a fairly complicated layout of the transistors and gate drive circuit, increasing overall size of the power stage. On the other hand the limited power MOSFET gate voltage swing results in suboptimal operation at very light or higher load conditions. In the implementation shown in this paper, the benefits of both methods as well as of pulse-frequency-modulation operation (PFM) are utilized. As shown in Fig.1, the power stage is created of only three segments and the gate voltage of one segment is varied. As a result the power stage implementation is significantly simplified. At heavier loads two or three transistors of the segmented stage are active. At light-medium load range only one transistor is active and its gate voltage swing is modified. Finally at very light loads the controller operates the power stage in PFM mode.

B. Gate Voltage Swing Scaling Circuit

In [3] we proposed a dual output switch capacitor circuit for scaling the gate-drive voltage. The disadvantage of this implementation is large number of transistors required and system efficiency degradation due to the losses in the switch capacitor circuit. A different method for scaling the gate voltage of power MOSFETS is achieved by modifying the gate-driver circuit as shown in Fig.2. Also shown in the figure is the configuration of signals required to operate the circuit. The gate voltage scaling circuit is controlled by the gate swing controller block shown in Fig.1. This block consists of a controller Finite-State Machine (FSM) and the logic circuits required for generating the gating signals shown in Fig.2. As the load current changes based on the value of $i_c[n]$ the gate swing controller adjusts the pulse widths t_{PMOS} and t_{NMOS} and sets gating signals P_{PMOS}, P_{NMOS}, N_{PMOS}, N_{NMOS}. Consequently the gate-swing scaling circuit adjusts the voltage swings P_{swing} and N_{swing}, and sends the gate voltage signals P_{gate} and N_{gate} to the power MOSFETS. Compared to the Switch-Capacitor circuit used in [5] this circuit does not require any additional switches or passive components. Furthermore it does not incur additional losses in the system.

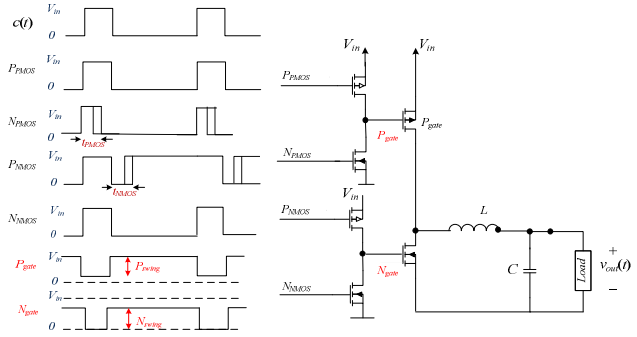


Fig.2 Gate Voltage Swing Scaling circuit and associated waveforms

III. Efficiency Optimization Controller Design and Mode Selection Criteria

This section briefly reviews losses in power MOSFETs and describes the criteria used for the efficiency optimization. It also discusses the modification in controller architecture of Fig.1 to implement efficiency optimization techniques.

The dominant sources of losses in high frequency SMPS are gate-drive and conduction losses associated with power MOSFETs[1-2,11-13]. The conduction loss can be described with the following equation [2,7]

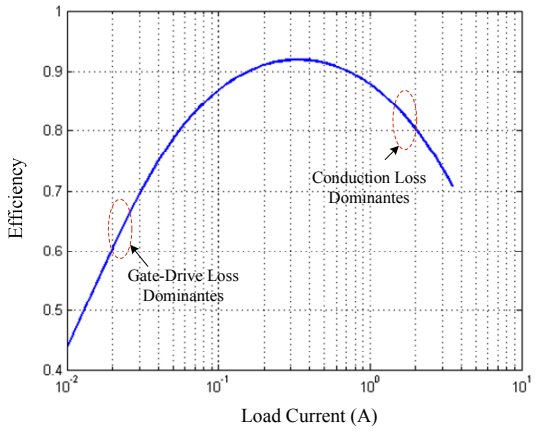
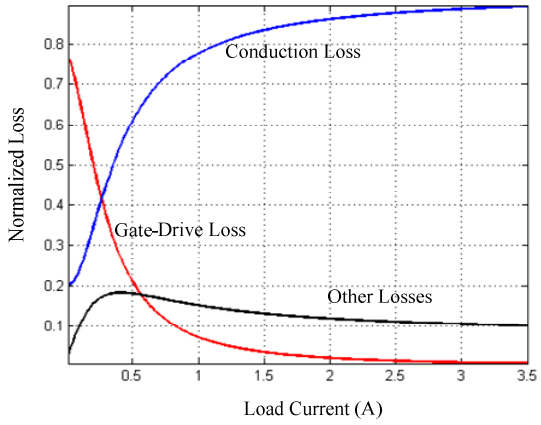


Fig3. a) Efficiency of a Converter ,V_{in} = 5,V_{out} =1.8, f_s =1MHz , K =1,L= 2µH



b) Each loss component as a percentage of total loss, over the load range

$$P_{cond} = i^2{}_{rms,P} \times R_{dson,P} + i^2{}_{rms,N} \times R_{dson,N} \qquad (1)$$

Where $R_{dson,P}$ and $R_{dson,N}$ are PMOS and NMOS on-resistances respectively. Ignoring the interconnect resistance, the R_{dson} of a segmented power stage having equally sized transistors can be modeled as

$$R_{dson} = \frac{R_{ds0}}{K(V_g - V_{th})} \qquad (2)$$

where R_{ds0} is defined by process parameters and width of one segment, K is number of segments in power stage, V_{swing} is the gate-voltage swing of the MOSFET and V_{th} is the device threshold voltage. The gate drive losses can be described with the following equation [7]

$$P_g = K(Q_{g,N} + Q_{g,P})V_g f_s = K(C_{g,N} + C_{g,P})V_{in} V_{swing} f_s \quad (3)$$

, where $C_{g,P}$ and $C_{g,N}$ are PMOS and NMOS gate capacitances associated with charging and discharging the MOSFETs in one segment and V_{in} is the gate drive supply voltage. Fig.3.a shows the efficiency of a converter running at fixed frequency, modeled based on these equations and Fig.3.b shows each loss component as a percentage of total loss, over the load range. It is evident that gate-drive losses are dominant at light load and conduction losses are dominant at medium to heavy load region.

For a given process technology the product of gate charge and on-resistance is fixed. Therefore to improve efficiency over the load range, the number of segments in the power stage and the gate drive voltage can be changed to continuously optimize the trade-off between the conduction loss and gate drive loss. As we mentioned before, to achieve high efficiency over the full range using only the segmentation technique will require large number of segments. This results in a fairly complicated layout of the transistors and gate drive circuit in on-chip implementation. Even a bigger problem is that the parasitic components of the layout can cause significant delays of some segments, unequal current distribution during switching transients, and consequent current breakdown of the circuit

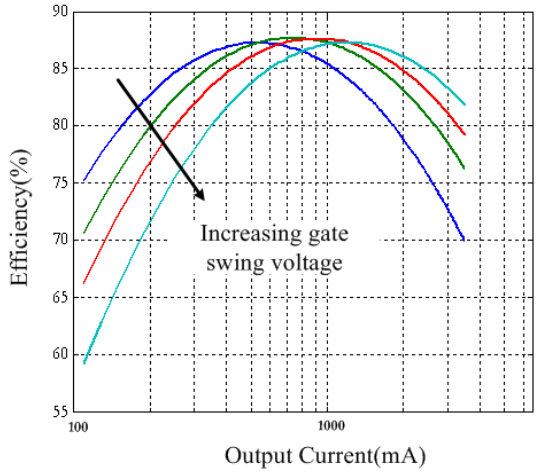
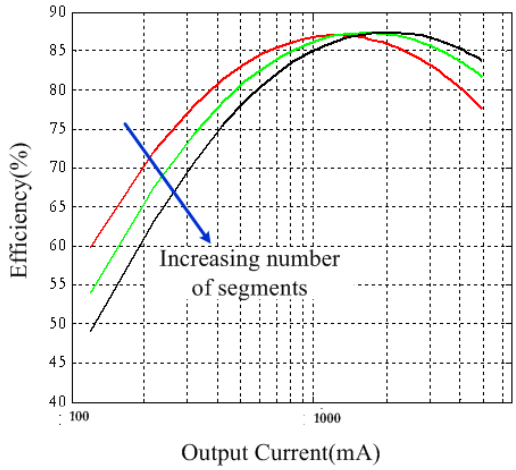
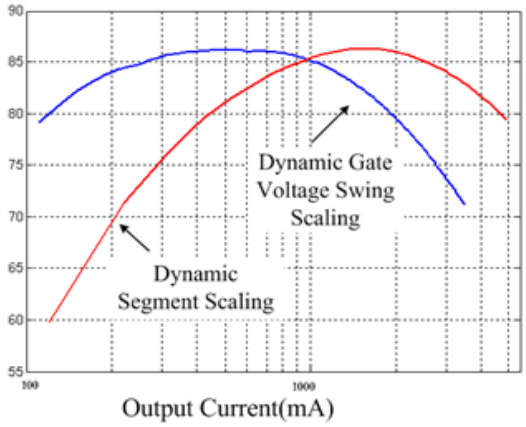


Fig4. a) Efficiency curves as the gate-voltage swing increases,



b) Efficiency curves as the number of segments increase



c)Efficiency optimization that can be achieved by the combination of two methods.

under heavy load conditions. Additionally as Fig.3.b, shows gate-drive losses are dominant at light to medium load current range. For this reason, applying gate-voltage swing scaling in this region, improves efficiency more effectively due to the dependence of P_g on gate voltage swing V_{swing} .To determine the optimal operating sequence for each load condition the efficiency of the system is modeled and shown in Fig.4. The trade-off between the gate-drive and conduction losses can be optimized by changing the gate voltage swing and number of segments at different output currents as shown in Fig.4.a and Fig4.b. For the load current range of 100mA-1A Fig4.a gives the current threshold values for scaling the gate-voltage swing in order to optimize the efficiency as shown in Fig4.c. For the load current range above 1A, Fig4.b gives the current threshold values for adjusting the number of segment in order to achieve the optimized curve shown in Fig4.c. Fig4.c demonstrates that combining both efficiency techniques will result in a far better efficiency improvement over the current range of 100mA-1A. For the load currents below 0.1A the controller operates the power stage in PFM mode to achieve additional savings. The threshold values are stored in gate-swing, segment and PFM controllers.

The controller implementation of Fig.1 significantly differs from traditional steady-state estimator-based controller [3]. In this case, the current reference $i_c[n]$ is used not only for the output voltage regulation, but also as the signal for governing on-line optimization. Based on $i_c[n]$ value and the stored threshold values, *gate swing controller* , *segment selector* and *PFM controller* configure the power stage so that for the given peak current total losses are minimized.

IV. Experimental Results

An experimental system was build based on block diagram of Fig.1to verify the operation of the system. The 5V-1.8V DC-DC converter consists of three segments with L = 2.2 µH, C = 40 µF, and f_{sw} = 1 MHz. The ADC and programmable reference voltage were implemented on an application specific integrated circuit and previously discussed in [8]. The controller including the ΣΔ DAC is implemented on an FPGA board with the exception of ΣΔ DAC filter and the comparator.

A. *Steady state efficiency improvements*

Fig.5 shows the steady-state efficiency improvement results obtained with using the optimization method discussed in this paper. In the light to medium load region, compared to the non-optimized operation the efficiency is improved by as much as 18% using gate-voltage swing scaling. Additionally in the medium range where segment adjustment is implemented the efficiency is improved by 8%. Fig.5. also shows that combing the two methods with PFM operation as described in this paper results in improved efficiency compared to implementing only one method.

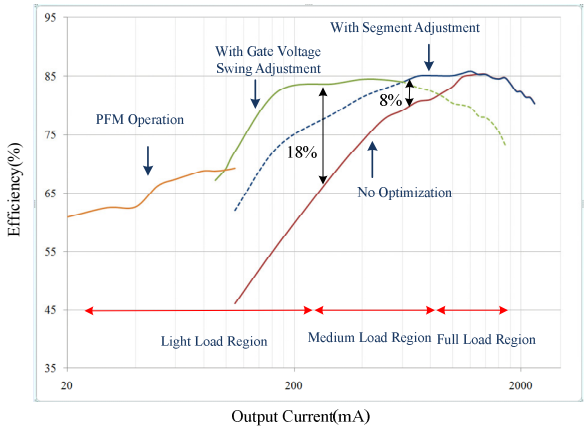


Fig.5. : Efficiency improvements with the optimization controller presented here.

B. *Dynamic behavior*

Fig.6.a shows the dynamic response of the converter with segmented operation. Upon a load transient, the controller adjusts the segment configuration as $i_c[n]$, shown at the output of ΣΔ DAC as $v_c(t)$ changes. Fig.6.b shows the transient response of the converter with gate-swing scaling operation. As the load changes from 500mA to 1A, the gate swing controller updates the pulse width t_{PMOS} and t_{NMOS} control signal, *pulse_s*l[n] thereby increasing the gate voltage swing dynamically to offset the effect of increased conduction losses in power MOSFETs. Fig .7 shows the operation of the system in PFM mode. As the load changes to below 0.1A, the PFM controller is activated based on the value of $i_c[n]$. The controller disables the low-side switch, adjusts the voltage swing of the high-side switch, P_{gate}, to full scale and consequently runs the system in PFM mode.

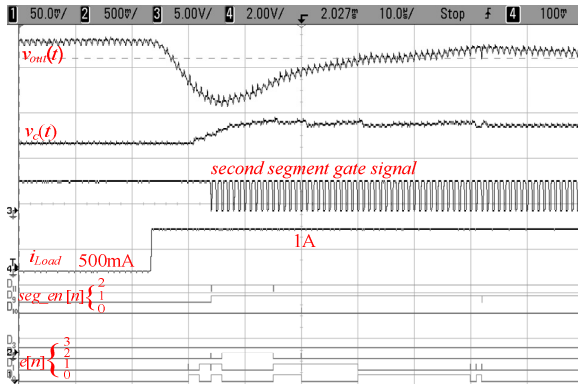


Fig.6.a: Dynamic response with segmented operation. Ch1: Output converter voltage (50mV/div); Ch2: analog current command (500mV/div); Ch3: Second Segment gate signal (5V/div) ; Ch4: load step command; D0-D3: ADC error e[n]; D9-D11: Segment Enable signal; Time scale is 10µs/div.

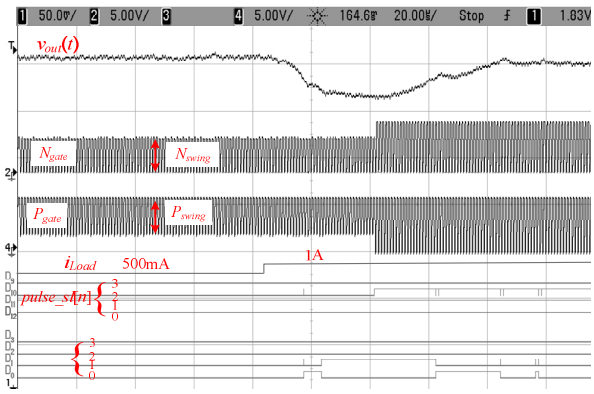


Fig. 6.b.: Dynamic response with gate-swing scaling operation. Ch1: Output converter voltage (50mV/div); Ch2: NMOS gate-swing voltage (5V/div) ; Ch4: PMOS gate-swing voltage(5V/div); D7: load step; D0-D3: ADC error, e[n];D9-D12:4 MSB bits of pulse select signal; Time scale is 20µs/div.

Fig.8 compares the dynamic response of the converter under two different cases, with the optimization controller presented in this work and with steady-state estimation-based optimizer. The operation of this estimation-based optimizer is described as follows. Upon detecting a load transient all segments are turned on to avoid over-stressing the power MOSFETs for the worst case scenario, the controller remains in this state until the steady-state error $e[n] = 0$ is detected (period 1). The controller then counts for few cycles while $e[n] = 0$ (period 2) and adjusts the segments for the new load current value. Also shown on the figure are the measured losses for each controller configuration at the load current. These show that the steady-state estimation-based optimizer will result in extra energy consumption during transients. The energy consumption under both methods is measured at different load step frequencies. Fig. 9 shows that dynamic optimization controller results in 20% peak energy savings.

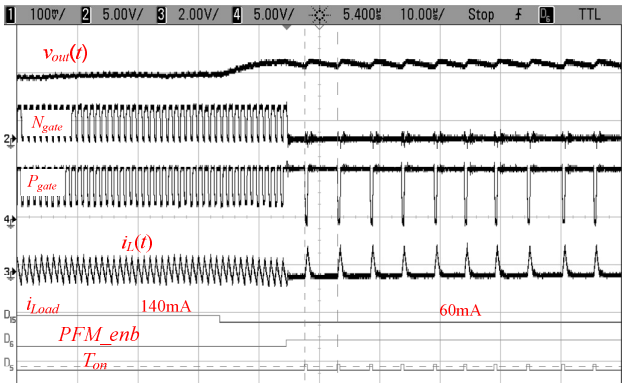


Fig.7.: Dynamic response with PFM Operation: Ch1: Output converter voltage (100mV/div); Ch2: NMOS gate-swing voltage (5V/div) ; Ch4: PMOS gate-swing voltage(5V/div); Ch3: Inductor current (2A/div); D15: load step;

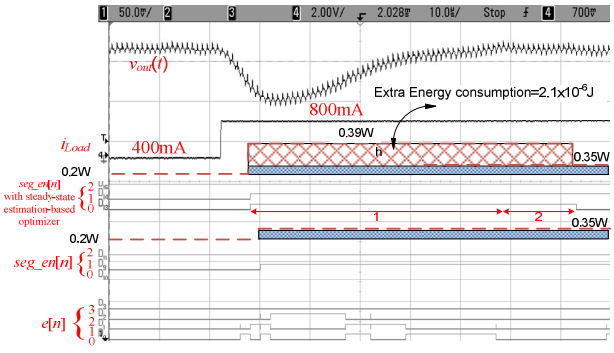


Fig.8.: Dynamic response with estimation-based optimizer and instantaneous online optimizer: Ch1: Output converter voltage (50mV/div); Ch2: load step command. D0-D3: ADC error, e[n];D9-D11: Segment Enable signal for instantaneous optimizer; D13-D15:Segment Enable signal for steady-state estimation-based optimizer ;

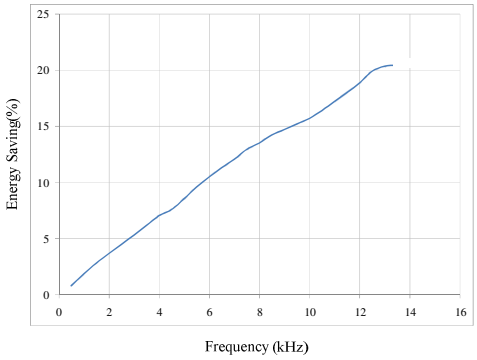


Fig.9. : Energy savings with instantaneous online optimizer versus estimation-based optimizer

V. Conclusion

In this paper a digital controller is introduced that dynamically changes mode of operation in a segmented power

stage to maximize power processing efficiency when highly dynamic loads are supplied. The controller operates as a mixed-signal peak current program mode voltage regulator, where a digital current reference is created and used for the efficiency optimization. The losses are minimized by combining two methods. Based on the current reference, in each switching cycle, the optimal number of power switch segments and gate voltage swing levels are set through the controller. A prototype system was build to verify the effectiveness of the system. The results show that the on-line optimization improves efficiency by as much as 18% in the light load region and 8% in medium load.

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