Oversampled Digital Power Controller with Bumpless Transition Between Sampling Frequencies

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***Abstract*—In today's digitally controlled power supplies fast analog-digital converters sampling at a multiple of the switching frequency are used to reduce the latency time of the conversion. Conversely, in many cases the actual compensator is still sampled at the switching frequency which introduces an additional latency time. To reduce this latency time, a new compensator architecture is presented in this paper which allows a bumpless transition between two compensators operating at two different sampling frequencies. Operating at the switching frequency during steady-state provides noise suppression, while operating at the full "oversampling" frequency during transients reduces the compensator's latency time significantly. A method for the bumpless transition between the two compensators is presented which is simple to implement and can be easily integrated into existing control architectures. Experimental verification demonstrates clear performance gain over existing control architectures.**

I. Introduction

With the demands for increased output power, reduction in the output voltage and the need for higher efficiency, today's switched mode power supplies (SMPSs) are challenged to deliver good transient performance using smaller/cheaper components. While digitally controlled SMPSs are becoming more popular, most digital control schemes are simply a direct replacement of their analog counterparts and still use simple linear (PID) compensators. With today's digital systems, alternative more complex control schemes which have been investigated in recent years are now applicable in practice.

Time-optimal or charge-balanced control achieve the "fastest" possible settling time, combined with minimal voltage deviation [1]–[4]. However to be fully effective, accurate knowledge of the power stages components, high computational burden and high-performance analog components are generally required. Some implementations counteract these drawbacks by assuming certain relationships or estimating parameters. The reaction to partial load steps is often an issue for these types of schemes.

An alternative control scheme, "Linear-Non-Linear" control, uses a fast hysteretic loop in parallel with a PID control loop which improves the transient performance significantly [5]–[8]. The design challenge here is the definition of the comparator thresholds controlling the additional loop. An analytical method for their calculation has not been published to date.

In [9], an "event-based" system is demonstrated which utilizes an asynchronous analog-digital converter (ADC) to trigger the control loop every time the output voltage changes. The control loop is modified in such a way that the compensator can be executed with a non-fixed sampling frequency by dynamically scaling the coefficients to "simply emulate" an analog (continuous time) compensator. The system reduces the latency time, but can suffer from high-frequency noise as there is no limitation of the sampling frequency by the ADC. Also, asynchronous ADCs are not common in power designs (yet) and can provide a potential hurdle in practical applications due to their power consumption and noise issues.

All of these system architectures have a common property, i.e. the reduction of the sampling delay of the control loop with the introduction of additional asynchronous input elements, typically comparators. To reduce the sampling introduced delay in a conventional digital loop, most of today's digital power controllers use already ADCs with effective sampling rates much higher than the switching frequency. While special "power" ADCs are currently investigated in the research community, e.g. [10], most of the ADCs used are based on a pipeline architecture which requires multiple cycles to convert a single input value. To reduce their conversion times, they are subsequently clocked with multiples of the desired sampling frequency, typically the switching frequency. However, in most cases only one sample per switching cycle is processed by the compensator, while the remaining samples are "dropped."

Recently so-called "oversampled" control methods have also been investigated [11]–[13]. Like most existing control schemes, the output voltage signal is sampled at a higher frequency than the switching frequency. However, unlike most existing schemes, each sample is processed by the compensator. The reduced latency time, due to the faster sampling, allows the control designers to use compensators with higher bandwidths. Conversely, this oversampled approach can suffer from several drawbacks like for example more demanding ADC requirements due to an increased sampling frequency, and sensitivity to high frequency noise. While fast, application-specific ADC architectures and implementations have been presented in the literature [10], the increased sensitivity to high frequency noise, e.g. the output ripple voltage, remains a design issue.

In [12], [13], an additional notch filter is introduced into the control loop to remove noise at multiples of the switching

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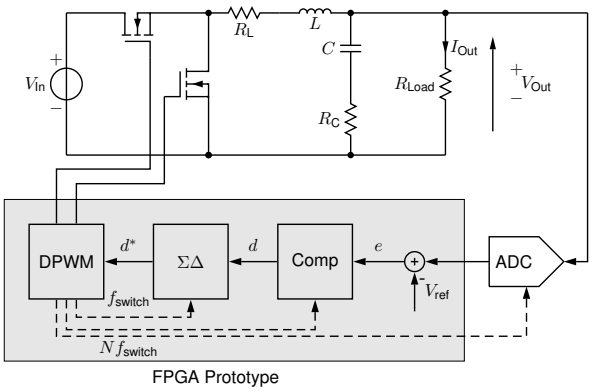

Figure 1. System block diagram

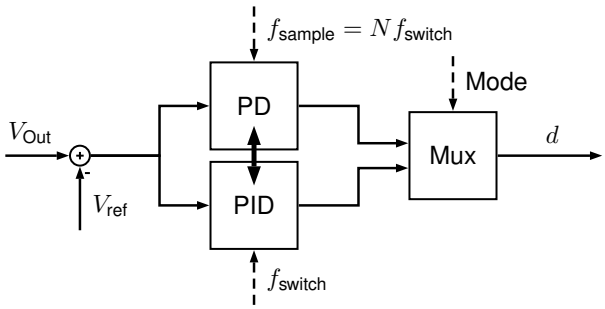

Figure 2. Compensator block diagram

frequency. The order of this digital filter depends on the oversampling factor, e.g. the ratio between the switching and the sampling frequency, and increases the design complexity significantly; in particular when the oversampling factor is not a power of two.

In this paper, a new approach to address the problems of oversampled compensators is presented. The system features a compensator architecture with variable sampling frequency, comprised of two linked compensators. During steady-state operation, a robust compensator running at the switching frequency is active (steady-state mode). This provides good noise suppression due to the natural sampling of the output voltage. A "faster" compensator running at the full sampling frequency is active during load transients (transient mode) reducing the compensator's latency time. A proper (bumpless) transition between the modes is detailed which allows the application of this compensator in practice. Implementation on a FPGA and experimental results for a single-phase buck converter are presented.

II. System Overview

The control system discussed in this paper (Fig. 1) consists of an analog-digital converter (ADC), a compensator (Comp), a sigma-delta modulator (ΣΔ) and a digital pulse

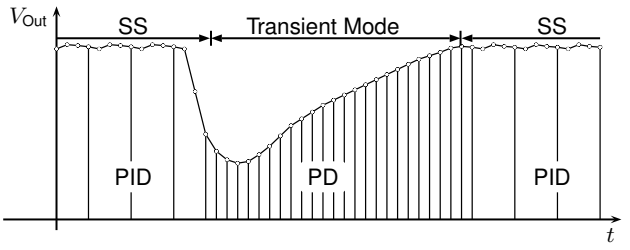

Figure 3. Mode of operations

width modulator (DPWM). The ADC samples the output voltage of the power stage at a frequency f_{sample} which is generally N-times the switching frequency f_{switch}. The compensator operates at a variable frequency which is either the sampling frequency (oversampled case) during a transient or the switching frequency during steady-state. The sigma-delta modulator increases the effective resolution of the DPWM in order to improve operation during steady-state and to reduce the design complexity of the DPWM. The DPWM generates the switching signals for the power converter including any required dead-time.

Internally the compensator (Fig. 2) contains two separate, but linked compensators working at the sampling and the switching frequency respectively. A bumpless transition is introduced to allow a smooth change between the two frequencies. During steady-state, a PID compensator operating at the switching frequency is utilized as it provides zero steady-state error and good robustness against noise and system tolerances. Also the propagation of the output ripple voltage through the control loop is prohibited due to sampling at the switching frequency. A fast PD compensator operating at the full ADC sampling frequency is active during transients which reduces the compensator's latency time. The proposed compensator allows a reduction of settling time and maximum deviation of the output voltage compared to a standard PID compensator.

III. Bumpless Compensator Architecture

With reference to Fig. 3, the compensator has two modes of operation. These are now discussed in more detail along with the mechanism of detecting and switching between these modes.

A. Modes of Operation

PID- and PD-type compensators have been used separately in the past. PD compensators are used extensively in several different applications for their ease of implementation and good transient performance. On the other hand, one acknowledged disadvantage is the non-zero steady-state error. Due to a lack of integral action, a non-zero output signal always requires a non-zero input value which leads intrinsically to a non-zero steady-state error. Commonly, this is addressed either by using high DC loop gains that minimize the error, or with additional integral action which changes the reference value of

the control loop to compensate for the steady-state error. The additional integral action can also be replaced by a constant bias signal, typically referred to as the "operation point." PID compensators, on the other hand, provide good robustness and zero steady-state error, but do not offer the same transient performance.

In the proposed control scheme, both compensators are designed independently according to well-known techniques employed in compensator design for SMPS. The only system specific constraints are structure (PID and PD) and sampling frequency (f_{switch} and f_{sample}). By introducing a simple yet effective method to change between the two different compensators (bumpless transfer), the advantages of the two different compensator types are combined.

B. Design Procedure for a Bumpless Transition

Bumpless transfer between operation modes has been investigated in the past. A common application is the transfer between manual and automatic operation mode in a PLC system. For PID/PD compensators, bumpless transfer can be guaranteed if the compensator's output does not change significantly during the transition [14]. While this method has been mainly employed for continuous-time compensators in the past, it is here utilized to change between two discrete-time compensators which are also discretized with two different sampling times. Note that bumpless transition between the two compensators does not influence the individual stability criteria of the individual designs.

In the detailed control scheme, two different transitions are possible: Steady-state to transient mode and transient to steady-state mode. The first does not necessarily have to be bumpless rather is should be fast, as it directly influences the system's response to load transients. The later must be smooth (bumpless), as it occurs after load transients when the output voltage has nearly recovered. If this is not guaranteed, the compensator will switch back to transient mode leading to undesired oscillations between the two modes. To ensure bumpless transition, a method is now detailed which is simple and easy to implement.

Assuming the PD compensator is currently active and the condition for steady-state operation becomes valid, the compensator switches to steady-state mode. During this transition, the compensator's governing equation changes from a PD type

$$d_{\text{T,N}} = d_{\text{bias,N}} + K_{\text{P,T}}\, e_{\text{N}} + K_{\text{D,T}}\,(e_{\text{N}} - e_{\text{N-1}})\ , \qquad (1)$$

to a PID type

$$d_{\text{SS,N}} = K_{\text{P,SS}}\, e_{\text{N}} + K_{\text{D,SS}}\,(e_{\text{N}} - e_{\text{N-1}}) + d_{\text{i,N}} \qquad (2)$$

$$d_{\text{i,N}} = d_{\text{i,N-1}} + K_{\text{I,SS}}\, e_{\text{N}}\ , \qquad (3)$$

where $K_{\text{P,T}}$, $K_{\text{D,T}}$ are the gains during the transient mode, and $K_{\text{P,SS}}$, $K_{\text{D,SS}}$, $K_{\text{I,SS}}$ are the gains during the steady-state mode. $d_{\text{bias,N}}$ is an optional bias signal for the PD compensator which further reduces the steady-state error.

The perturbation of the output signal during the transition from (1) to (2) can therefore computed as

$$\Delta d = d_{\text{SS,N}} - d_{\text{T,N}}\ , \qquad (4)$$

which should be kept as small as possible to ensure a bumpless transition. To do so, the contributions of the three independent parts to the overall perturbation are now described, followed by a simple method to compensate for this.

Firstly, the proportional part changes from $K_{\text{P,T}}\, e_{\text{N}}$ to $K_{\text{P,SS}}\, e_{\text{N}}$, resulting in a difference of $\Delta d_{\text{D}} = (K_{\text{P,T}} - K_{\text{P,SS}})\, e_{\text{N}}$, where e_{N} is the error signal of the current cycle.

Secondly, the derivative part changes from $K_{\text{D,T}}\,(e_{\text{N}} - e_{\text{N-1}})$ to $K_{\text{D,SS}}\,(e_{\text{N}} - e_{\text{N-1}})$ where it must be noted that the time interval for the computation changes from T_{sample} to T_{switch}. This results in a dependency of the output perturbation on the gain values and the current/past error signals which can be simply expressed as an equation, but is not favourable for hardware implementation. As it will be detailed later in this paper, the transition between transient and steady-state mode occurs only with small derivative values, hence leading to a negligible contribution of the differential part.

Thirdly, bias signal and integral part change during the transition. However, if the integral part of the PID compensator is used as bias signal during PD operation, two problems are solved at the same time. The steady-state error during PD operation is improved, while its contribution to the perturbation during mode transition is also eliminated.

This results in an overall perturbation

$$\Delta d = d_{\text{SS,N}} - d_{\text{T,N}} = (K_{\text{P,T}} - K_{\text{P,SS}})\, e_{\text{N}} \qquad (5)$$

during mode transition. As previously mentioned, the perturbation of the actual output signal should be kept as small as possible. This can be done by implementing an additional update of the integral action during the transition between the operation modes, where the update factor is calculated as

$$d^{*} = (K_{\text{P,T}} - K_{\text{P,SS}})\, e_{\text{N-1}} \qquad (6)$$

and is added to (3). This additional equation, a reconfigurable PID/PD compensator and its controlling state-machine can be easily implemented into today's systems.

C. Detection of Operation Modes

The detection of the different operation modes is a key design issue of the proposed control system where several different constraints have to be taken into account.

The first consideration is the availability of the sampled output voltage. Two different scenarios are possible:

(a) The output voltage is sampled at "full speed" during transient mode and at the switching frequency during steady-state operation. While this can save energy during steady-state due to the reduced sampling rate (depending on the selected ADC architecture), it introduces a latency time up to one switching cycle. To counteract, additional hardware, e.g. comparators, can be used to detect transients between two samples and signal the ADC to sample at "full speed." However, assuming the ADC allows an instantaneous change in sample frequency, the compensator still has to wait for the arrival of at least one sampled value, prior to taking action.

(b) The output voltage is always sampled at "full-speed," while the compensator is executed at different frequencies.

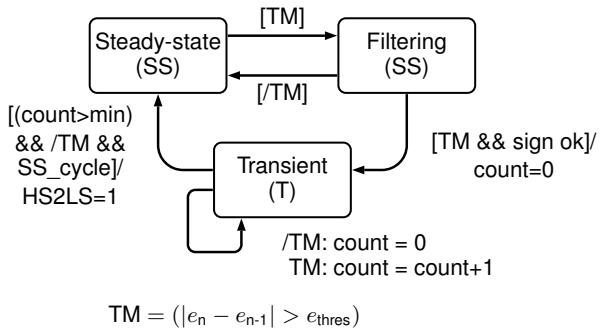

Figure 4. Operation mode state machine

This method is used for the presented system as it omits the need for additional comparators and enables the computation of the discrete derivative of the output voltage, i.e. the difference between two consecutive samples, at all times. The result is compared with a predefined threshold (e_{thres}) and used as criteria (TM) for transient detection.

The second consideration is the selection of the detection threshold which is a trade-off between noise resistivity and speed. If the threshold is too high, the system detects only large transients and misses small/medium ones, referred to "false negatives." This degenerates the reaction time. On the other hand if the threshold is set too small, the control system can pick up noise very easily and can be unintentionally forced into transient mode ("false positive"). If false positives occur frequently, they can become visible at the output voltage, as a bumpless transfer is only implemented for the transition from transient to steady-state mode, not vice versa.

In order to reduce the transient detection threshold and to improve the system response, an additional "noise filtering" principle has been developed. It filters "single-sample" spikes, i.e. error signals exceeding the transient threshold for only one sample, and allows a significant reduction of the detection levels. This simple filter method is implemented as a small state-machine (Fig. 4) controlling the operation mode of the compensator. Assuming the system is in "steady-state" operation and the derivative exceeds a predefined threshold, indicated to the state machine by the control signal TM, the system enters a "noise filtering" state. At the arrival of the next sample, the system enters "transient mode" only if two conditions are met, i.e. when the derivative exceeds the transient threshold (signal TM) and when it has the same sign as the previous derivative. This ensures the filtering of single sample spikes, which create two large derivative values with alternating sign bits. Only identical signs imply a continuing deviation of the output voltage in the same direction. For this design, the transition from transient to steady-state mode also features a filter technique. The state-machine ensures that the steady-state condition is met for a predefined number of consecutive samples (min) prior to returning to steady-state operation. Also the return to steady-state mode only occurs at the main sampling interval, so that the steady-state compensator can restart operation immediately and bumpless transition is ensured.

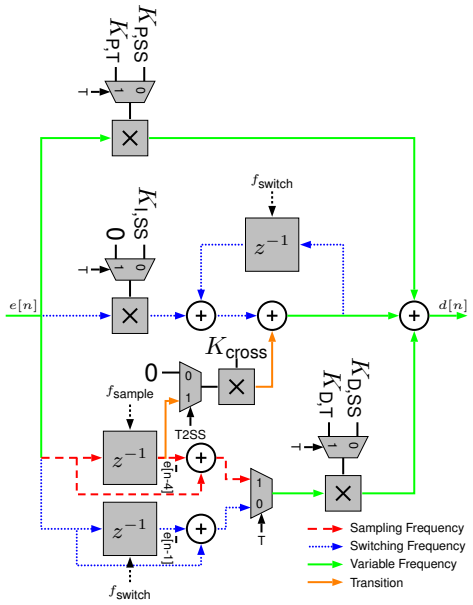

Figure 5. Implementation of the proposed compensator

It should be noted that both filter conditions influence the applicability of the system. If the transition between the modes cannot occur "fast enough" or the compensator is forced to remain in a certain operation mode, the system's response to load transients is compromised. In particular, the reaction to fast repetitive load transitions can course problems in such a case. The detailed filter procedures do not suffer from this drawbacks.

IV. Implementation

The implementation of the proposed compensators architecture in today's digital processes and the integration into existing power converters is straight-forward. "Off-the-shelf" ADCs can be employed since the required oversampling factor is small (e.g. an oversampling factor of four is used for the experimental prototype). For comparison, other approaches use much larger oversampling factors which even require specialized ADC implementations. The proposed compensator design follows standard digital signal processing techniques and can be easily implemented using any digital design method, e.g. Verilog HDL.

Unlike most existing compensators which are implemented as digital IIR filters using a direct or canonic structure, the proposed implementation illustrated in Fig. 5 splits the compensator into three separate parts (data paths): proportional, integral and derivative. This enables a simple practical integration of the bumpless transition method into the compensator. To increase hardware utilization, most of the hardware is shared between the two compensators. The proportional and

Table I
COMPENSATOR HARDWARE RESOURCES

Block	PID	Additional Hardware
Multipliers	3	1
Adders	2	1
Subtractors	1	1
Registers	2	1
Multiplexers		5
Control FSM		1

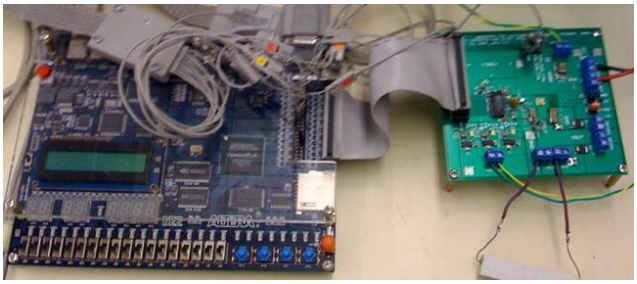

Figure 6. Experimental prototype board

derivative parts feature selectable gains, so that the coefficients of the data paths can be chosen according to the active operation mode. Two separate data paths for the computation of the derivatives (running at f_{sample} and f_{switch}) are required, as the derivative is used to detect the transient condition and needs to be computed for each sampled value. This leads to separate subtracters, while the multiplier is still shared between the two paths. Bumpless transition is ensured by an additional signal path updating the integral action during the transition into steady-state mode. The update coefficient K_{cross} should be selected according to (6) to ensure a bumpless operation.

The compensator structure is dynamically changeable by using the various different execution patterns of the individual data paths. This execution is controlled by a state-machine (Fig. 4) and is dependent on the current operation mode. With reference to Fig. 5, data paths can be executed

1) only during steady-state operation (switching frequency).
2) continuously with the sampling frequency (sampling frequency).
3) with a variable frequency dependent on the operation mode (variable frequency).
4) only during the bumpless transition between the operation modes (transition).

In Table I, the required hardware resources for the proposed compensator are compared with an implementation of a standard PID compensator, where the second column shows the hardware required for a conventional PID compensator. The third column details the additional hardware required for the presented scheme. Along with multiplexers for the selection of the compensator coefficients and a second derivative computation, only one additional signal path for the bumpless transition is required. This can be added to existing designs without excessive increase in area.

Note that the detailed implementation is kept flexible for FPGA implementation/prototyping and is not optimised for low area consumption. Optimization techniques, like an optimization of resolution, resource sharing through a sequential/pipelined operation, or fixed coefficient selection (favourably with a power of two), can reduce the area consumption significantly. Details are given in [15], [16]. Also an implementation in software for execution on digital-signal-processors (DSPs) is possible [17], [18].

V. EXPERIMENTAL VERIFICATION

The proposed control system has been verified on a FPGA experimental platform (Fig. 6). The power stage is a single phase buck converter with $f_{\text{switch}} = 500\,\text{kHz}$, $L = 950\,\text{nH}$, $C = 250\,\mu\text{F}$ and $R_{\text{C}} \approx 0.5\,\text{m}\Omega$. An "off-the-shelf" ADC with a sampling frequency was chosen with $f_{\text{sample}} = 2\,\text{MHz}$ (oversampling factor 4), trading off performance gain and ADC complexity. The control scheme together with all other required digital hardware blocks has been implemented on an Altera Cyclone 2 FPGA. The bode plots of both compensators are shown in Fig. 7. The cross-over frequencies are 20 kHz and 55 kHz with phase margins of about 45°.

The performance of the proposed control system is shown in Fig. 8. The maximum deviation for a 15 A load step is 175 mV with a settling time of 13 µs. This is a reduction of about 50% compared with a naturally sampled PID. The achieved improvements can be used to reduce the output capacitance without degenerating the system's performance. Signal D_2 shows the activity of the compensator where the transition between the two operation modes is clearly visible. This transition is not visible in the output voltage hence leading to a smooth change (bumpless transfer) between the operation modes.

VI. CONCLUSIONS

A new approach to improve system response of power converters based on a variable sampling frequency has been presented. To combine the benefits of naturally sampled and oversampled technique without suffering from their drawbacks, the operation frequency of the proposed compensator is changed according to demands. Oversampling during transient and natural sampling during steady-state operation combine the robustness and performance of both domains. A simple transition scheme, to allow the bumpless transition between the two operation modes and hence its applicability in practice has been outlined. Implementation and integration is relatively simple and only requires a small overhead compared with standard digital compensators used today. The control scheme has been implemented in Verilog HDL and verified on a FPGA platform with a single phase buck converter. The performance of the proposed oversampled compensator exceeds naturally sampled designs without suffering from the drawbacks of standard oversampled compensators.

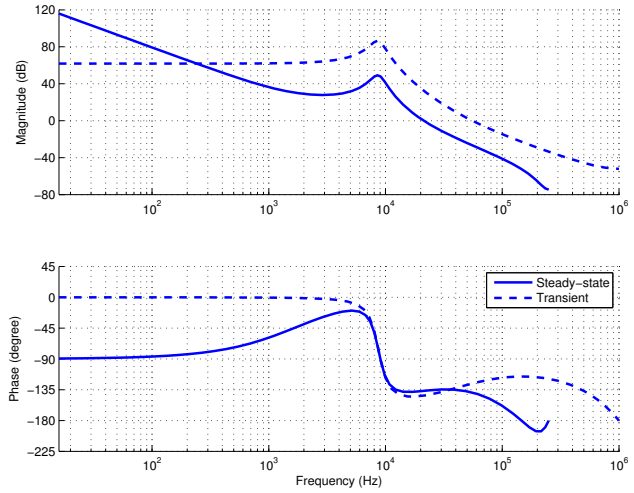

Figure 7. Bode plot of steady-state and transient compensator

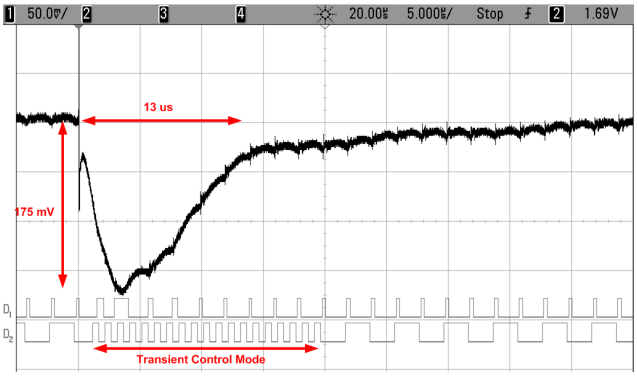

Figure 8. Transient response of the proposed control scheme

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