Minimum Deviation Digital Controller IC for Single and Two Phase DC-DC Switch-Mode Power Supplies

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***Abstract*— A digital PWM voltage mode controller integrated circuit (IC) for high-frequency dc-dc switching converters achieving virtually minimum possible, i.e. optimum, output voltage deviation to load transients is introduced. The IC is implemented with simple hardware, requiring small silicon area, and can operate as a single-phase or a two-phase controller. To minimize the area and eliminate known mode transition problems of the optimal response controllers, two novel blocks are combined. Namely, an asynchronous track-and-hold analog-to-digital converter (ADC) and a "large-small" signal compensator are implemented. The ADC utilizes a pre-amplifier and only four comparators having approximately eight times smaller silicon area and power consumption than an equivalent windowed flash architecture. The "large-small" signal compensator consists of two parts, a digital PID minimizing small variations and a zero-current detection-based compensator suppressing large load transients. The large-signal compensator requires no extra calculations and has a low sensitivity to parameter variations. It utilizes a synchronization algorithm and the PID calculation results to obtain a bumpless mode transition and stable response to successive load transients.**

The IC occupying only 0.26 mm^2 silicon area is implemented in a CMOS 0.18µm process and its minimum deviation response is verified with a single and dual-phase 12 V-to-1.8 V, 500 kHz 60/120 W buck converter.

I. INTRODUCTION

Switch-mode power supplies (SMPS) used in consumer electronics, portable applications, and computers, are required to meet stringent voltage regulation requirements [1], [2] using a cost-effective implementation occupying a small volume. The regulation is usually achieved with on-chip integrated controllers, which, in analog implementation, occupy a silicon area as small as 0.6 mm^2 [3]. The integrated controllers most frequently utilize voltage mode pulse-width modulation, where a PID compensator provides an accurate output voltage regulation and robustness of the system over a wide range of operating conditions. However, due to inaccurate high-frequency dynamics of averaged small-signal models of the converters, usually used in the conventional PID design [4], the response time of the compensator is fairly limited. As a result, the reactive components of the power stage output filter are usually oversized. Furthermore, since the obtained linear time-invariant (LTI) model is based on the small-signal variations assumption, it might not be fully valid for large excitations, frequently occurring in modern SMPS during large load changes.

Since the controller speed is closely related to the output voltage deviation, i.e. the size of the filtering components, various analog and digital linear [5]-[7] and nonlinear [8]-[17] control methods for improving the speed of the controller, have been investigated.

Arguably, the most promising results are demonstrated though various digital implementations of the optimal control [11]-[16], where the recovery from a transient is achieved through a single on-off switching action.

Even though the optimal control methods have demonstrated superior performance compared to conventional solutions, they have not been widely adopted due to one or more of the following four problems: i) Instability caused by transitions between steady state and dynamic modes, i.e. chattering; ii) High sensitivity to quantization effects and converter parameter variations, iii) Overly complex hardware required for implementation requiring a large silicon area for implementation; and iv) Inability to react to consecutive load steps occurring during the dynamic mode.

The main goal of this paper is to introduce a novel digital controller IC that achieves virtually minimal possible, i.e. the optimal, deviation during load transients and is implemented with fairly simple hardware, occupying a small silicon area,

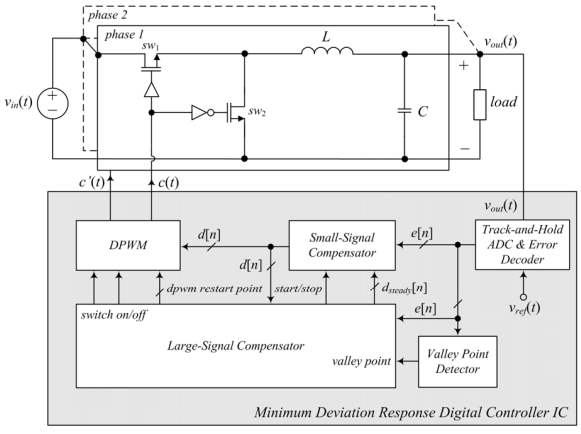

Figure 1. A dual-phase buck converter controlled by the combined "large-small" signal digital controller.

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without suffering from the above mentioned problems. Depending on the load conditions, the controller, shown in Fig.1, operates either as a small-signal or a large-signal compensator and provides smooth, i.e. bumpless, transition between the static and dynamic modes. The IC also provides the optimal deviation response to narrowly time-spaced load transients and has a low sensitivity to power stage parameter variations and quantization effects. Furthermore, the IC can either regulate operation of a single phase converter or that of a two-phase interleaved topology. To reduce the power consumption and silicon size of the controller while maintaining sufficient accuracy and speed a novel Track-and-Hold ADC architecture is also developed and implemented.

In the following section, the operation of the IC with a single-phase buck converter is explained and then extended to a dual-phase case. Special attention is given to mode transition problems and the resulting overshoot. Section III discuses problems related to overly complex hardware required for the implementation of optimal digital controllers and describes novel hardware-efficient architectures of major controller blocks. Particular attention is devoted to the application specific ADC design that, compared to conventional architectures, takes about 8 times smaller silicon area. Section IV presents experimental results verifying the operation of the controller with both single phase and two-phase buck converter.

II. PRINCIPLE OF OPERATION

The controller of Fig.1 has two control modes. Around steady state, in small-signal mode, the operation of the power stage is governed by a conventional voltage mode digital PWM regulator [21, 23]. Based on the output voltage error value $e[n]$, produced by the ADC, a control signal for digital-pulse width modulator (DPWM) $d[n]$ is created, to keep the output regulated.

The large signal compensator constantly monitors $e[n]$ and $d[n]$, and, while in steady-state ($e[n]=0$), calculates a duty ratio value $d_{steady}[n]$ by averaging $d[n]$ over several switching cycles. As it will be explained soon, this value is later used to obtain a bumpless transition between two compensators while a large load transient is suppressed.

Operation of the large signal compensator is fairly simple. During transients, when $e[n]$ exceeds a specified threshold value, it takes the active control role. It immediately turns on or off the main switch, depending on the sign of $e[n]$ (type of the transient), and disables the operation of the small-signal compensator. The controller's state remains unchanged until the inductor current $i_L(t)$ is equal to the load current $i_{load}(t)$. At that point, capacitor current changes its sign and reaches its peak or valley point. For a given converter topology, this value is also the minimum achievable voltage deviation, i.e. the smallest possible undershoot/overshoot. At this point a synchronization algorithm reactivates the DPWM, and subsequently the PID compensator, such that a smooth transition between the modes is achieved.

It can be seen that reaching the peak or valley point is a trivial task; however, due to quantization and sampling errors the detection of the peak or valley point will always be delayed and due to the utilization of small inductances (typically less than 500nH) may result in relatively large charge injection and consequent stability problems. The following section illustrates the problem and provides quantitative motivation for the controller presented in this paper.

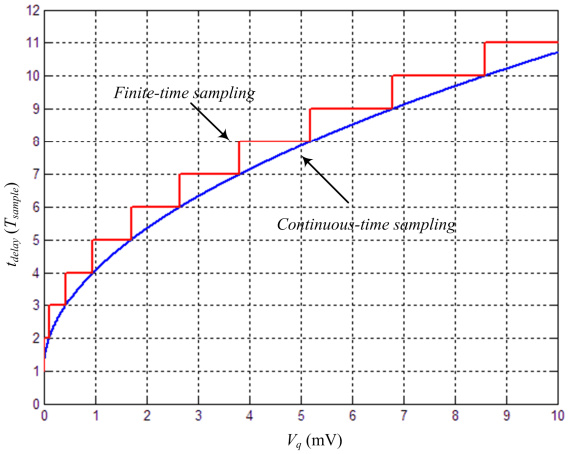

Figure. 2. The influence of ADC quantization step V_q and sampling rate on the worst-case delay time t_{delay} generating voltage overshoot. (T_{sample} is 62.5 ns)

A. Mode Transition

In the presence of in-accurate valley or peak point detection any subsequent control actions dependent on it will only contribute to a greater error. This is particularly true for existing time-optimal controllers [11]-[16] which attempt to compensate the lost capacitor charge through a single on/off control action. This action is usually followed by second mode of operation, where a conventional PID compensator is active to provide stable steady-state operation.

These time-optimal controllers are usually burdened with detecting both the correct valley point and voltage deviation in order to calculate the proper t_{on} and t_{off} times; however, it can be shown that a worst-case delay equal to

$$t_{delay} = \sqrt{\frac{2 \cdot L \cdot C \cdot V_q}{V_{in} - V_{out}}} + t_{ps} \qquad (1)$$

will always be present, where V_q is the quantization voltage and t_{ps} is the combined power stage, sampling and computation delay. Due to the random nature of disturbances in the converter circuit, the actual delay is not constant and cannot be simply compensated.

The relationship found in (1) is illustrated in Fig. 2 where the immense hardware requirements for a proper implementation of the time-optimal control law become apparent.

A typical result of the delay is shown in Fig. 3, where a 4mV quantization step ADC is used. The error due to the valley point detection delay is compound by the t_{on}/t_{off} control action and subsequent PID takeover, denoted by the extra injected charge ΔQ_1 and ΔQ_2 respectively. Often, the resulting overshoots/undershoots cause chattering problem where the controller goes through multiple changes between its two modes of operations.

In the method presented here, rather than achieving recovery to steady state in the minimum possible time, the

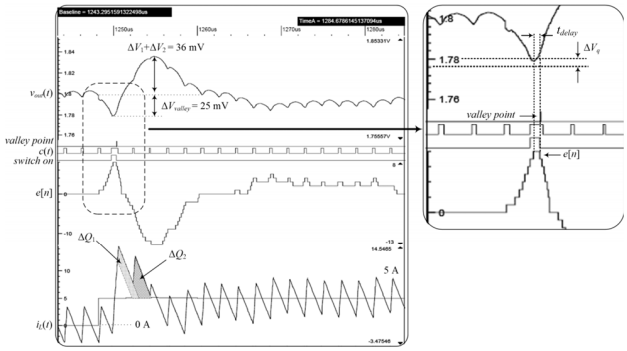

Figure 3. The voltage overshoot caused by incorrect valley point detection, power stage delay, and synchronization during 5-A load step applied to a buck converter with L of 0.47 µH and C of 400 µF.

aim is to achieve recovery with minimum possible voltage deviation and bump-less transition between two modes.

To obtain this, by minimizing the impact of inaccurate valley point detection, in the controller from Fig.1, the transition between the large and small signal compensator is always performed at the valley point in a synchronized manner.

For the light-to-heavy load transient the smooth transition between two compensators is achieved by matching the average value of $i_L(t)$ to the load current. As shown in Fig. 4, this is obtained by extending the initial on-time of the control signal $c(t)$ by t_{on} and by inserting the switch off time t_{off}. On/off times, t_{on} and t_{off}, are dynamically calculated as:

$$t_{on} = \frac{D \cdot T_{sw}}{2} \tag{2}$$

$$t_{off} = (1-D) \cdot T_{sw} \tag{3}$$

where D is the extracted steady duty ratio $d_{steady}[n]$ and T_{sw} is the switching period. During this short sequence, internal error registers of the small-signal compensators are cleared while the register holding the previous duty-ratio value $d[n-1]$ is updated with $d_{steady}[n]$ before it is restarted. In case of the heavy-to- light load transient, the same goal can be achieved by extending switch-off time by:

$$t_{off} = \frac{(1-D)}{2} \cdot T_{sw} \tag{4}$$

The use of the extracted steady state duty ratio removes the need to know the power stage parameters and also conveniently takes into account all the losses.

B. *Extension to a Two-Phase Buck Converter*

In some applications (e.g.. microprocessors), it may be necessary to use two interleaved converter phases to supply twice larger load current. For that case, the controller from Fig. 1 is modified to provide the same functionality as in the single-phase case. Control signal $c_1(t)$ for phase 1 is identically generated as in the single-phase case. On the other hand, for interleaved phase 2, upon exit from the valley point, control signal $c_2(t)$ is altered based on the sequence used for the opposite transient.

III. PRACTICAL ON-CHIP IMPLEMENTATION

The introduced large-small signal digital controller, as well as other state-of-the-art fast transient response digital solutions [11]-[16], require accurate and quick A/D conversions, in order to ensure appropriate and timely control actions. To provide such characteristics, in [11], an application specific 6-bit ADC, as a part of an optimal-time controller, is presented. The presented ADC provides fast conversion time and small quantization steps, but also has a large power consumption and silicon area of about 0.5 mm^2, which is comparable in size to a complete analog controller, making it unsuitable for numerous low-power applications. In addition, the large number of comparators provide no benefit during the valley and peak point detection periods, when only one comparator is toggled. To solve this problem and take advantage of the importance of the valley point detection, a new Track-and-Hold ADC architecture is developed and presented.

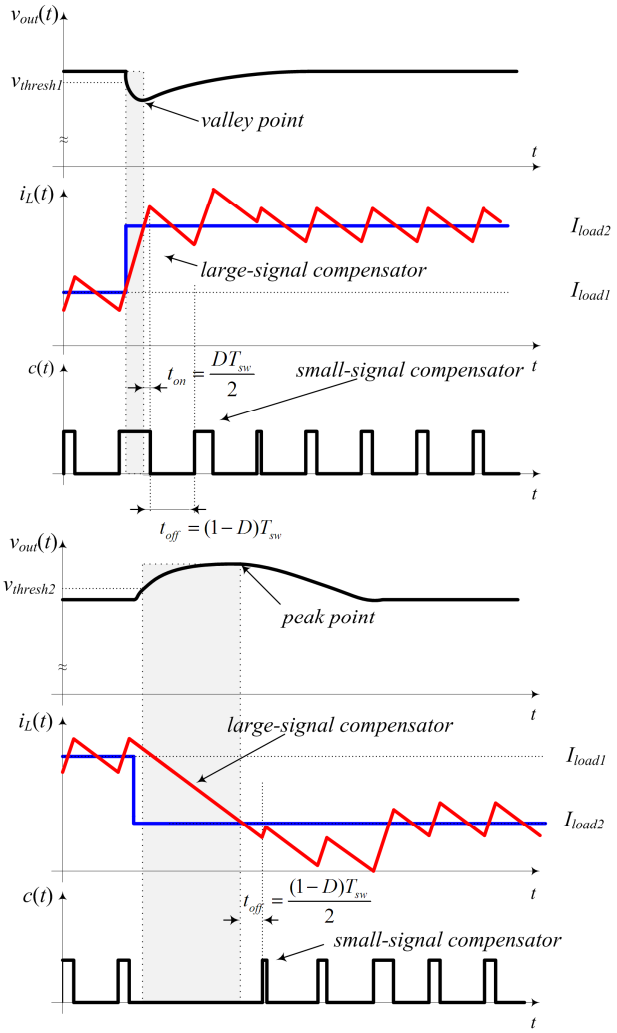

Figure 4. Principle of operation of the "large-small" signal compensator during light-to-heavy (top) and heavy-to-light (bottom)

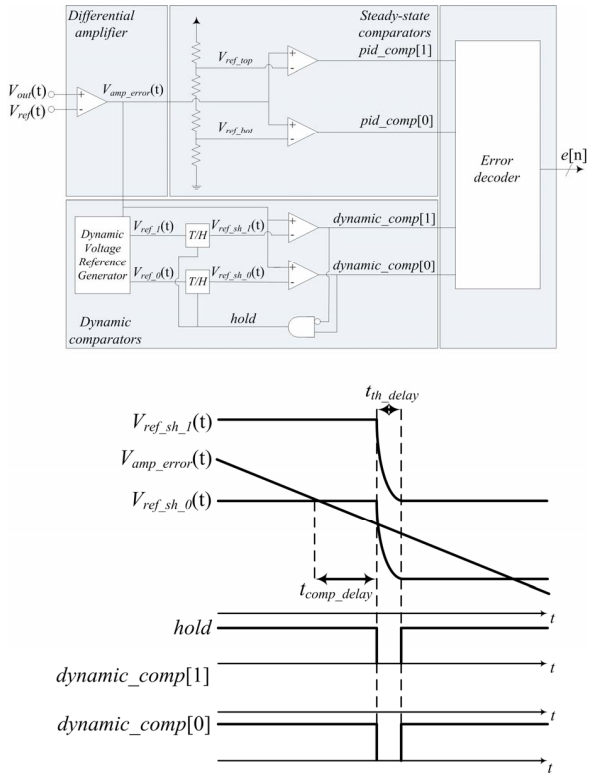

Figure 5. Block diagram (top) and a single track-and-hold transition (bottom) of the Track-and-Hold ADC.

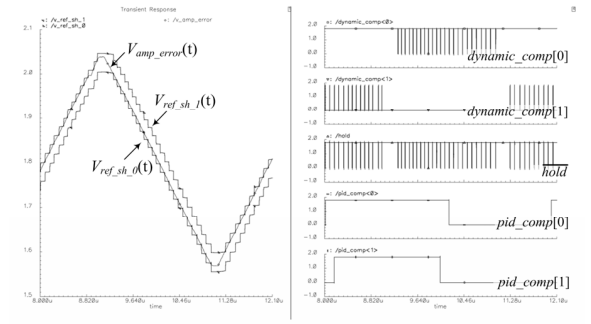

Figure 6. ADC simulation results: key analog signals (left) and digital logic outputs (right).

Conventional ADC architectures trade-off speed, accuracy, silicon area and power in order to satisfy a wide range of applications. These tradeoffs are best illustrated by the successive approximation and Flash ADCs. The successive approximation ADC (SAR) combines a single comparator, DAC and successive approximation register to generate iteratively converging input voltage approximations [23]. Speed and accuracy are sacrificed in exchange for smaller silicon area and lower power consumption. On the other hand, the Flash ADC combines $2^n - 1$ comparators in parallel, ensuring an n-bit output with a fixed conversion time, at the expense of increased power loss and silicon area [20,23,24].

The proposed Track-and-Hold ADC delivers conversion times and accuracy comparable to those of the Flash ADC architecture at a fraction of power and silicon area, combing the best of the SAR and Flash architectures. The block diagram of the novel ADC and a single track and hold transition are shown in Fig. 5. The Cadence HSpice simulation results are also shown in Fig. 6.

The detection of the peak and valley are at the core of the novel Track-and-Hold ADC. As a result, the Track-and-Hold ADC operates by continuously tracking the amplified error signal, $V_{amp\_error}(t)$, using a small window around it. The window is composed of two signals, $V_{ref\_sh\_1}(t)$ and $V_{ref\_sh\_0}(t)$, which are sampled and held $V_{amp\_error}(t)$ signal values with $+kV_q$ and $-kV_q$ offsets (The k denotes the differential amplifier amplification). The reference signals are generated using the Dynamic Voltage Reference Generator and two Sample-and-Hold circuits.

When $V_{amp\_error}(t)$ is outside the window, detected using the dynamic comparator outputs and two simple gates, the reference signals are re-sampled asynchronously. During the reference sampling process, the digital error representation is updated to reflect the $\pm V_q$ change using the dynamic_comp signal edges. Due to the comparator and sample-and-hold delays, denoted by t_{comp_delay} and t_{th_delay}, the digital error representation will accumulate an offset. To mitigate this, two steady-state comparators are used to detect the offset in the decoded digital error and re-calibrate it whenever the error signal crosses the zero point.

Furthermore, to minimize requirements on the comparators, a pre-amplifying stage is introduced. The pre-amplifier utilizes a bandwidth reduced two-stage operational transconductance amplifier [23] in order to filter high-frequency noise and generate an amplified error signal. As a result the comparators effective quantization step is larger, the required conversion time slower and the power consumption requirement reduced.

The Cadence Hspice simulation results of the Track-and-Hold flash ADC with a pre-amplification of 5 are presented in Fig. 6. It can be observed that proper tracking (left) of the fast changing input signal is achieved and that its digital outputs are generated as desired. The area and current consumption of the proposed ADC is compared with an in-house built 7-bit Flash ADC in Table I. A eight-fold reduction is obtained in both area and current consumption. A photograph of the chip, implemented using a 0.18µm CMOS process, is shown in Fig. 7. All digital blocks including a programming and debugging unit utilize less than 4500 logic gates.

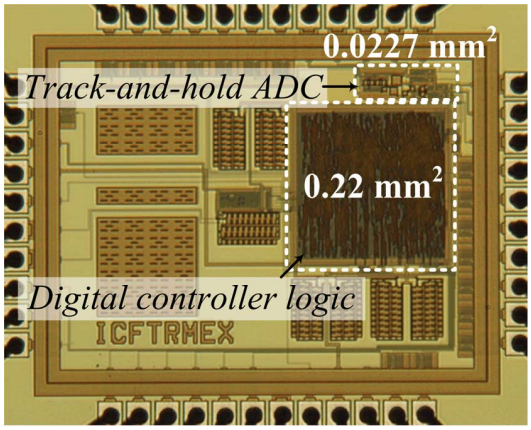

Figure 7. The large-small signal digital controller IC.

TABLE I. COMPARISON OF THE TRACK-AND-HOLD ADC AND CONVENTIONAL 7-BIT FLASH ADC

	Track-and-Hold ADC	***Flash ADC***
Conversion time (ns)	15	15
Area (mm^2)	0.0227	0.2
Current (mA)	0.24	2

IV. EXPERIMENTAL RESULTS

The operation of the large-small signal digital controller, from Fig. 1, is verified with a 60-W single-phase and 120-W dual-phase converter switching at 500 kHz. The parameters of a single-phase converter are given in Table II and are representative of modern point-of-load (POL) converters [18,19]. To compare the performance with a conventional PID, initially, the large-signal compensator is disabled and the operation of the small-signal compensator verified.

TABLE II. SINGLE-PHASE CONVERTER PARAMETERS

V_{in}	12 V
V_{out}	1.8 V
f_{sw}	500 kHz
L	0.47 µH
C	400 µF
ESR	0.5 mΩ
I_{load} (max)	30 A

Next, the large-signal compensator is enabled and the comparison with the previous result is shown in Fig. 8. The bandwidth of the small-signal compensator is $1/10^{th}$ of the switching frequency. When the large-signal compensator is enabled the voltage deviation is reduced by a factor of three as illustrated in Fig. 9. The voltage deviation can further be reduced with a faster transient detection system as illustrated by the red waveforms. In addition, the peak transient inductor current is also reduced which prevents undesirable inductor saturation. These improvements are the result of the instantaneous control action of the large-signal compensator which increases the inductor current to the new steady-state load current. Once the valley point is detected the transition between the large-signal and small-signal compensator is performed as explained in the principle of operation. In the case of incorrect valley point detection due to capacitor ESR or quantization errors, an overshoot is detected and the t_{off} time is appropriately increased ensuring a bumpless transition.

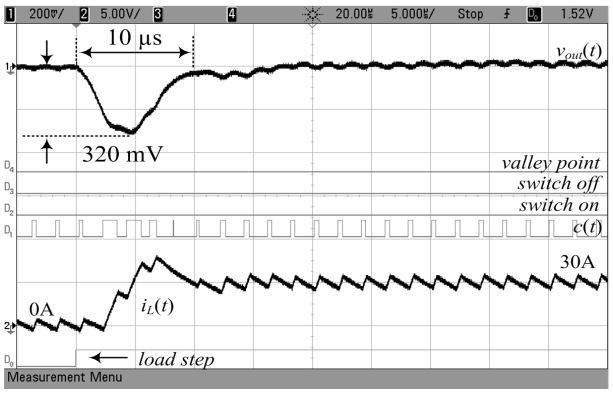

Figure 8. The response of the small-signal compensator for a load step from 0 A to 30 A.

The controller behavior in the presence of consecutive load transients, from 0 A to 12 A and 12 A to 30 A, is demonstrated in Fig. 10. The large-small signal controller effortlessly transitions between the large-signal and small-signal compensators under any load conditions, resulting in guaranteed minimum voltage deviation. In addition, the dual-phase controller output voltage and interleaved phase 2 inductor current waveforms are also shown in Fig. 11, verifying the successful minimum-deviation and bumpless transition. It should be noted that the presented experimental results show transient performance comparable to the time-

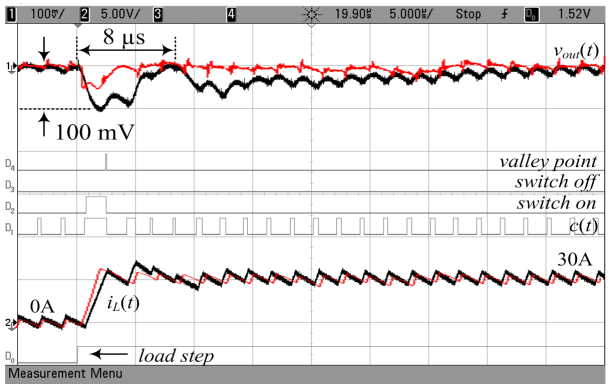

Figure 9. The response of the combined large-small signal compensator for a load step from 0 A to 30 A without (black) and with (red) fast transient detection.

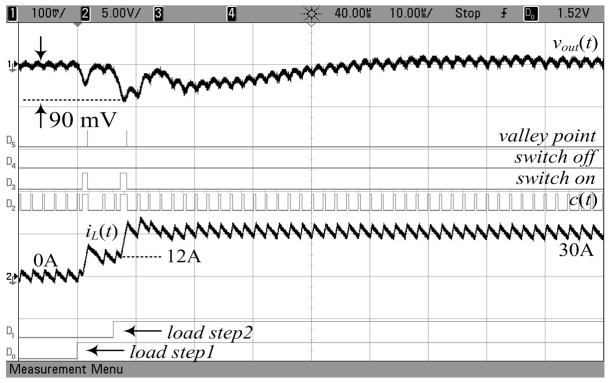

Figure 10. The response of the combined large-small signal controller under consecutive load transients.

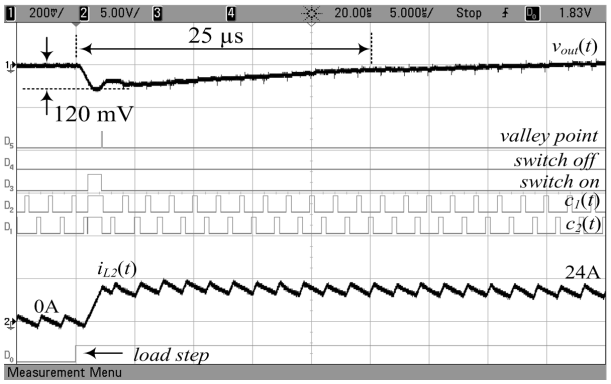

Figure 11. The response of the combined large-small signal controller for a dual-phase converter for a load step from 0A to 50A.

optimal controllers. The maximum deviation is not larger than that of the time-optimal systems and in a number of cases total recovery time is even shorter, due to the absence of overshoots/undershoots and previously mentioned chattering problems related to practical implementation problems.

V. CONCLUSIONS

The combined large-small signal controller IC that provides minimum output voltage deviation is presented. The controller implements a very simple control law and utilizes novel hardware efficient architecture of a Track-and-Hold ADC to detect and measure rapid load disturbances. The Track-and-Hold ADC has a conversion time of only 15 ns, about 8 times smaller area than the conventional ADCs, and a quantization step of only 4 mV. It's simple design allows for significant area and power reduction, enabling the use of optimal control architectures in low-power SMPS.

To overcome the bandwidth limitations of the averaged small-signal model, the controller IC implements two dedicated compensators: for the large-signal and small-signal operation. The solution for the bumpless transition at the valley point between two modes of operation taking into account the inductor current ripple is introduced. The controller was implemented in a CMOS 0.18 μm process occupying 0.26 mm^2. Due to the controllers simple architecture all digital logic blocks were implemented with less than 4500 gates. The controller operation is verified experimentally with modern POL converters under various load test conditions, including the consecutive load disturbance case. The controller was also verified with a dual-phase buck converter. All experimental results exhibit optimal voltage deviation for a given power stage and load step size, resulting in greater than three times reduction of transient output voltage deviation, equivalent to the same reduction of output capacitor value, compared to conventional PID compensators.

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