Multiphase Optimal Response Mixed-Signal Current-Programmed Mode Controller

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***Abstract*— This paper presents a simple and practical implementation of a proximity optimal-time (OT) response controller for multiphase interleaved dc-dc switch-mode power supplies (SMPS). This novel solution enables equal current sharing between phases not only in steady state, but also during load transients. It also achieves a bump-less transition between the transient and steady state, where the interleaved operation is resumed without any delay. To minimize calculation burden and hardware complexity, a single digital voltage loop and multiple analog current loops are combined to implement a capacitor-charge balance based optimal-time recovery algorithm. The interface between the loops is provided through a structure consisting of a sample-and-hold circuit (S&H) and a relatively slow successive approximation digital-to-analog converter (DAC) providing control signals for all the current loops. The effectiveness of the controller is demonstrated on a 2-phase, 5V-to-1.8V, 20W, interleaved buck converter operating at a 1MHz switching frequency. The experimental results verify equal current sharing under all operating conditions, bump-less transition between the modes, and demonstrate that upon a transient converter reaches new steady state in the virtually fastest possible time.**

I. INTRODUCTION

In low-power dc-dc SMPS used for supplying various portable and consumer electronic devices, the speed of the recovery time after a load transient is of a key importance. By reducing the time the SMPS needs to reach the new steady state after a transient, the size of the output filter of this cost-sensitive device can be significantly reduced. With the ultimate goal of achieving the fastest possible response for a given power stage, i.e. recovery through a single on-off action of the power switches, numerous methods have been developed. Those include trajectory path methods [1, 2], non-linear/ linear controllers [3]-[7], and methods based on the capacitor charge balance [8]-[12]. Most of these optimal-time response methods utilize recent advances in digital control of low-power SMPS to implement relatively sophisticated algorithms. While the digital optimal controllers have proven superior dynamic performance compared to analog solutions, their operation in multiphase interleaved systems has not been demonstrated in the listed previous art. Even though, in the multiphase interleaved systems [13]-[18] the speed of the transient response is one of the most important parameters.

Two problems can be correlated to the absence of the digital optimal control solutions for the multiphase systems: hardware complexity required for implementation and a lack of solution for equal current sharing during load transients. The optimal controllers usually rely on the instantaneous matching of the output load and inductor current, which, in the interleaved multiphase system, is challenging to achieve. Due to the time-shift between the phases, a large mismatch between instantaneous inductor current values usually exists.

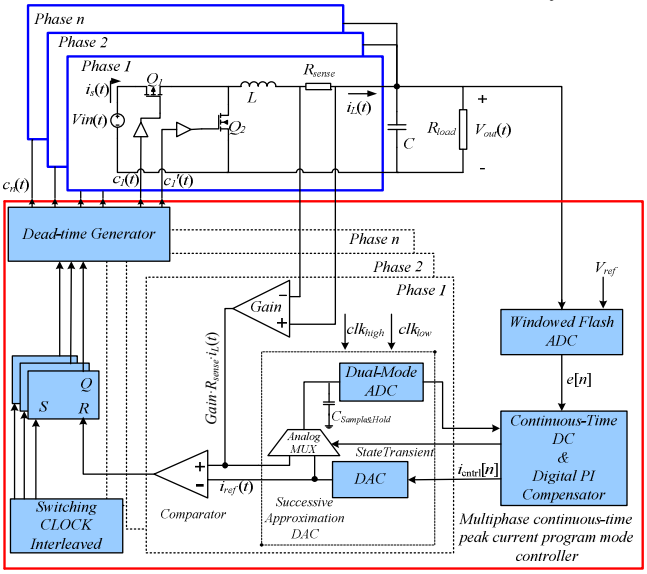

Fig. 1. Multiphase time-optimal controller regulating operation of an interleaved buck converter

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This causes difficulties in matching the sum of inductor currents to that of the load and, equally importantly, in providing equal current sharing during transients. Furthermore, mode transition problems, causing possible instability, which have been noticed in numerous single-phase implementations [1]-[12], have not been addressed for the multiphase system.

The main goal of this paper is to introduce a mixed-signal solution for the optimal control of multiphase interleaved dc-dc SMPS. The novel system, shown in Fig. 1, provides not only recovery from load transients in virtually fastest possible time but also proper dynamic current sharing during transients and bump-less transition between the modes. Furthermore, as it will be described in later sections, due to its mixed-signal realization, at light loads, the controller allows automatic transition to more efficient pulse frequency mode (PFM) of voltage regulation.

II. System Overview

Fig.1 shows the block diagram of the novel multiphase current program mode controller architecture. The voltage feedback loop is built as a digital block and the current loops are analog. Fig. 2 shows a more detailed diagram of the voltage loop that sets reference values for the current loops, either through a successive approximation DAC or through the sample and hold circuits, depending on the load conditions.

The controller has three distinctive modes of operation. In steady state, at medium and heavy loads, it works as a conventional mixed-signal peak current-programmed mode (CPM) system, similar to the one proposed in [19]. During transients, the continuous-time digital controller (CT-DC) similar to [10] is active, to achieve virtually fastest possible response. At light loads it behaves as a pulse frequency modulation (PFM) regulator.

A. Steady state

In steady state, the output voltage is sampled continuously by a windowed flash analog-to-digital converter (ADC), which produces an error signal $e[n]$. For small errors, i.e. $|e[n]| \leq 1$, the system is in steady state, operating as a CPM regulator. In an n-phase system, the analog references for the current loops are formed by n successive approximation DACs.

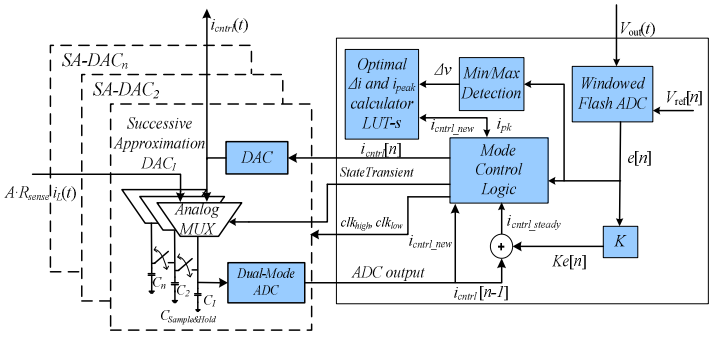

Fig. 2. Block diagram of the voltage loop

In each switching cycle, the new current reference is formed as:

$$i_{cntrl}[n] = K \cdot e[n] + i_{cntrl}[n-1], \quad (1)$$

where $e[n]$ is the error signal, K is an integrating coefficient, and $i_{cntrl}[n\text{-}1]$ the value of the control signal of one cycle before. The analog equivalent of $i_{cntrl}[n]$ is also captured by the sample and hold circuit (S&H) of Fig.2. In the following switching cycle the sample is used to form new "one cycle before" value after being converted to its digital equivalent, with the *Dual-Mode ADC* that, in this mode, takes samples at the switching rate. The use of sample and hold capacitor makes the implementation of the DAC relatively simple and, as it will be described later, significantly reduces the complexity of the time-optimal response algorithms compared to all-digital implementation [5]-[11]. More importantly, the S&Hs allow practical implementation of the time-optimal algorithm for multiphase systems.

After being converted to its analog domain, the current control reference is compared with the representation of the inductor current. The output of the analog comparator resets the SR latch to produce duty pulses and complete the current loop [20].

B. Load transient mode

The transient is sensed by the *mode control logic* block, which triggers the optimal control mode at the time instant when the absolute value of the output voltage error exceeds 1, i.e. $|e[n]| \geq 2$. At that moment the main switch is immediately turned on or off, depending on the type of the transient. Simultaneously, a direct connection between the current sensing circuit of Fig.1 and S&H is established, through analog multiplexer, and the dual-mode ADC is set to operate in asynchronous mode reassembling operation of a continuous time processor [21]-[24]. This is performed to capture the peak/valley point of the inductor current during transients and consequently transfer it into its digital equivalent. As described in the following section, the captured peak/valley value is used by the *Optimal Δi* calculator, which sets two current references, to achieve a bump-less time-optimal response.

C. Pulse Frequency Modulation

When the current drops below the peak inductor current ripple value, the controller automatically switches to PFM mode of regulation. In this mode, the clock generator from Fig.1 is suspended, the current reference $i_{cntrl}[n]$ is set to a fixed value $i_{PFM}[n]$ (smaller than the equivalent current ripple), and the SR latch is clocked by the windowed ADC.

Each switching cycle is initiated by the ADC. It begins when the error signal, $e[n]$, becomes larger than 1 and ends when the inductor current exceeds the analog equivalent of $i_{PFM}[n]$.

It should be noted that, unlike in voltage mode digital pulse frequency regulators [25], [26], this implementation virtually does not introduce any hardware overhead, minimizing the overall cost of the controller implementation.

III. Fast Transient Response in CPM Based on Capacitor Charge Balance Algorithm

In this section, the operation of a single-phase optimal response CPM that utilizes capacitor-charge balance algorithm is first explained. Then, it is shown how the concept can be extended to multiphase interleaved systems.

A. Single-phase operation

Compared to the voltage mode control [10], implementation of the continuous-time digital controller for CPM is significantly simpler. The reason is that only two current control reference values are necessary. Those are the peak/valley value during a transient and the new steady-state after the transient, where, as shown here, the first one does not need any calculations since it can be directly captured by the S&H of Fig.2.

The operation of the introduced system can be explained by looking at the diagrams of Fig.3. They show the key waveforms of a single-phase converter during a light-to-heavy load transient. During steady state, the fast recovery system monitors the output voltage continuously. As soon as the load transient is detected, the analog current reference i_{ref} (Fig.1) is set to its maximum allowable value, to prevent inductor saturation. Simultaneously, the block named *Optimal Δi* generator is activated. This block sets two reference values shown in Fig.3: i_{peak} - the maximum current and the new steady state value, labeled as i_{cntrl_new}. To simplify implementation, only i_{peak} is calculated while i_{cntrl_new}, which is equal to the current at voltage valley point [10], is captured with the S&H. This process is followed by the calculation of Δi, also shown in Fig. 3,

The calculated Δi is used to set the digital peak current reference as:

$$i_{peak}[n] = i_{cntrl\_new}[n] + \Delta i[n]. \tag{2}$$

During this calculation period, the speed of the DAC is increased such that the new reference value is be set before $i_L(t)$ actually reaches it.

The actual calculation of the current difference is performed using a simple capacitor charge balance based algorithm, starting from the equation stating that the lost of the capacitor charge due to voltage variation needs to be equal to the extra charge brought by the inductor, i.e.

$$Q = C\Delta v = \frac{1}{2}\Delta i(t_{on} + t_{off}) \tag{3}$$

For an ideal buck converter the expression for Δi becomes:

$$\Delta i = \sqrt{\frac{2C(1-D)V_{ref}\Delta v}{L}} \tag{4}$$

It should be noted that this system completely eliminates stability problems related to transition between optimal and steady state mode. Furthermore, even when the voltage recovery is not optimal, the current reaches its proper steady state at the end of the on-off the cycle. This is because the new steady state is not determined through calculations but by capturing the actual new current value of the inductor current at peak/valley point.

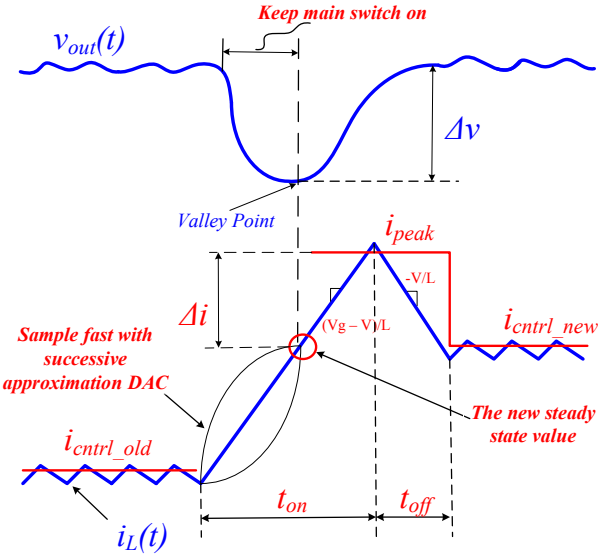

Fig. 3. The key wavforms of a single-phase power stage during a light-to-heavy load transient. Top: output voltage; Bottom: the inductor current.

B. Multiphase opertion

Compared to the voltage mode of regulation, parallel operation in CPM is simpler, since the inductor would behave as a voltage-controlled current source. Therefore, a multiphase converter behaves as a set of current sources charging a parallel combination of the output capacitor and the load resistor. However, the main obstacle in implementing an optimal-time controller for multiphase systems is maintaining balanced current sharing between the phases right after the transient. As it can be seen from Fig.4, showing waveforms of

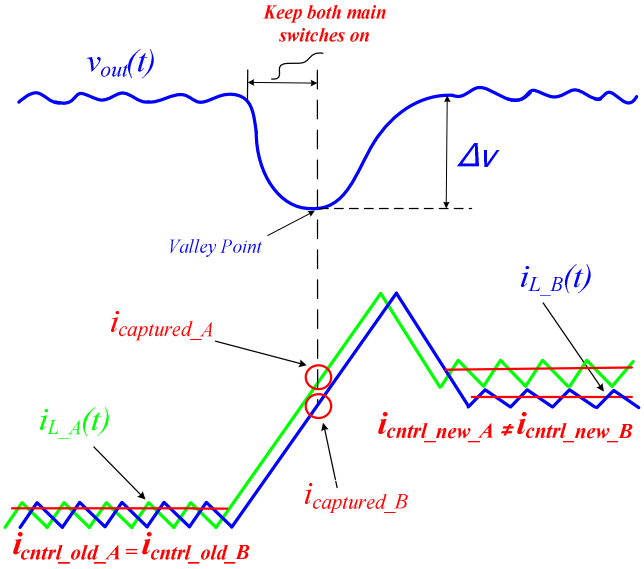

Fig. 4. The key wavforms of a two-phase interleaved buck converter during a light-to-heavy load transient. Top: output voltage of the converter; Bottom: inductor phase currents.

a two-phase interleaved system, unlike in the single-phase case, at the valley point the instantaneous inductor currents are usually not equal to their steady state values. This is caused by the time-shift of the phase currents.

To resolve this, the sample-and-hold circuits of Fig.1 are used, as well as the fact that, at the valley/peak point, the sum of phase currents is equal to the output current. When the valley/peak voltage point is detected, the inductor current of each phase is captured and saved in the respective sample and hold capacitor. Then, the outputs of all sample-and-hold capacitors are briefly short-connected such that the average value of all the sample circuits is obtained in all phases. As results, the new steady state references of all phases are the same and their sum is equal to the output current.

Averaging can be obtained in the digital domain as well, after the new control values have been digitized and divided by the number of phases. For 2^k (k =1, 2, 3..) phases, this operation is simple, since the division can be reduced to an arithmetical shift. However, doing digital averaging for other numbers is not trivial and does require a considerable time.

IV. Simulations and Experimental Verification

The operation of the new controller is verified both through experiments and simulations. The system of Fig.1 was verified experimentally on a two-phase 5V-to-1.8V, 20W buck converter operating at 1MHz. The digital part of the continuous-time controller feedback loop was implemented with an Altera DE-2 FPGA board and off-shelf ADCs. Simulations are performed to verify the system operation for a larger number of phases, i.e. for three and four phases.

A. Experimental Results

Figs. 5 to 9 demonstrate load transient operation. From Fig. 5 showing response for 8 A light-to-heavy load changes, it can be seen that the two phase system recovers to a new steady state through a single on-off action of each main switch and that equal current sharing is maintained before and after the transient. The waveforms also verify seamless, i.e. bump-less, transition between transient and steady state modes as well as operation without stability problems.

Figs. 6 and 7 show how $i_{ref}(t)$ (the analog comparator reference signal of Fig.1) changes during transient and inherent current protection feature of the system. As described in Section III, in Fig.6, it can be seen that the reference is set first to the peak value, then to the the new reference value. The waveforms of Fig.7 show the case when the peak value is limitted by the maximum allowable reference produced by the controller, to prevent inductor saturation.

Fig. 8 shows that the developed control system has the ability to recover in optimal time to successive load transients occurring during on/off sequence calculation. The first transient is a light-to-heavy load change of 2.2 A and it is followed by another 2 A step.

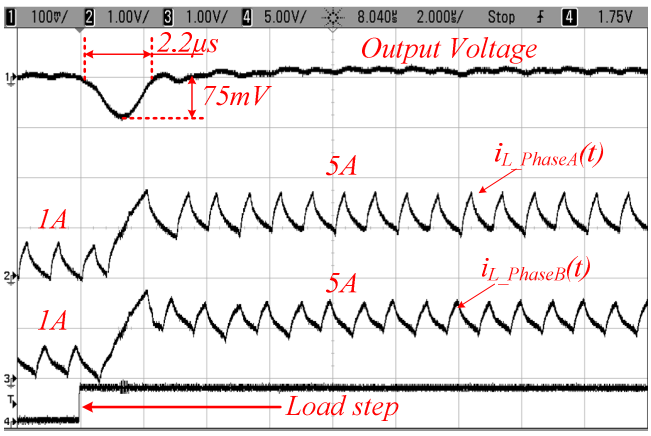

Fig.5. Transient response on a two-phase interleaved buck converter for an 8A light-to-heavy load step change. Ch.1: Output voltage (100 mV/div); Ch2 and 3: Signals from current sense circuit; Ch.4: Load step command. The time scale is 2µ/div.

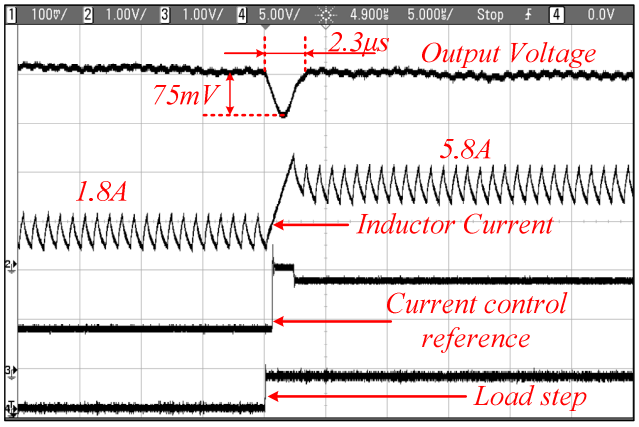

Fig.6. Key controller and power stage wavforms during a light-to-heavy load transient. Top: Output voltage (100 mV/div); Ch.2: Signal from a current sense circuit; Ch.3: Current control reference $i_{ref}(t)$; Ch.4: Load step command. The time scale is 5µs/div.

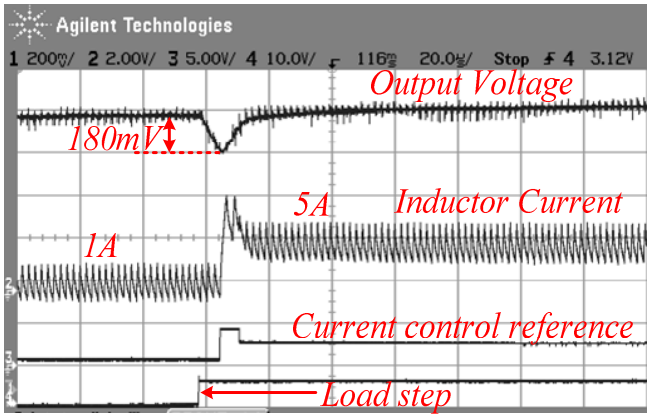

Fig. 7. Operation of current protection. The waveforms from top to bottom are: Output voltage (200mV/div); Amplified inductor current; Current control reference; Load step signal. The time scale is 20µs/div.

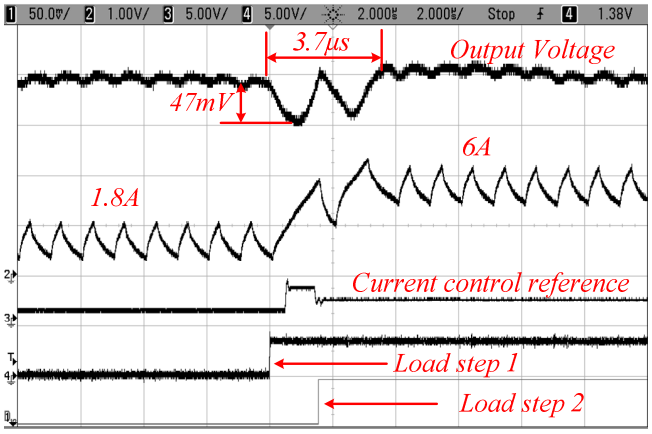

Fig. 8. Two consecutive transients using CT-DC. Top to bottom: Output voltage (50mV/div); Sensed inductor current; Current control reference; First load change command ; Second load change command. The time scale is 2µs/div.

Fig. 9 shows automatic transition between the continous current CPM mode pulse-frequency regulation. It can be seen that, upon a quick recovery from the initial change, controller "recognizes" very light load conditions and automatically switches to PFM regulation, as described in Section II.

B. Simulations

Based on the 2-phase experimental prototype a model of the converter is made and extra phases with the same current rating are added. The obtained model is then tested through simulations using the mixed-signal NCSIM simulator of the Cadence [27]. All the analog parts of the system were developed using Verilog AMS and the digital parts were in Verilog HDL. Simulation results are shown in Figs. 10 and 11. In these simulations "voltage probes" are set at the capacitors of sample and hold circuits and their numerical values are produced on the plots. It can be seen that both in the 3-phase cases and the 4-phase case equal current sharing is maintained before and after the transient and that bump-less transition is achieved in all cases.

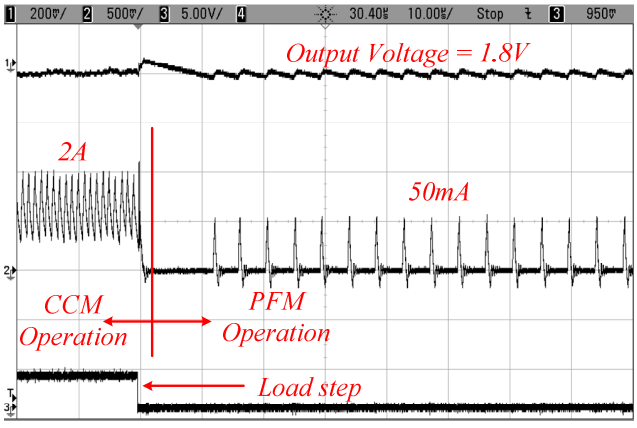

Fig.9. Transition between CPM and PFM modes for a heavy-to-light load transient. Ch.1: Output voltage (200mV/div); Ch.2: Signal from current sense circuit of a phase; Ch.3: Load step signal. The time scale is 10µs/div.

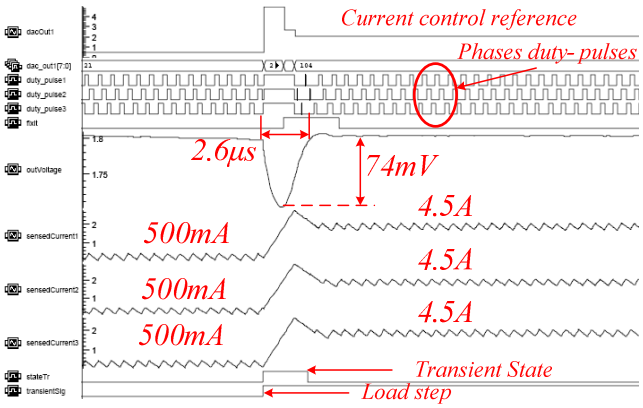

Fig. 10. Load transient rtesponse of a 3-phase interleaved system (simulation results).

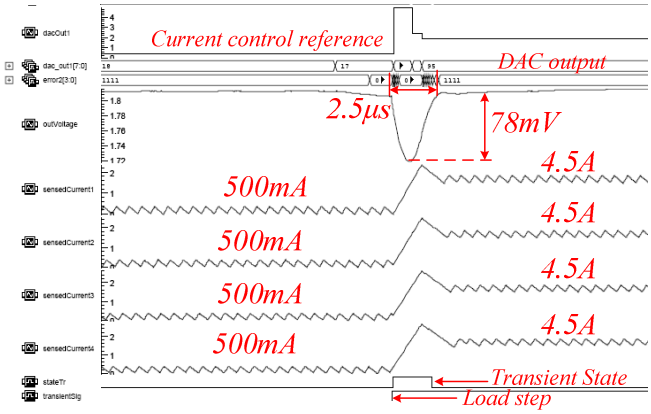

Fig. 11. Load transient rtesponse of a 3-phase interleaved system (simulation results).

V. CONCLUSION

An optimal-time control method and system for multiphase interleaved converters is introduced. The controller is implemented as a mixed-signal system, where the voltage loop is digital and current loops are implemented in analog manner. The optimal response is obtained utilizing simplified version of capacitor charge balance algorithm. To ensure proper dynamic current sharing during transients and bump-less transition between the modes of the controller, a simple solution based on short-connecting of the capacitors of sample-and-hold circuits is presented. The effectiveness of the controller is demonstrated on a two-phase experimental prototype, where both virtually the fastest possible transient response for a given power stage and equal current sharing in all operating conditions, including transients, are demonstrated.

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