Oversampled Digital Controller IC Based on Successive Load-Change Estimation for DC-DC Converters

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Abstract – **This paper presents an oversampled digital controller IC for low-power switch-mode power supplies (SMPS) that achieves fast response with a minimized addition of switching losses due to its control actions. To reduce the voltage deviation and improve converter response time, the controller samples the output voltage four times per switching cycle. A single voltage sample is processed by the conventional digital PID compensator to provide tight voltage regulation. Three additional samples are used to calculate the change in duty ratio value that results in the fastest possible response. If the load disturbance is significant, potentially causing large deviation, additional switching pulses are injected based on the estimated load change. To prevent operation at frequencies larger than the switching frequency, while still taking into account the results of oversampling, a novel oversampled digital pulse-width modulator (ODPWM) is introduced. The ODPWM adds or subtracts additional pulses such that the extra pulses are most effective in achieving fast recovery. The controller is implemented on-chip in CMOS 0.18μm technology. The complete controller occupies 0.53 mm² of silicon area and takes only 5500 logic gates for the implementation. Its functionality and effectiveness are demonstrated on a 12-V-to-1.8-V, 60-W buck converter switching at 500 KHz. Compared to a fast PID compensator, having crossover frequency equal to 1/10th of the switching rate, the new IC reduces the voltage deviation by two times.**

I. INTRODUCTION

Digital controllers [1]-[14] for dc-dc converters usually regulate the output voltage by taking the samples produced by an analog-to-digital converter (ADC). To improve the converter efficiency, minimize the power consumption of the controller circuit and reduce the hardware complexity, the ADC and accompanying digital pulse-width modulator usually update their values once per switching cycle. Previously, several such low-power, high-frequency digital controller IC implementations [1]-[5] were presented. However, compared to analog IC controllers [15], the dynamic response of those is usually inferior, negatively affecting the size of the power stage components, especially the output capacitor.

Recent linear [7] and non-linear digital controllers [8]-[14] have demonstrated that oversampling of the output voltage results in significant response improvements and reduction of power stage components. The linear controllers usually benefit from modest oversampling rates only, due to the converter

model limitations, which for linearized systems is valid for frequencies significantly smaller than the switching frequency. The dynamic response of linear controllers can potentially be improved by significantly increasing the switching frequency during transients [16,17]. However, such a solution would introduce significant switching losses.

On the other side, non-linear controllers do not have model-related limitations [8]-[14] but their implementation still usually require operation at relatively high oversampling rates and, consequently, fairly complex hardware. Often, the complexity and the silicon area occupied by such an ADC [14] exceed that of a complete analog controller [18], making digital implementations unpractical in low-power cost-sensitive applications. Furthermore, during load transients, these methods also often require the switching action of the power transistors to be performed at the rate significantly larger than that used in steady state causing increased switching losses. As a result, for frequent load changes, the converter efficiency is lower compared to conventional implementations [1]-[5].

The main goal of this paper is to introduce a non-linear oversampling controller, shown in Fig.1, which achieves
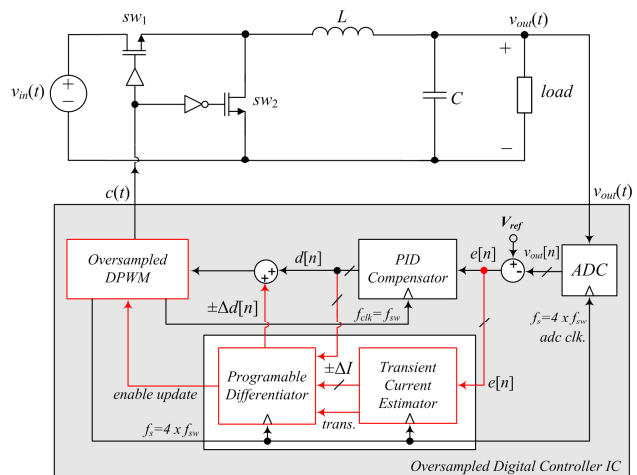

Fig. 1. The oversampled digital controller IC regulating the operation of the buck converter.

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significant output voltage transient improvements compared to conventional PID based controllers [1]-[5] using a very modest increase in oversampling rate and the minimum number of additional switching actions of the power transistors. During transients, the controller estimates the change in the load current [10,13] and accordingly modifies the control action such that the calculated changes of the duty ratio are averaged and "glued" to the DPWM. As a result, the switching frequency is not increased, but yet the effect of oversampling is fully utilized.

In the following section the controller operation based on successive load-change estimation is explained. In Section III we address the practical implementation of the key controller blocks, in particular oversampled DPWM with glued logic, and present the controller IC. In the final section, experimental results obtained with a buck converter prototype verifying the controller's operation are demonstrated.

II. PRINCIPLE OF OPERATION

Figures 1 and 2 can be used for explaining how the control pulses in this controller are generated. To minimize the delays existing in once-per-cycle sampled systems [1]-[5], the oversampling controller of Fig.1 takes four samples of the output voltage errors signal $e[n]$ during each switching cycle. Those four samples are processed by two functional blocks. The first block consists of *Programmable Differentiator* and a *Transient Current Estimator* (Fig.1). This block is active during transients only, to improve dynamic response. It takes all four error samples and, as shown in Fig.2.*a*), during output voltage deviations, produces $\Delta d[n]$ values, corresponding to increase of the duty ratio control variable $d[n]$. The value $\Delta d[n]$ is calculated with the programmable differentiator, which parameters are dynamically changed by the estimator. The estimator uses a modification of capacitor charge balance
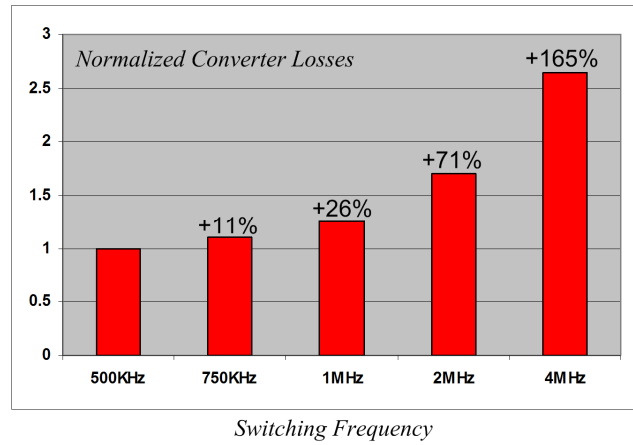

Switching Frequency

Fig. 3. Normalized converter losses versus the frequency of the switching actions for a typical industrial converter designed to operate at 500 kHz [19].

algorithm [8]-[12] to estimate proper differentiator gain, ideally resulting in proximity time-optimal response.

The second block is a PID compensator that takes every 4th sample and by producing duty ratio control signal $d[n]$ keeps system stable in steady-state conditions.

Ideally, during transients, this system could operate at the 4 times higher rate than the switching frequency to obtain a fast response. However, this implementation is not completely practical. As it can be seen from Fig.3, such an operation would incur additional switching losses and, for highly dynamic loads, significantly reduce the converter efficiency. Another practical problem is related to random quantization effects significantly affecting accuracy of $\Delta d[n]$ calculations.

To solve for both of the previously mentioned problems sequence of Fig.2.*a*) is modified as shown in Fig.2.*b*). Instead of producing $\Delta d[n]$ pulses at the 4 times the switching rate they
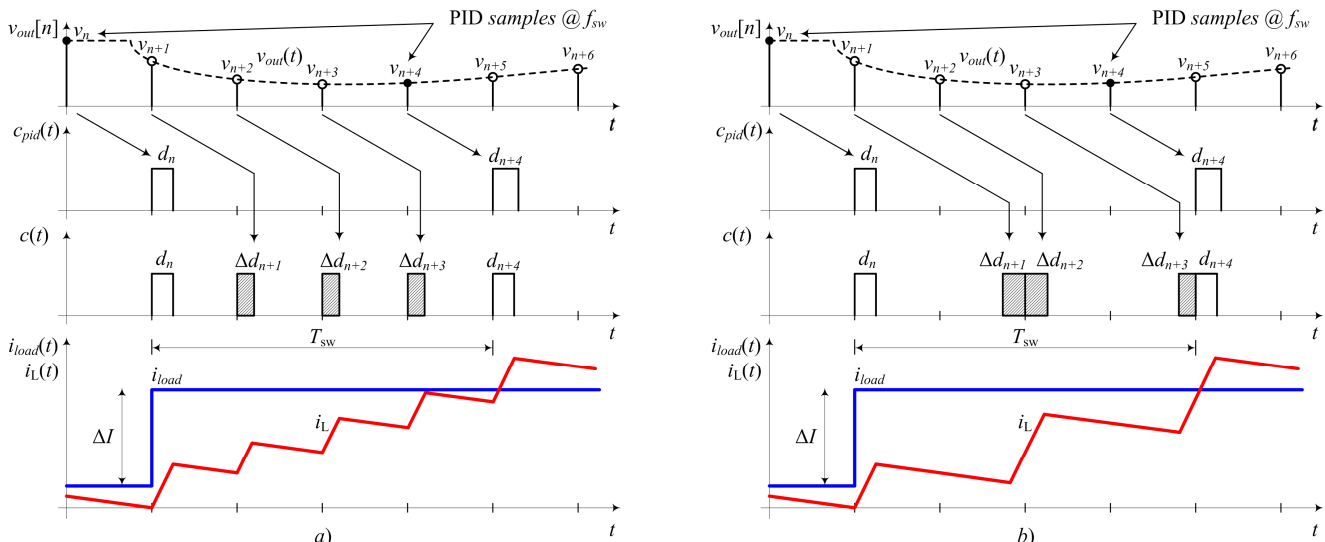

Fig. 2. The operation of the oversampled digital controller during transient: *a*) multiple control actions based on successive load-change estimation *b*) control actions are "glued" to limit switching activity during transients to $2f_{sw}$.

are created every other switching cycle, while still the information about the calculated values is maintained. To minimize the random error effect, the average value of several pulses is calculated and their average value produced every other sampling cycle. At the sampling instants where the $\Delta d[n]$ pulses coincide with those produced by the PID compensator, the increments are "glued" to the created pulse-width modulated signals. In this way, the switching rate of the system during transient is reduced to $2f_{sw}$, where f_{sw} is the nominal frequency of the converter, reserved for the steady state operation.

The created pulses are sent to an oversampled digital pulse-width modulator (ODPWM). The ODPWM provides updates of the calculated values at the twice switching frequency. The ODPWM actively monitors the switching pulses of Fig.2.a), and, accordingly, readjusts their relative position to reduce the effective switching frequency, as shown in Fig.2.b). Its operation is described in the following section.

III. PRACTICAL IMPLEMENTATION

A. Oversampled DPWM

To resolve the problem of frequent switching actions, shown in Fig. 2.a), and reduce power stage switching losses during transients, the ODPWM attaches the oversampled pulses, such that the effect of the oversampling calculations is maximized
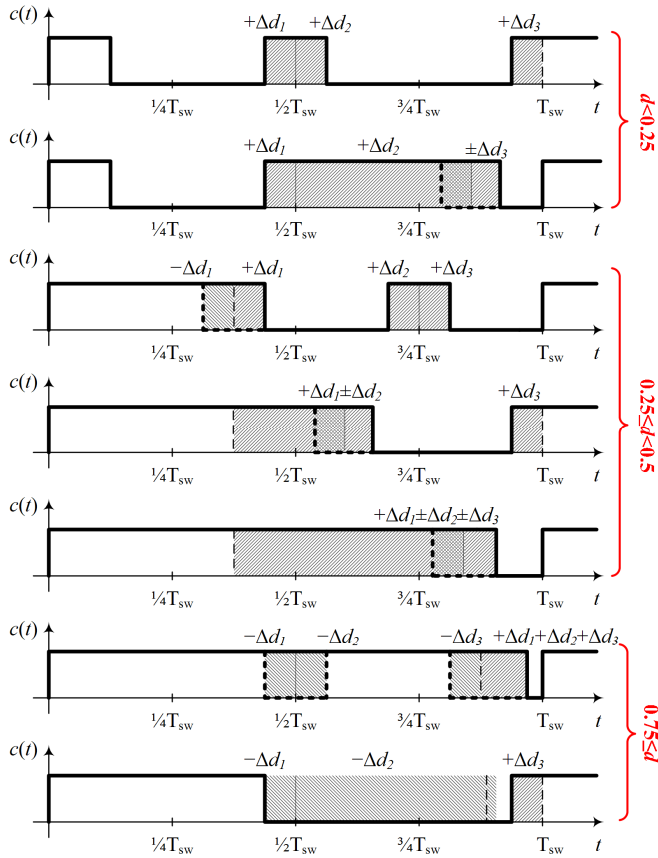

Fig. 4. Switching waveforms generated by the ODPWM for different duty ratio values.

without a significant increase of switching frequency.

The principle of operation is illustrated in Fig. 4 and can be explained through the following example. For PID-calculated duty ratio values less than 0.25, additional pulses Δd_1 and Δd_2 are merged at the middle of the switching period while Δd_3 is appended to the rising edge of the next generated PID pulse. If Δd_1 and Δd_2 are significantly large such that they extend beyond $\frac{3}{4}T_{sw}$, Δd_3 is merged with the falling edge of Δd_2 in order to reduce the delay of the control action and improve the response. Therefore the effective switching frequency is limited to $2f_{sw}$. A similar approach is used for duty ratios above 0.25. The only difference is that negative oversampled $-\Delta d$ pulses can be now generated by subtracting them from the original pulse. This is beneficial for minimizing the voltage deviation during heavy-to-light load steps.

From Fig. 4, it can be observed that the ODPWM, while reducing the effective switching frequency, also minimizes the control action delay. This reduction in control delay contributes significantly to the reduction in output voltage deviation.

B. Conditions for Transient Operation

Modern power converters [20,21] usually have a substantial output voltage ripple due to the output capacitor ESR and the small inductance necessary for fast transient response. To appropriately react to load disturbances, the required ADC quantization step is small, typically in the range of a few millivolts [11-12,14]. This is several orders of magnitude smaller than the steady-state output voltage ripple [7]. To make the controller insensitive to the sampled voltage ripple, a trivial solution would be to increase the ADC quantization step above the ripple magnitude. The penalty of the increased quantization step is a slower transient response. Alternatively, ripple-compensation techniques [7] may be utilized at the price of more complex controller hardware. To resolve this problem in a simple manner, threshold conditions for transient operation with a small ADC quantization step are introduced and derived here.

To prevent the triggering of the system by small high-frequency variations of the load current and output voltage ripple, minimum injected pulse-width thresholds of the oversampling controller are calculated based on the worst-case steady-state ripple. In order to make these thresholds robust, both the capacitor ESR and the inductor current ripple are taken into account during this analysis. The change in the output voltage in steady-state is given by:

$$\frac{dv_{out}}{dt} = R_{esr} \cdot \frac{di_L}{dt} + \frac{1}{C} \cdot i_c, \quad (1)$$

where R_{esr} is the capacitor ESR value. From (1) it is clear that the maximum/minimum output voltage rates of change, causing maximum Δe, occur when the capacitor current is maximum/minimum and is given by:

$$\Delta e_{max} = \frac{-\dfrac{dv_{out}}{dt} \cdot T_{sample}}{V_q} + Q_{error}, \quad (2)$$
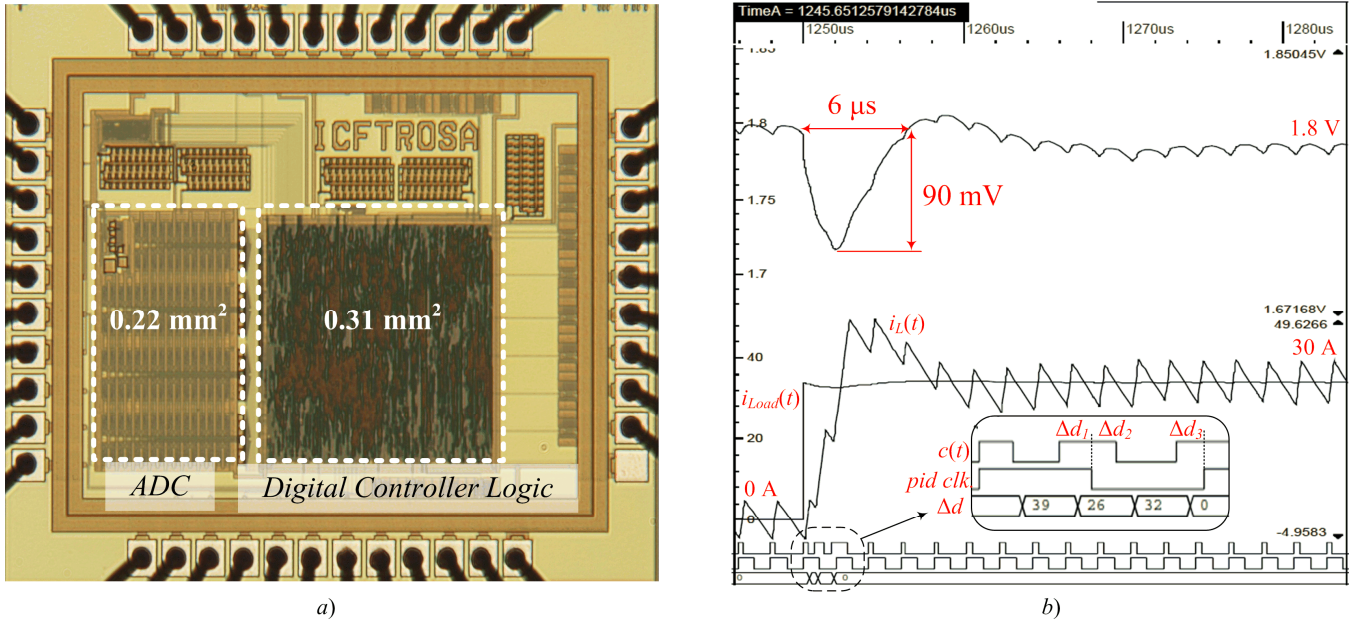
a)

b)

Fig. 5. The oversampled controller IC: *a)* chip die photo *b)* mixed-signal simulation for a load step of 30 A with a buck converter switching at 500 KHz and having inductor and capacitor values of *L*=325 nH and *C*=600 µF.

where Q_{error} is the maximum quantization error due to the ADC sampling (Q_{error} = 1). Therefore the minimum injected duty value thresholds then become:

$$\Delta d_{min} = \pm \Delta e_{max} \cdot c_{1/2}, \qquad (3)$$

where coefficients c_1 and c_2 are calculated based on the charge-balance principle [8]-[12] and the rising/falling inductor current slope respectively [22]. On the other hand, in order to reject the influence of large noise, the above analysis can be repeated to determine the maximum $\pm \Delta d_{max}$ threshold values. The value of $\pm \Delta d_{max}$ is obtained from the sum of the maximum load step and the inductor current ripple value, which is simply substituted into (1) in place of i_c. If the rate of change of the load step is known it can also be included in the analysis; however, it may be beneficial to assume it is zero such that the initial output voltage drop due to R_{esr} is also filtered out. The values of the $\pm \Delta d_{min}$ and $\pm \Delta d_{max}$ thresholds calculated by (3) are set within the *programmable differentiator*.

C. IC Implementation

The controller architecture from Fig. 1 is fabricated on-chip in CMOS 0.18µm technology and the chip die is shown in Fig. 5.*a*). A summary of the key IC parameters is provided in Table I. The controller occupies 0.53 mm² of active silicon area. The digital portion of the controller is implemented in Verilog HDL and after synthesis it consists of 5500 logic gates. The operation of the controller is verified with a mixed-signal simulation. For a 30-A light-to-heavy load step, the results are shown in Fig. 5.*b*) where a 90 mV output voltage deviation and 6 µs settling time are observed. As it can be seen in Fig. 5.*b*), to minimize switching activity and improve efficiency, the

additional pulses are effectively "glued" while they are produced only until the voltage deviation is suppressed.

TABLE I.   OVERSAMPLING CONTROLLER CHIP SUMMARY

Technology	TSMC 0.18µm CMOS
Supply voltage	1.8 V / 3.3 V
ODPWM resolution	8 bits
ODPWM nominal frequency	500 KHz
ADC resolution	4 mV
ADC sampling frequency	2 MHz
ADC conversion time	300 ns
Controller complexity	5500 gates
Controller area (digital part)	0.31 mm²
ADC area	0.22 mm²
Total active chip area	0.53 mm²

IV. EXPERIMENTAL SYSTEM AND RESULTS

An experimental system verifying the operation of the oversampled controller IC was built based on the diagram shown in Fig. 1. The power stage is a 60-W, 12-V-to-1.8-V buck converter switching at 500 KHz. The inductor value *L* is 325 nH and the output capacitor value *C* is 600 µF. The on-chip ADC has a 4 mV resolution and a 300 ns conversion time. The PID compensator coefficients are externally programmed onto the chip to obtain a bandwidth higher than 1/10th of the switching frequency. Initially, controller blocks responsible for the non-linear operation are disabled and controller response is verified.
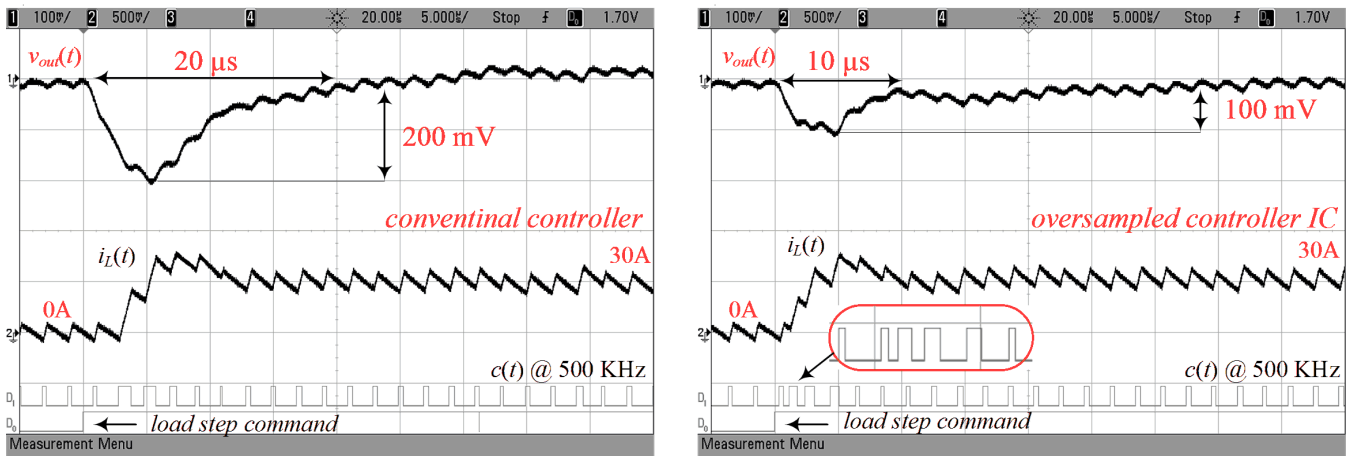
Fig.6. The controller response to a 30-A load step with *a*) Conventional controller (left) *b*) Oversampled controller IC (right) – Ch1: Output converter voltage (100mV/div); Ch2: actual inductor current $i_L(t)$; D1- switching control signal, D0- load step command. Time scale is 5μs/div.

Fig. 6.*a*) shows the obtained response with a load step of 30 A with the PID compensator only. Even though the PID compensator reacts aggressively, increasing the inductor current to a value near the load step in one control action, due to the one cycle delay the voltage deviation is large and equal to 200 mV. The settling time is around 20 μs.

In the next step, the non-linear parts of the controller are enabled and the obtained controller response with the identical load step is tested as shown in Fig. 6.*b*). In this case, as soon as the load step is detected, by taking three additional samples, Δ*d* pulse values are calculated by the programmable differentiator block. To minimize the number of switching actions and improve the converter efficiency the ODPWM attaches the pulses as described previously. As a result, only one additional switching sequence is added as shown in Fig. 6.*b*). Fig. 6.*b*) demonstrates also that the additional pulses are injected only until the initial voltage deviation is stopped, i.e. the inductor current has reached approximately the output load current. Therefore, during most of the settling period and in steady-state the converter switches at the nominal 500 KHz. The obtained voltage deviation is reduced by a factor of two (50%) compared to the PID compensator only and is 100 mV. The settling time is reduced to approximately 10 μs.

V. CONCLUSION

A practical oversampling digital controller IC for dc-dc converter is presented. The controller operates at a modest 4x oversampling rate. The controller utilizes parallel processing of error signal, where a PID compensator and a programmable differentiator are combined to provide stable operation and fast transient response. To minimize the switching losses transients and quantization effect while maintaining all advantages of the oversampling, "glue logic" and application specific oversampling digital pulse-width modulator are introduced.

Also, conditions for eliminating the unintentional triggering of the controller, due to capacitor voltage ripple are derived. The effectiveness of the IC is verified on an experimental

system, demonstrating fast transient response and stable operation in all operating conditions.

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