Self-Tuning Mixed-Signal Optimal Controller with Improved Load Transient Waveform Detection and Smooth Mode Transition for DC-DC Converters

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***Abstract*— A hardware efficient optimum-deviation voltage mode controller with a fast and noise-insensitive detection of the key voltage waveform points during load transients is introduced. To reduce the effects of noise and delays on the detection, a two extreme point detector with a voltage tracking window is introduced. In addition, an on-line algorithm for the compensation of load-dependent duty ratio variations effecting stability of optimal controllers is developed. The effectiveness of the system is verified with a 12V-to-1.6V/50 W, 500 kHz buck converter demonstrating about 30% smaller voltage deviation compared to the conventional optimal controller.**

***keywords*— high frequency switch-mode power-supply, voltage-mode control, optimal control, self-tuning**

I. INTRODUCTION

Recent proof-of-concept linear [1],[2] and non-linear controllers [3]-[7], [9], demonstrate significant improvements in dynamic response compared to conventional PID compensated systems potentially allowing a drastic reduction of the power stage filtering components. However, in cost-sensitive low-power systems ranging from a fraction of watt to several hundreds of watts, a wider adoption of the fast response methods has been delayed. This is mostly due to hardware complexity and difficulties in an accurate identification/measurement of the power stage waveforms during transients [3]-[7],[9]. These problems are particularly prominent in digital and mixed-signal optimal controllers [4]-[7],[9], theoretically providing the fastest possible dynamic response and/or the minimum output voltage deviation during transients.

A wider adoption of the optimal controllers largely depends on the development of hardware efficient solutions for the following problems: *i) fast and accurate detection of load transients,* in order to minimize delays and prevent unstable oscillatory control actions, due to quantization effects [4]-[8] and noise-related fault transient detection; *ii) accurate detection of the valley/peak point*, where the inductor current is equal to the load current, used to accurately determine the optimal on/off transistor switching sequence [4]-[7], [9]. In addition to the waveform detection related requirements, the optimal controller also needs to provide *iii) smooth transition between the dynamic and steady state modes of operation*, two modes usually present in the operation of such controllers.

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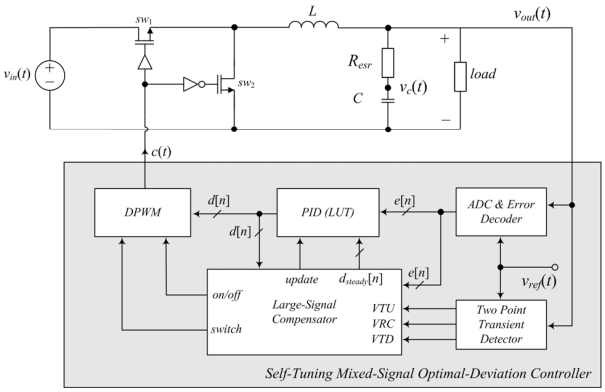

Fig. 1: Self-tuning mixed-signal optimal-deviation controller regulating operation of a single-phase buck converter.

The main goal of this paper is to introduce a hardware efficient optimal-deviation controller architecture solving the three outlined problems. The controller, shown in Fig.1, utilizes two novel blocks. The first block, *Two Point Transient Detector*, is a two extreme point detector mixed-signal circuit that minimizes delays and noise effects, drastically improving load transient and peak/valley point detection. The second block, *Large-Signal Compensator*, contains a self-tuning compensator providing smooth mode transition through on-line correction of load related duty ratio variations, which as shown in the following section, are a potential source of instability. Section II also explains the principle of operation of the entire controller. Practical implementation of the key blocks is shown in Section III. Section IV presents experimental results verifying improvements over the existing solutions.

II. PRINCIPLE OF OPERATION

The controller of Fig.1 operates in two control modes. During steady-state the operation of the power stage is governed by a conventional voltage mode digital PWM

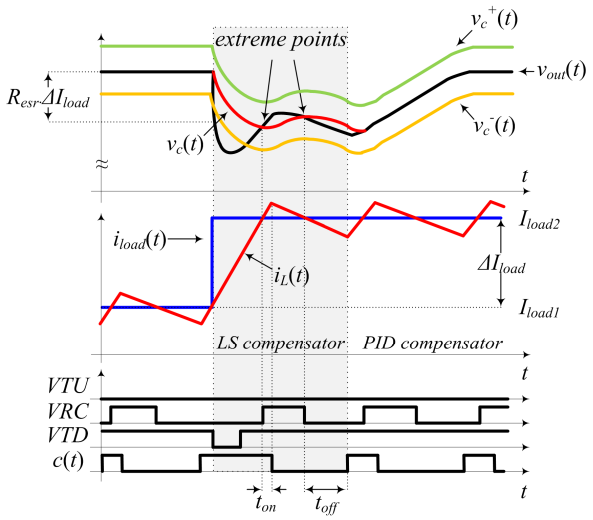

Fig. 2: Key waveforms of the introduced self-tuning optimal deviation controller during a light-to-heavy load transient.

regulator [10],[11] and, during transients, the *large signal compensator* employing minimum-deviation compensation [9] is activated. The transient mode is activated as soon as a significant load change occurs and is detected by the novel *two-point transient detector*. After the transient is suppressed the steady-state compensator is reactivated and a smooth mode transition is achieved using the proposed on-line duty-cycle correction method.

A. Acquisition of the main transient parameters

The *two-point transient detector* of Fig.1 is the key element in providing improved acquisition of the load transient parameters compared to the previous solutions [9]. It creates three output signals that depend on the instantaneous values of the output capacitor voltage $v_c(t)$ and its current. During sudden load changes it detects transients greater than a pre-defined threshold creating either a voltage transient up (VTU) or a transient down (VTD) signal, depending on the type of the transient. The threshold is introduced to prevent incorrect detection during steady-state, caused by noise, which can lead to stability problems. The threshold also prevents activation of the fast control mode for small disturbances, which can be effectively suppressed by the steady-state compensator. The third signal VRC indicates that the instantaneous inductor current is larger than the load current, i.e. that the output capacitor is being charged. The edges of VRC are indicative of two extreme points whose importance in improving accuracy of the detection will be explained shortly.

Fig.2 can be used to explain the operation of the detector and the subsequent actions of the fast mode controller. It shows the key analog and digital waveforms of the controller for a light-to-heavy load transient. In addition to the output voltage of the converter $v_{out}(t)$, the control signal $c(t)$, and the three output signals of the detector, the figure also depicts internal signals of the detector. Namely, it shows estimated voltage across the ideal output capacitor $v_c(t)$ (labeled in Fig.1), i.e. the output voltage without the component caused by the capacitor equivalent series resistance R_{esr}, as well as, signals $v_c^+(t)$ and $v_c^-(t)$ forming a tracking window around the output and the estimated value. As shown in the next section, the tracking window minimizes hardware requirements and the estimate is used to reduce the noise influence and improves the speed of the transient detection. In particular, during a sudden load transient of ΔI_{load}, the output voltage $v_{out}(t)$ instantaneously changes, due to the *Resr*, while the $v_c(t)$ initially remains unchanged, as shown in Fig.2. When this difference is greater than the window width, i.e. pre-defined threshold, a transient is detected. Such an implementation eliminates noise related triggering, since the circuit is active only when a significant amount of current is taken from the capacitor. For the same reason, it allows for the reduction of the threshold size increasing the speed of the detection compared to conventional detection [5], [7]-[9].

As soon as the transient is detected, the main switch is turned on or off, depending on the load transient type. The state of the switch is left unchanged until the inductor current $i_L(t)$ is equal to that of the load $i_{load}(t)$. At this instant, the extreme value of $v_c(t)$, is detected, as the point where the estimated and the output voltage are equal (capacitor current is zero).

A.1. Two-point valley/peak point detection

Ideally, after the peak/valley point is detected, the current state of the power switches is shortly extended such that an optimal response is obtained [4], [5],[7],[9]. Afterwards, the operation of the steady state controller resumed. However, in practice such a mode transition is challenging to achieve [7]-[9]. Due to the inherent delays of the detection and. control circuits, the time instant of the extreme point is not captured with a sufficient accuracy [9]. As a result, in modern converters having large inductor current slew rates, a significant mismatch between the instantaneous inductor and load currents usually occurs, causing stability issues related to multiple mode transitions. To minimize the effect of this delay, in this system a dual-extreme point detection method is introduced.

The advantages of the dual extreme point detector over the

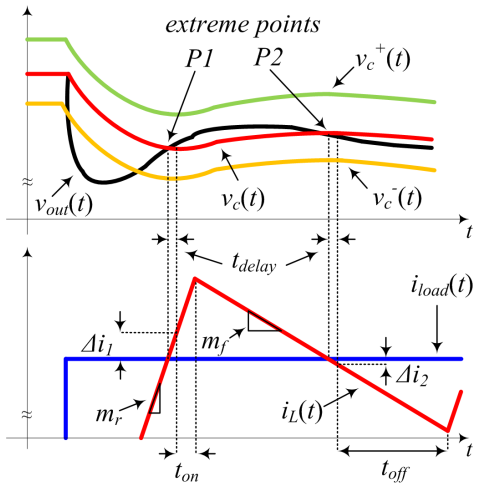

Fig. 3: Zoomed-in light-to-heavy transient, illustrating the current mismatch as a result of identical extreme point detection delay, t_{delay}.

single point and other detecting techniques [3]-[7] can be explained by looking at Fig.3, showing zoomed-in waveforms of Fig.2, in the region where two capacitor current zero crossings (extreme points) occur. In order to decrease the current mismatch caused by potentially inaccurate estimation *the extreme point where the inductor current slope is smaller is always used as the instant of the mode transition*.

In modern SMPS the difference in the slopes can be as high as 8 times [12]. For example, in a 12V to 1.6V converter with an inductance value of 320 nH [12], a 300 ns detection delay causes a 10 A mismatch for the rising slope and a 1.5 A mismatch for the falling one. This example is illustrated in Fig. 3, by Δi_1 and Δi_2. Further analysis on the influence of the detection delay in high current slew rate converters is undertaken in the next section.

B. Mode Transition and on-line D correction

In the case of a light-to-heavy load transient, after the first extreme point is detected, the on time of the main switch SW_1 (Fig.1) is extended by

$$t_{on} = \frac{D \cdot T_{sw}}{2}, \tag{1}$$

to obtain an optimum-deviation response [9], where T_{sw} is the switching period and D is the steady-state duty-cycle. The subsequent transition to the steady state mode depends on the slopes of the inductor current: *i)* In the case of accurate valley point detection, i.e. a small inductor current rising slope, from this point the steady-state mode is resumed *ii)* For the case of Fig.3 (a large rising and a small falling slope), the detection is performed in two points. After the first extreme point P_1 is detected and the on-time extended by t_{on}, the main switch is turned off. Subsequently, the second extreme point P_2, where the inductor and load currents are equal again, is detected with a much higher accuracy, and the off time of the switch is extended by

$$t_{off} = \frac{(1-D) \cdot T_{sw}}{2}. \tag{2}$$

This sequence is followed by the reactivation of the PID regulator, i.e. steady-state mode.

In an ideal lossless converter, the previously described switching sequenced provides bumpless mode transitions. However, in a realistic converter, the smooth transition cannot be guaranteed. This is due to the presence of losses affecting steady-state duty ratio value. This load dependent variation often causes problems in the mode transitions [7], due to inaccurate calculations of (1) and (2) for the new steady state, or any other duty-ratio dependent optimal switching sequence [4]-[7]. This can be illustrated by looking at Fig. 4, showing a simplified dc model of a buck converter [13] and a related equation describing the relation between state duty ratio value and the load current, when the feedback loop is closed:

$$D = \frac{V_{out}}{V_{in}} \cdot \left(1 + \frac{R_{eq} \cdot I_{load}}{V_{out}} \right) \tag{3}$$

where R_{eq} models converter losses.

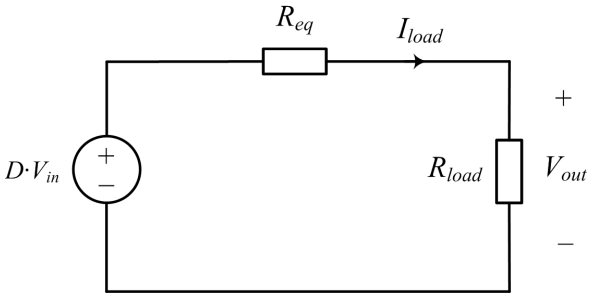

Fig. 4: Steady-state equivalent circuit of a buck converter.

Conventional solutions [3]-[7], [9] use a high bandwidth small-signal compensator, to quickly converge to the new steady-state duty ratio. However, as described in the following section, for the cases when the relative change of duty ratio is significant such a solution is ineffective, even when the converter has a fairly high efficiency.

To eliminate this problem an on-line steady-state duty-cycle correction algorithm, which estimates the load current step and records the given steady-state duty ratio value for all operating conditions, is created. The load current step is estimated using the length of the main switch on and off time intervals until the extreme points are detected, and the respective inductor current slopes during these periods.

The relationship between the rising, m_r, and falling edge, m_f, (shown in Fig. 3) of the inductor current is given by

$$\frac{m_r}{m_f} = \frac{2^{N_{DPWM}} - 1 - d_{steady}[n]}{d_{steady}[n]}, \tag{4}$$

where N_{DPWM} is the number of DPWM bits and d_{steady} is the zero load steady-state duty ratio value[13]. Using (4) the load current steps are estimated and categorized into three states: *Zero* (less than 1/8 of the maximum estimated load current step), *Low* (less than 3/4 of the maximum estimated load current step) and *High* (greater than 3/4 of the maximum estimate load current step). For a given state the change in the steady-state duty ratio value is obtained from a look-up table and used during the re-activation of the small-signal compensator.

The look-up table is updated continuously during steady-state, denoted as a period of similar *d*[n] values, and used during subsequent mode transitions in order to guarantee a smooth PID take-over.

III. PRACTICAL IMPLEMENTATION

A practical implementation of the circuit creating the waveforms of Fig.2 and Fig.3 is shown in Fig. 5. It takes advantage of the fact that the estimate $v_c(t)$ can be obtained by matching the $R_{esr}C$ time constant, τ_{esr}, of the output capacitor with $R_{esr}^* C^*$ [5]. By comparing $v_{rc}(t)$ to $v_{out}^*(t)$, the extreme points and zero current crossing of the output capacitor are detected, as shown in Fig. 2. By comparing the values of $v_c^{+*}(t)/v_c^{-*}(t)$ to $v_{out}^*(t)$ voltage drops, i.e. load step larger than $R_{esr} I_{loadmin}$ are detected. The size of the tracking window, i.e. the minimum detectable load step, $I_{loadmin}$, is adjusted by the offset between $v_c^*(t)$ and $v_c^{+*}(t)/v_c^{-*}(t)$.

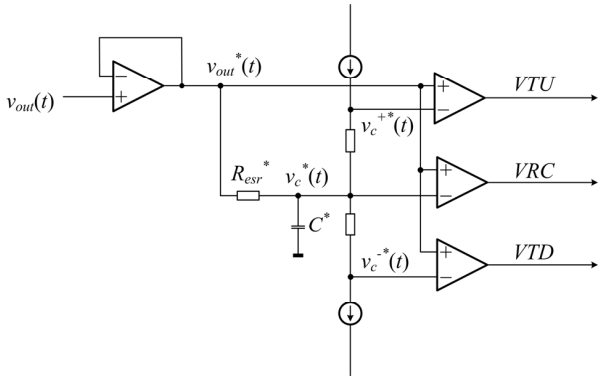

Fig.5: Extreme point and transient detection circuit.

This implementation can detect consecutive load steps and does not suffer from the ADC quantization effects [8], [9]. However, the sampling rate of the comparators introduces a small delay in the detection of the extreme points leading to a maximum inductor current error equal to (5).

$$I_{L_{error}} = -\frac{V_{out}}{L} \cdot T_{sample} \tag{5}$$

where T_{sample}, is the sampling period. As described in the previous section, the effect of the delay is largely compensated by the two-point detection method. In fact, the over-sampling rate requirements of the comparators, resulting in the same maximum inductor current error, are decreased by a factor equal to the ratio of rising and falling inductor current slopes. In modern SMPS this can be as large as 8 times [13].

It is also important to note that the novel detection method also minimizes the effect of mismatches in the voltage estimation circuit. Any mismatch between the actual τ_{esr} and the time constant of the estimation filter results in an extreme point detection error equal to the difference between the two time constants [5]. Due to varying temperature and humidity the actual difference can be up to 50% [14].

For the converter used for the experimental verification here, nominally having 1.5 mΩ equivalent series resistance of the output capacitor, this maximum tolerance results in a 300 ns point detection error. As described previously, with the newly proposed detection algorithm, this error translates to a 1.5 A current mismatch. Compared to a 10 A mismatch, for the case when the conventional sampling is used, the new method provides significant improvement in the accuracy of the peak/valley point detection, and consequently, improves the transient response of the controller, as shown in the following section.

IV. EXPERIMENTAL RESULTS

The operation of the controller is verified with an off-shelf 60-W single-phase 12 V to 1.6 V buck converter switching at 500 kHz and having an efficiency near 90% at the full load [12]. The converter uses a 320 nH inductor and a 400 µF capacitor.

The performance of the optimal controller, with (labeled as fast detection) and without the novel fast transient detection and on-line D correction blocks (labeled as slow detection/in-accurate D_{steady}), in response to a 32 A light-to-heavy transient is shown in Fig. 6. With the fast detection circuit the output voltage deviation decreases from 100 mV to 70 mV. Also, without the on-line duty-cycle calibration a second 100 mV voltage dip occurs. It can be seen that for the proposed controller employing the novel *Two Point Transient Detection* block the output voltage deviation is about 30% smaller than for the conventional sampling case.

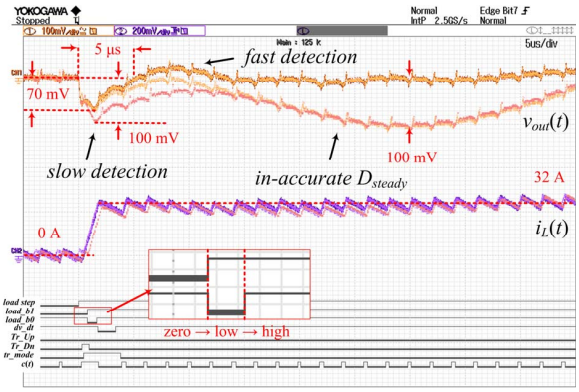

Fig. 6. 32A light-to-heavy transient, illustrating the effects of slow detection and incorrect small-signal duty value synchronization.

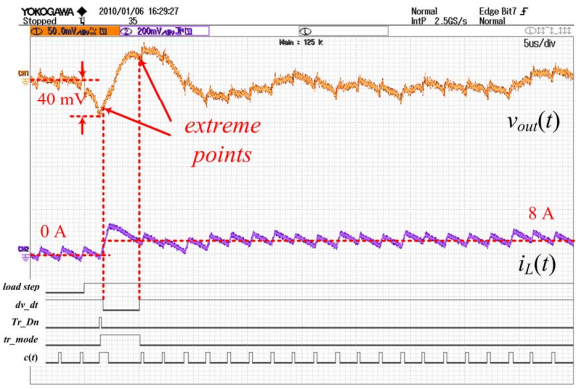

Fig. 7. 8A light-to-heavy transient with reduced sampling rate, illustrating the benefit of the second extreme point.

The advantage of this method in terms of the reduction of the sampling rate is shown in Fig. 7, for a small 8 A light-to-heavy transient, where the comparator output over-sampling rate is decreased from 32x to 8x. Compared to solutions employing only the first extreme point the inductor and load current matching accuracy remains un-affected while the sampling rate is decreased by a factor of 4.

V. CONCLUSIONS

A self-tuning mixed-signal optimal-deviation controller with improved load transient waveform detection and bumpless mode transition is presented. The system utilizes a simple to implement, ideal capacitor voltage estimation circuit with offset window to increase the speed of load transient detection. A significant improvement of the peak/valley point detection is achieved with the introduced two-point detection method, based on the sampling at the point where the inductor current slope is small. Furthermore, problems in mode

transitions between steady state and dynamic mode are eliminated by the on-line duty ratio correction algorithm presented here. Experimental verifications with an off shelf buck converter demonstrate that the system results in about 30% smaller undershoot compared to the same optimal controller using conventional detection.

REFERENCES

[1] S. Saggini, P. Mattavelli, M. Ghioni, and M. Redaelli, "Mixed-signal voltage-mode control for DC-DC converters with inherent analog derivative action," *IEEE Trans. Power Electron*.,vol. 23, pp. 1485–1493, May 2008.

[2] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, "High-bandwidth multisampled digitally controlled DCDC converters using ripple compensation," *IEEE Trans. Ind. Electron*.,vol. 55, pp. 1501–1508, Apr. 2008.

[3] A. Soto, P. Alou, and J.A. Cobos, "Nonlinear digital control breaks bandwidth limitations," in *Proc. IEEE Applied Power Electronics Conf*., 2006, pp. 724–730.

[4] G. Feng, E. Meyer, and Y.-F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters," *IEEE Trans. Power Electron*., vol. 22, pp. 1489–1498, July 2007.

[5] Zhenyu Zhao and A. Prodić, "Continuous-time digital controller for high-frequency DC-DC converters," *IEEE Trans. Power Electron*., vol. 23, pp. 564–573, Mar. 2008.

[6] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimović, "Proximate time-optimal digital control for synchronous buck DC-DC converters," *IEEE Trans. Power Electron*., vol. 23, pp. 2018–2026, July 2008.

[7] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Parameter-Independent Time-Optimal Digital Control for Point-of-Load Converters," in *IEEE Trans. Power Electron*., vol. 24, pp. 2235-2248, Oct. 2009.

[8] Y.-F. Liu, E. Meyer and X. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Trans. Power Electron*., vol. 24, pp. 2567–2577, Nov 2009.

[9] A. Radić, Z. Lukić, A. Prodić, and R. de Nie, "Minimum deviation digital controller IC for single and two phase DC-DC switch-mode power supplies," in *Proc. IEEE Applied Power Electronics Conf*., 2010, pp. 1–6.

[10] B. J. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. on Power Electron*., vol. 18, pp. 438 – 446, Jan. 2003.

[11] A. Prodić and D. Maksimović, "Design of a digital PID regulator based on look-up tables for control of high-frequency DC-DC converters," in *Proc. IEEE Workshop on Computers in Power Electronics*, 2002, pp. 18-22.

[12] "PIP212-12M data sheet," NXP Semiconductors, Eindhoven, Netherlands.

[13] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. New York, NY:Springer Sience+Business Media Inc., 2001.

[14] "TAIYO YUDEN high value multiplayer ceramic capacitors 2009 product catalog," TAIYO YUDEN, Tokyo, Japan.