Parameter Insensitive Passive Lossless Current Sharing Method Based on Negative Current

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***Abstract*— A parameter insensitive passive lossless current sharing method that minimizes conduction losses is introduced. Using only the information about the polarity of inductor current an optimal current sharing is achieved. The accurate knowledge of the converter component values is not required and the practical implementation is well-suited for on-chip integration. The effectiveness of the new system is demonstrated with a 12V-to-1.5V/70 W, 500 kHz dual-phase interleaved buck converter demonstrating about 1.7% improvement in efficiency compared to no current sharing.**

***Keywords*— multiphase, passive current sharing, parameter-insensitive, high frequency.**

I. INTRODUCTION

Modern switch-mode power supplies (SMPS) increasingly rely on the use of two or more interleaved phases in order to provide sufficient output current, decrease the output voltage ripple and achieve fast transient response [1]. As a result, of a key importance is not only to regulate the output voltage but also the phase current distribution. The main reasons are to maximize the converter efficiency and prevent potentially improper current sharing, leading to thermal runaway and premature failure. Current-mode converters [2]-[4] regulate both the output voltage and inductor currents. However, they usually require costly, and often lossy, current sensors [3],[4] or depend on parameter sensitive systems, whose accuracy varies with operating conditions and external conditions [5],[6]. To improve the accuracy of these passive solutions, self-tuning lossless current sensing methods were proposed [6]-[8]. However, an important drawback of these solutions is fairly complex implementation.

The main goal of this paper is to introduce a parameter insensitive and lossless current sharing method without the above mentioned problems. In addition to allowing a very simple hardware implementation and not being affected by parameter variations, the new controller minimizes the total converter conduction losses. A simplified block diagram of a multi-phase interleaved buck converter and a controller employing the proposed method is shown in Fig. 1. The *Current Sharing Logic* block compares the polarity of all inductor currents, determined by the *Current Polarity* blocks, and passively removes any unnecessary current offsets in order to maximize the efficiency, while a conventional digital voltage mode converter regulates the output voltage. The controller principle of operation is further explained in the following section. The practical implementation is described in Section III and the experimental results verifying the proper current sharing are presented in Section IV.

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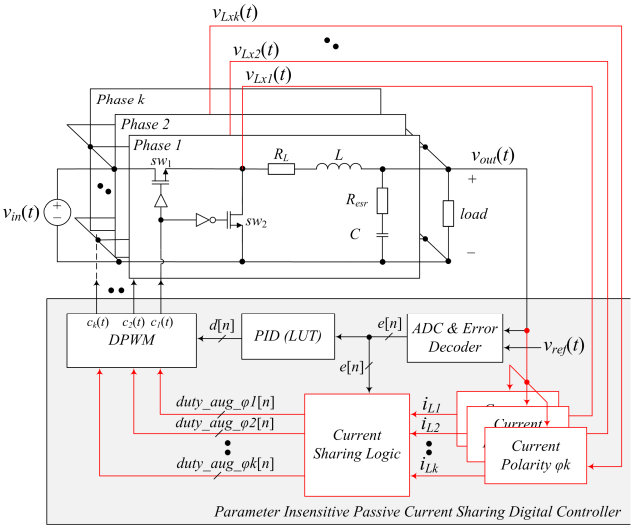

Figure 1: The parameter insensitive passive current sharing digital controller regulating operation of a multi-phase voltage mode interleaved buck converter.

II. PRINCIPLE OF OPERATION

The proposed current-sharing method relies on a property of interleaved buck converters: when the effective duty cycles of all phases are matched, the total current is shared such that the conduction losses are minimized [1]. Under such a condition, the current distribution is given by (1), where R_{eq} is the equivalent phase resistance of the phase n, $n \in \{1,2,\ldots,k\}$.

$$\boldsymbol{I_1 \cdot R_{eq1} = I_2 \cdot R_{eq2} = \ldots = I_k \cdot R_{eqk}} \qquad (1)$$

To achieve perfectly matched duty ratio control signals, several multi-phase digital pulse-width modulator (DPWM)

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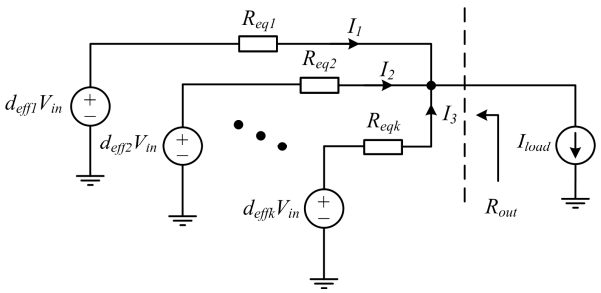

Figure 2: Equivalent circuit model of a k phase interleaved buck converter.

architectures have been proposed [1],[9]-[11] that ideally result in the minimized conduction losses. However, in practice, due to delays caused by circuit layouts and mismatches in the timing characteristics of the gate drivers and semiconductor switches, the effective duty cycles often significantly vary. As a consequence, suboptimal operation, from the efficiency point of view, occurs as well as circulating currents between the phases. The following subsection is devoted to the phenomenon.

A. Suboptimal Operating Conditions During Steady-State

Here, it is assumed that each phase current consists of two components: a component defined by (1) and a circulating current caused by a duty ratio mismatch. The following analysis quantifies the mismatch value causing a negative phase current, which is used as the key parameter in the proposed current sharing scheme.

The *k*-phase interleaved buck dc model, shown in Fig. 2, can be used to analyze the suboptimal operating conditions mentioned previously. Ideally, for a converter with infinitely fast switch transition times, the effective steady-state duty ratio value, shown in Fig. 2 as $\boldsymbol{d_{effn}}$, of the n^{th} phase is

$$\boldsymbol{d_{effn} = d}\ . \tag{2}$$

where d is a common duty value, issued by a perfectly matched multi-phase pulse-width modulator MPWM. Under such a condition, the current distribution is given by (1) and results in minimum conduction losses. However, imperfections of the MPWM, circuit layouts, and finite transition times change the waveform of the signal at the switching node (v_{Lxn} of Fig.1) and, consequently the effective duty ratio value as shown in Fig.3. The effective value is the

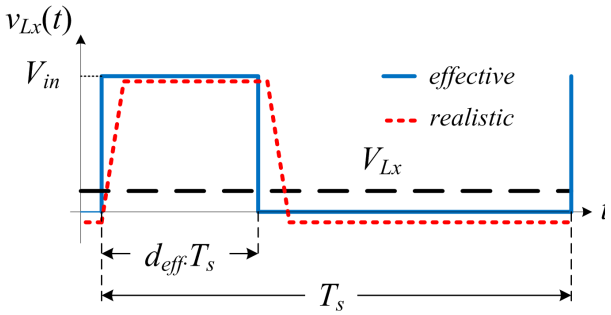

Figure 3. The realistic voltage waveform at the Lx node and an effective representation resulting in the same DC voltage.

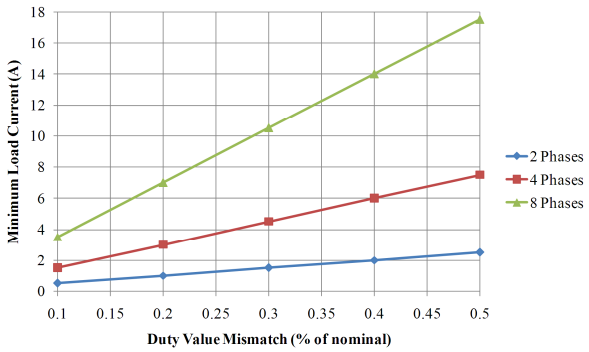

Figure 4. The minimum load current at which one phase conducts negative current as a function of the duty value mismatch.

duty ratio of a perfect square wave signal resulting in the same dc output voltage as the realistic waveform:

$$\boldsymbol{d_{effn} = d^* + \hat{d}_n}\ , \tag{3}$$

where d^* is the average duty ratio value of all phases and $\hat{\boldsymbol{d}}_n$ is the n^{th} phase offset. When the offsets of all phases are not the same, the current distribution diverges from (1), resulting in increased conduction losses. The cause can intuitively be thought of as additional circulating phase currents which do not affect the output voltage or load current. If the offset is large enough for a given load current one or more phase currents can conduct negative current. The minimum-load current at which a phase will conduct negative current, for a given phase offset, is shown in Fig. 4 for 2, 4 and 8 phases. It is assumed that the equivalent resistance is the same for all phases, and has a value equal to 3 mΩ. In addition, it is assumed that only one phase offset is different from all the other phase offsets (ie. $\hat{\boldsymbol{d}}_1 = \hat{\boldsymbol{d}}_2 = \ldots = \hat{\boldsymbol{d}}_{k-1} \neq \hat{\boldsymbol{d}}_k$), for simplicity.

We can see that even with a 0.1% duty value mismatch (equivalent to one 10bit DPWM LSB) for an 8 phase system, one phase will conduct negative current if the load current is less than 4A. In essence, any type of duty value offset can be detected using this single indicator. How this property is used to implement proper current sharing is described in the following subsection.

B. Calibration Procedure

The calibration process starts when one or more phases starts conducting negative current, detected by the *Current Polarity* blocks shown in Fig. 1, and the error signal $e[n]$ indicates the converter is in steady-state over several switching cycles. The *Current Sharing Logic* block augments the duty cycle value of the phase with the negative current until the polarity of the current is turned positive. This is repeated for all phases that at the beginning of the calibration were conducting a negative current. If the output voltage error deviates beyond an acceptable value (set by the application functional requirements) the calibration is temporarily suspended, until a steady-state is detected once again. This allows for incremental calibration even in the presence of dynamic and frequent load steps, as long as there are periods

during which a phase current is negative. Clearly, as the calibration procedure progresses, such conditions become associated with lighter and lighter load operation, until all the offsets are completely eliminated.

In addition, the above procedure requires only one bit of information per phase, enabling its use in master/slave controller configurations with minimal information sharing requirements. In fact, in the most simple implementation each slave would only need to compare its inductor current polarity with the masters and perform the calibration when they are opposite sign.

The frequency at which the duty-cycle can be augmented is dictated by the unit step input disturbance rejection characteristics of the closed-loop system and in part by the accuracy of the *Current Polarity* block, addressed in the following section. A good reference for robust controller design and analysis can be found in [14].

The accuracy of the calibration for different load steps is analyzed in the following subsection.

C. Current Sharing Accuracy for Varying Load Currents

Due to the fact that the duty-cycle value mismatch calibration is undertaken at lighter load current levels, the analysis of the current sharing accuracy at higher load current levels is necessary in order to quantify the potential current dependent mismatch. A dc model of a buck converter which includes the major non-ideal components, used to conduct the analysis, is derived using averaged switch modeling [13]. The voltage and current waveforms of the switch network are shown in Fig. 5, where

r_{dson1}	is the main switch on-resistance,
r_{dson2}	is the secondary switch on-resistance,
r_f	is the Schottky diode equivalent resistance,
V_{fo}	is the Schottky diode constant on-voltage forward drop,
t_{voff}	is the main switch voltage turn-off time,
t_{von}	is the main switch voltage turn-on time,
t_{dt}	is the dead-time, and
T_s	is the switching period.

The main switch current turn-on time is not included since it is negligible compared to the turn-off time for the operating

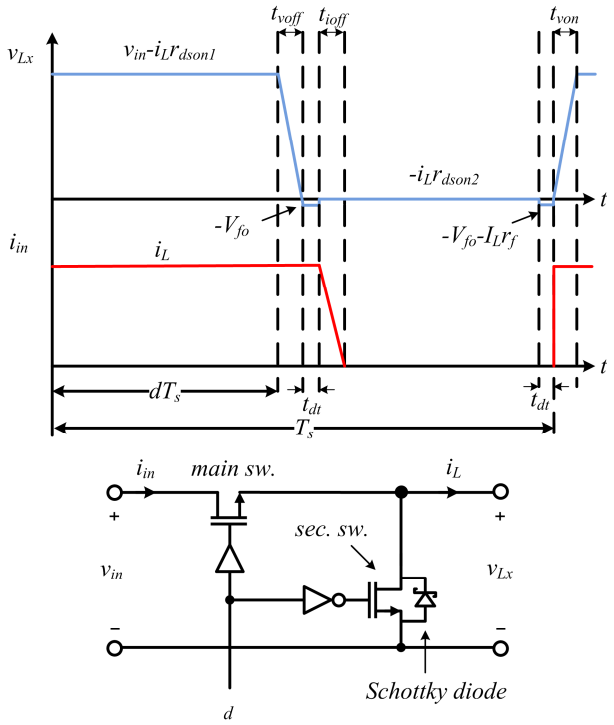

Figure 5. Averaged switch network voltage and current waveforms.

conditions considered in this paper [15]. In addition, it is assumed that the diode conduction time is minimal and as such the current through it is small during the main switch turn-off sequence, resulting in a constant voltage drop.

The resulting DC equivalent circuit for one phase is shown in Fig. 6, where t_v is the difference between t_{voff} and t_{von}. The absolute current mismatch, defined as the difference between inductor currents as a result of an duty value offset, are shown in Fig. 7 for a dual-phase interleaved buck converter for which the nominal values are:

TABLE I. NOMINAL CONVERETER PARAMETERS

V_{in}	12 V
V_{out}	1.5 V
T_s	2 µs
r_{dson1}	2 mΩ

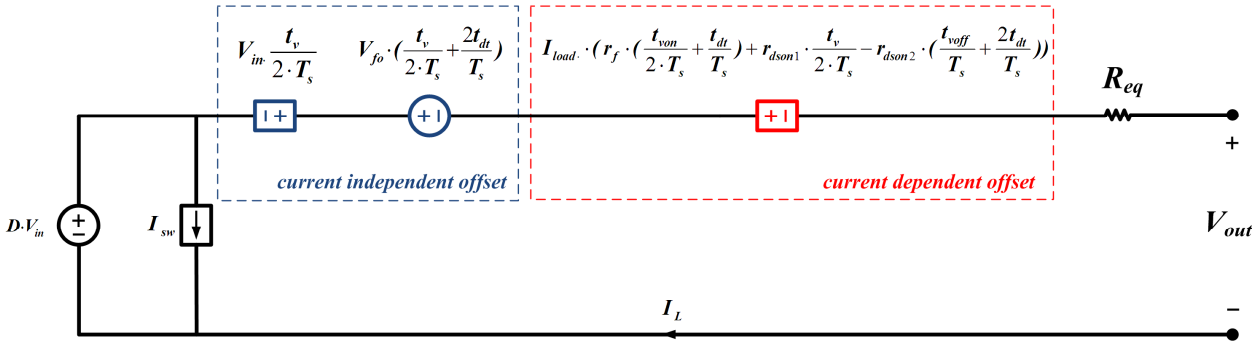

Figure 6. Equivalent circuit model of a buck converter including switching and conduction losses.

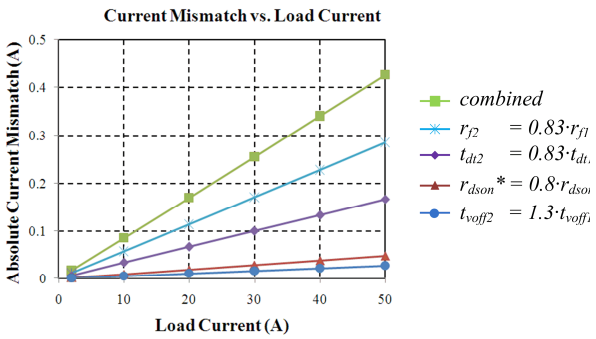

Figure 7. Absolute current mismatch vs. load current of a dual phase interleaved buck converter for varying parameter mismatch conditions.

r_{dson2}	0.6 mΩ
r_f	10 mΩ
V_{fo}	0.7 V
t_{voff}	20 ns
t_{von}	10 ns
t_{dt}	10 ns
I_{load} (max)	50 A

The parameters of one phase are fixed while a mismatch is introduced to the second. The switching times mismatch is +30%; the MOSFET on-resistance mismatch is -25%, for both switches; the dead-time mismatch is -20%; and the diode equivalent resistance mismatch is -20%. When all the converter parameter mismatches occur at the same time the resulting current mismatch is less than 0.45 A, or approximately 1% of the load current.

III. PRACTICAL IMPLEMENTATION

A practical implementation of the inductor current polarity circuit, the *Current Polarity* block in Fig. 1, is shown in detail in Fig. 8. It consists of an *RC* filter, differential amplifier and a comparator. It relies on the presence of the inductor series resistance (R_L) and the fact that the capacitor voltage is proportional to the inductor current, given by (6).

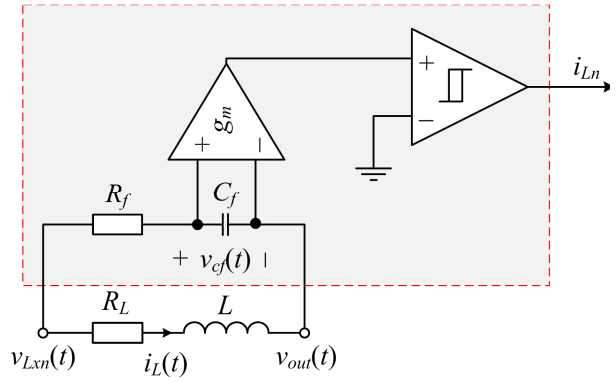

Figure 8. Current polarity sensing circuit.

$$v_{cf}(s) = R_L \cdot \frac{s\frac{L}{R_L}+1}{sR_fC_f+1} \cdot i_L(s) \tag{6}$$

From (6) it is clear that the DC polarity of the capacitor voltage is equal to the inductor current, ensuring accurate steady-state current sensing information. The dynamics of the sensing circuit affect the steady-state accuracy only when the difference between the L/R_L and R_fC_f time constants is large. In order to appreciate this we can examine the step-response of (6) for several time-constant mismatches, shown in Fig. 9 where L is 320 nH and R_L is 1 mΩ. It can be seen that for time-constant mismatch errors below 100% the normalized output will always be greater than 0.5. The importance of which can be realized through analysis of the multi-step response for varying normalized outputs, shown in Fig. 10 where the step period, T_{step}, is much shorter than the settling time of the current sensor. The relationship between the initial current value, I_{start}, and the final current value, I_{end}, is given by (7),

$$I_{end} = \frac{1-k}{k} \cdot I_{start} \tag{7}$$

where k is the initial normalized output found in Fig. 9. In the case where k is less than 0.5 it may be necessary to extend the step period until the normalized output is greater than 0.5 to ensure closed-loop stability.

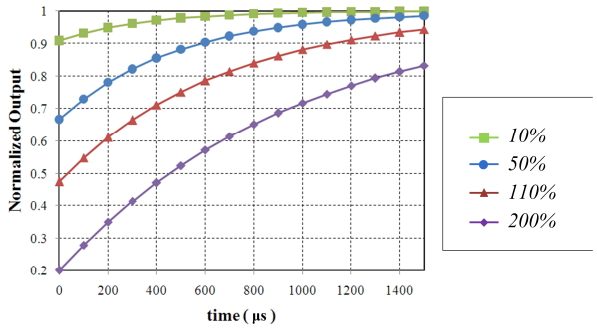

Figure 9. Step-response of the current sensing circuit with several L/R_L and R_fC_f mismatched time-constants (nominal L/R_L value is 320 µs).

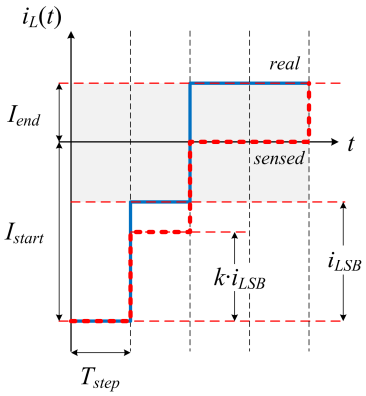

Figure 10. Multi-step response of the current sensing circuit.

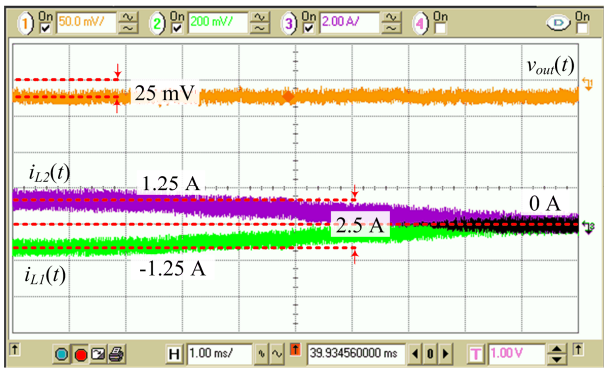

Figure 11. Duty cycle calibration as a result of a 2.5 A current difference with minimal output voltage deviation (Ch. 1 is using AC coupling).

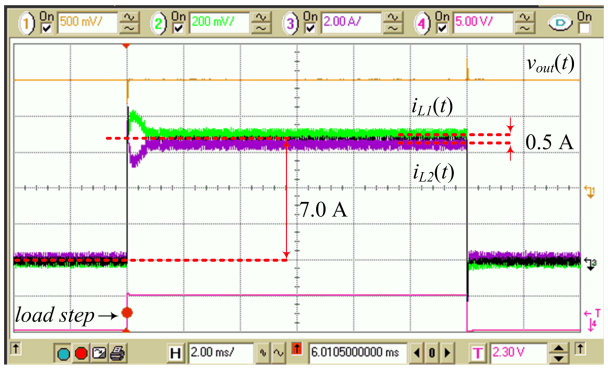

Figure 12. Current distribution after a 14 A load step, resulting in a 0.5 A current difference.

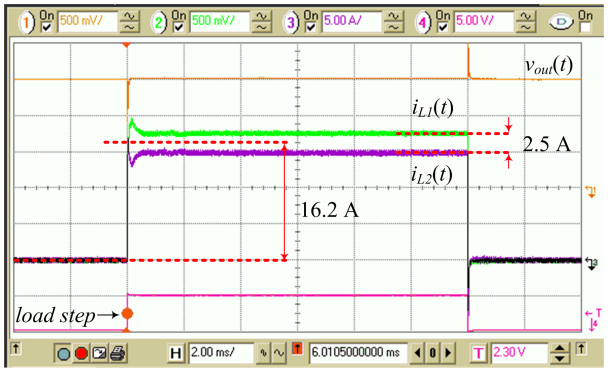

Figure 13. Current distribution after a 32 A load step, resulting in a 2.5 A current difference.

The main strength of this implementation lies in the fact that the accurate knowledge of the inductor parameters is not necessary and the accuracy is mainly affected by the input offset of the differential amplifier. In addition, the hardware complexity of this system is minimal and well suited for integrated applications, including low voltage.

It is important to note that the practical implementation presented here is not a unique solution. In fact, any sensing circuit or method which can accurately measure the inductor current polarity can be utilized.

IV. EXPERIMENTAL RESULTS

The operation of the controller is verified with an off-shelf 120-W dual phase 12 V to 1.5 V converter switching at 500 kHz, utilizing 320 nH phase inductors and a total capacitance of 400 uF [12]. The performance of the duty cycle calibration can be seen in Fig. 11 where the offset is removed in 8 ms without a significant output voltage disturbance.

The response of the converter to a 14A load step is shown in Fig. 12. The 0.5 A current difference at full load is equivalent to a 1.07 phase resistance ratio between the second and first phase. This agrees well with the measured equivalent phase resistance ratio of 1.05. The response of the converter to a 32 A load step is shown in Fig. 13, resulting in a 2.5 A current difference and 1.16 current ratio between the first and second phase at full load. This agrees well with the measured equivalent phase resistance ratio of 1.13. It should be noted that the difference in equivalent phase resistance ratios for the two load currents is due to the layout of the power board which has distributed loads with varying distances to each phase.

The efficiency vs. load current plot for the case where no current sharing, equal current sharing and passive current sharing (proposed) is used is shown in Fig. 14. It can be seen that, compared to no current sharing, this simple scheme improves the efficiency by up to 1.7% resulting in a larger than 10% reduction of the total losses and a proportional minimization of the cooling components.

The proposed method achieves minimal efficiency improvements compared to the equal current sharing method. However, it is important to note that the new method presented here is parameter insensitive and requires much simpler hardware implementation.

V. CONCLUSIONS

The parameter insensitive passive lossless current sharing method based on negative current detection is presented. The method eliminates undesired current offsets, resulting in minimized conduction losses. Compared to no current sharing a 1.7% efficiency improvement, or 10% reduction in

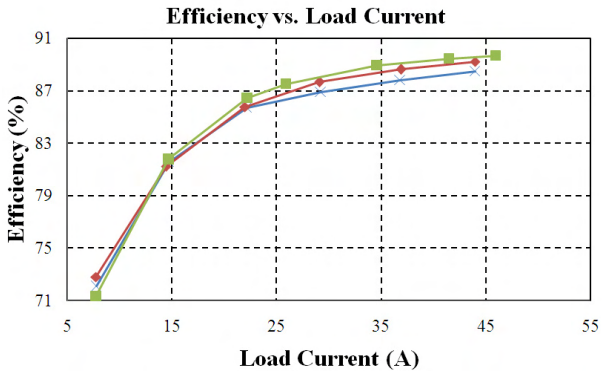

Figure 14. Efficiency vs. load current when no current sharing (x marker), equal current sharing (diamond marker) and passive current sharing (square marker) methods are used.

conduction losses, is observed. It utilizes a simple hardware implementation consisting of RC filter, differential amplifier and a single comparator per phase which can be implemented using a low-voltage process. Knowledge of the power stage parameters is not required and the method can be applied for n-phases without the introduction of output voltage perturbations.

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