ADAPTIVE SWITCHING FREQUENCY SCALING DIGITAL CONTROLLER FOR IMPROVING EFFICIENCY OF BATTERY POWERED DC-DC CONVERTERS

S. M. Ahsanuzzaman, Aleksandar Radić, Aleksandar Prodić
Laboratory for Power Management and Integrated SMPS, ECE Department, University of Toronto, CANADA
Email: {ahsansm,radicale,prodic}@ele.utoronto.ca

Abstract— **This paper introduces a practical system for improving efficiency of low power dc-dc converters regulated by digital voltage-mode PWM controllers. Depending on the input voltage, the controller adaptively changes the switching frequency, thus minimizing related losses while maintaining tight output voltage regulation and constraining electromagnetic interference (EMI) caused by the variable frequency operation. The presented architecture, whose key new element is all-digital adaptive clock and spread spectrum generator, can be implemented in the latest CMOS technologies and, as such, is well-suited for on-chip integration in portable battery-powered applications.**

The effectiveness of the system is verified with a 2.1 V/ 5 W buck prototype, where the input voltage ranges between 2.75 V and 5.5 V. The results show that, for an adaptive frequency regulation in the range between 780 kHz and 2 MHz, loss reduction of up to 18% is achieved.

I. INTRODUCTION

In modern portable battery powered electronic devices, the efficiency of the switch mode power supplies (SMPS) is one of the main concerns because it directly translates into battery life [1]. As shown in [1]-[4] batteries have a wide variation in voltage output depending on their charge level. The battery is usually connected to a fixed switching frequency SMPS providing a constant output voltage [2],[3],[5]. The output filter of such a supply is often oversized. The capacitor is usually sized based on the energy storage requirement during large load transients [6],[7], and the inductor is selected so that, for a given frequency, its steady-state ripple requirement is satisfied for the full range of input voltages, including the worst case. For a buck converter, the worst case corresponds to the largest input voltage. Such sizing provides tight output voltage regulation, but also results in a sub-optimal operation, from the efficiency point of view, for virtually all inputs except for the worst case. In other words, since the ripple for other input voltages is smaller than the allowable, the converter operates at a larger than the minimal possible frequency increasing switching losses. Conventional analog hysteretic controllers inherently providing constant current or voltage ripple [8] are not preferable solution. This is mostly due to the variable frequency of operation causing EMI problems and incompatibility for on-chip integration in the latest CMOS technologies, primarily dedicated to digital systems. While the EMI problems in numerous applications have been resolved, with spread spectrum mitigation techniques [9],[10], the on-chip integration with digital systems providing numerous benefits [11] remains a challenge. This is due to difficulties [12] in analog implementation of comparators, which need to be fast and accurate. On the other side, the digital hysteretic controller proposed in [13], operates at a fixed frequency not offering proposed efficiency improvement. Constant voltage ripple based hysteretic solutions [14] are challenging to implement, since they require sensing of very small output variations. On the other hand, constant current ripple designs [15] require current sensing introducing additional losses. Constant off-time controllers [16] also inherently provide constant ripple operation. However, this advantage comes only with buck-based topologies.

Frequency variations of the constant ripple controllers often raise EMI issues and, hence, mitigation techniques such as spread spectrum [9],[10] are applied. In low-power supplies most of these are implemented in an analog manner.

This paper introduces practical digital controller architecture of Fig.1 that minimizes losses by adaptively

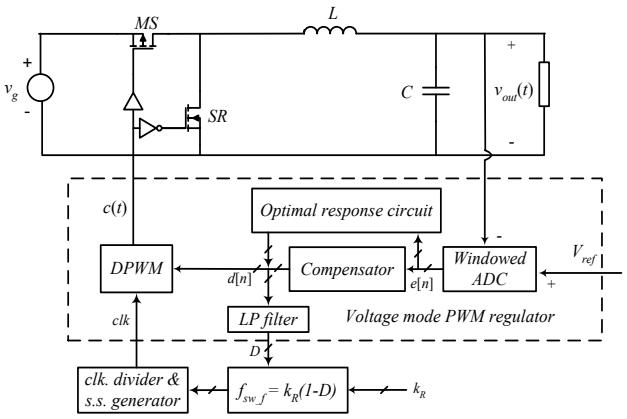

Fig.1: Adaptive switching frequency PWM controller regulating operation of a buck converter.

This work of Laboratory for Power Management and Integrated SMPS is supported by Exar Corporation.

changing the switching frequency, depending on the input voltage. To compensate for the variable frequency operation, not preferable in the targeted noise-sensitive applications, the controller employs adaptive EMI cancelation, using the key new element, named all-digital clock divider and spread spectrum generator.

II. Principle of Operation

The controller architecture of Fig.1 is designed around a digital PWM architecture [17]-[20], proven to be well suited for a full integration in the latest CMOS technologies [19],[20]. In this case, the clock frequency of the digital pulse-width modulator (DPWM) and, consequently, the switching frequency of the converter are changed using the *clock divider and spread spectrum generator* block from the figure. Input voltage dependent control signal $f_{sw\_f}[n]$ adaptively changes the fundamental frequency of the clock signal, as well as its spectrum. This means that the switching frequency f_{sw} is formed of two components, i.e. $f_{sw} = f_{sw\_f} + f_{ss}$. The fundamental component f_{sw_f} , is determined by the current ripple amplitude. The second component minimizing EMI, f_{ss} is created by the spread spectrum part of the generator.

To eliminate the input voltage measurement, the fundamental component resulting in a constant current ripple, for buck and boost converters, respectively, is selected as

$$f_{sw\_f} = \frac{V_{out}(1-D)}{2L \times \Delta i_L} = k_R \cdot D' \quad \text{[Buck]} \quad (1)$$

,

$$f_{sw\_f} = \frac{V_{out}}{2L \times \Delta i_L} D(1-D) = k_R \cdot D \cdot D' \quad \text{[Boost]} \quad (2)$$

,

where, Δi_L is the ripple amplitude, L is the output filter inductance, Vo is the output voltage, and D is the steady-state duty ratio value. In the system of Fig.1, this equation is implemented with a simple multiplier providing the control signal for the clock generator and having a control input $k_R[n]$ for regulating the ripple amplitude. The maximum allowable current ripple depends on the input and output voltages as well as on the width of the frequency side bands introduced by the spread-spectrum generator, increasing the current ripple and thus the steady-state voltage ripple. However, in modern SMPS the output capacitors are sized based on energy storage capability during transients. Consequently, from the charge ripple perspective, they are oversized and this portion of ripple is usually negligible [21].

To avoid potential slower dynamic response caused by operation at lower clock frequency, the controller employs an optimal response circuit [20], resulting in virtually minimum possible output voltage excursion during load transients.

III. Practical Implementation

The key new element of the presented architecture is the *clock and spread spectrum generator*. To generate spread spectrum, usually mixed-signal solutions based on analog circuit modifying the frequency of a voltage controlled oscillator (VCO) are used [22]. This principle is implemented in [23] to create a variable spectrum of a ring-oscillator based digital pulse-width modulator (DPWM). On the other hand, an all-digital solution based on modifying resolution of a counter based DPWM [24], as authors explained, results in voltage regulation problems.

A digital architecture suitable for implementation in the latest CMOS technologies, providing variable switching frequency and EMI mitigation, without the above mentioned problems is presented in the following subsection.

A. All-digital clock divider and spread spectrum generator

The all-digital clock divider and spread spectrum generator, generating both variable fundamental frequency and spread-spectrum frequency components, is shown in Fig. 2. Unlike conventional spread-spectrum implementations, utilizing a constant-frequency master clock, the proposed solution modifies the master clock frequency based on both the input voltage and desired spread spectrum bandwidth.

The operation of the generator can be described through the diagram of Fig.2 and corresponding waveforms of Fig. 3. The DPWM c*lk* signal is generated by a combined ring oscillator and 2^m:1 multiplexer. The multiplexer selects the location, ie. cell, where the pulse propagating through the 2^m-cell ring oscillator is transmitted to the output. Selection of the active input is performed with a wraparound adder producing digital signal s*el*[*n*]=s*el*[*n*-1] + *k*[*n*], where *k*[*n*] is a variable depending on $f_{sw} = f_{sw\_f} + f_{ss}$.

As seen in Fig.3, showing waveforms of a 64-cell generator, the lowest frequency is produced when *k*[*n*]=0. The pulse propagating through the ring-oscillator is transmitted through the first multiplexer input, in_0, resulting in a clock with a $64T_d$ period, where T_d is propagation time of each ring oscillator cell. For different values of *k*[*n*], the active multiplexer input changes resulting in faster frequencies. For *k*[*n*] = 30 (decimal), assuming s*el*[0]=0, the wraparound adder increments the active multiplexer input by 30 (i.e. such that the multiplexer input select pattern becomes 0, 30, 60, 26, 56,..,) resulting in a clock signal with a $30T_d$ period.

It can be seen that the frequency of the clock changes as

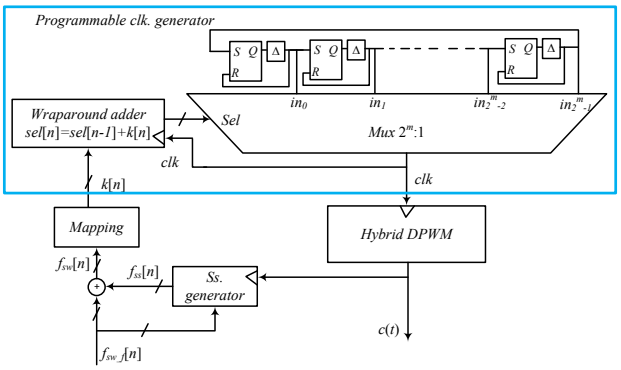

Fig.2: All-digital clock divider and spread spectrum generator.

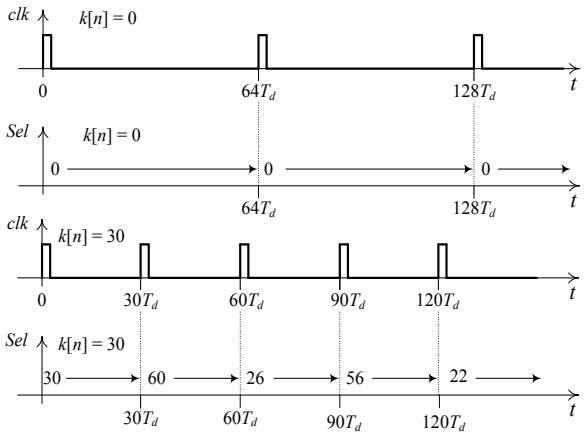

Fig.3: Key waveforms of 64-cell clock generator. Top two: for $k[n] = 0$; Bottom: for $k[n] = 30$.

$f_{clk} = 1/(kT_d)$ and 2^m discrete period steps can be obtained. Since the clock frequency is inversely proportional to the control signal $k[n]$, a mapping circuit is used to convert an input $f_{sw}[n]$ into the corresponding control value.

A.1) Simplified design for the clock divider module

A simplified clock divider and spread spectrum generator module is proposed in Fig.4, improving the monotonicity of the ring oscillator and reducing area requirement for possible IC implementation. The simplified implementation uses only two delay cells and an enable input to generate the desired clock frequency. The enable input is generated by a shift register block. The shift register performs division-by-2 operation each time the pulse is circled back through the ring oscillator until the quotient of the division becomes zero, while the output of the remainder block selects the mux output. Once the quotient is zero the enable input is driven high, generating a *clk* pulse. At this point, the wraparound adder updates the value of $sel[n]$ for the next cycle and the process is repeated.

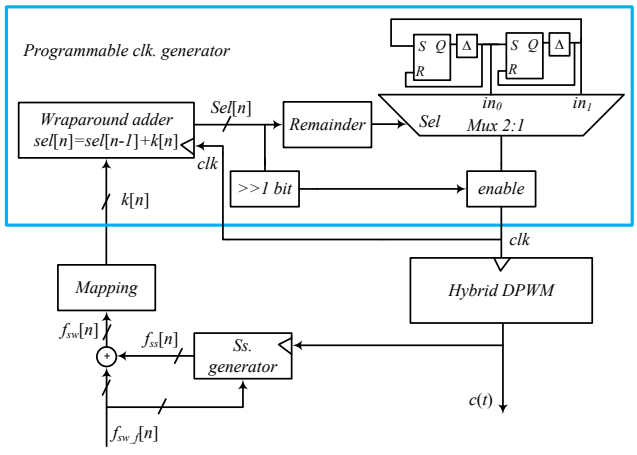

Fig.4: Simplified clock divider and spread spectrum generator.

B. Programmable spread-spectrum generation

To create a spread-spectrum modulating signal $f_{ss}[n]$ a pseudo-random number generator (PRNG) based on a linear feedback shift register [25] is modified such that its numbers range can be adaptively changed.

Figure 5 shows the modified PRNG that can create up to 2^p-1 different $f_{ss}[n]$ numbers in a pseudo random fashion. This generator is triggered by the rising edge of the pulse-width modulated signal c(t) (Figs. 1 and 2) and changes its value after each switching cycle. The range of the numbers produced by the generator is selected depending on the value of the fundamental frequency signal f_{sw_f}. For lower frequencies the f_{ss} range decreases keeping the ratio between the maximum f_{ss} variation and f_{sw_f} constant, limiting the degradation of the inductor ripple. The variation of the frequency range is performed by changing the number of the shift register in the feedback loop, using a demultiplexer controlled by most significant bits of f_{sw_f}.

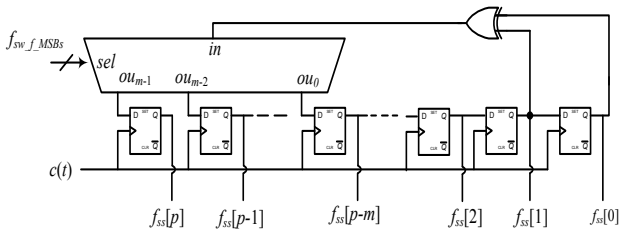

Fig.5: PRNG based on variable-length shift register.

IV. Experimental System and Results

To verify operation of the system shown in Fig. 1, an FPGA-based controller prototype was created. It controls operation of a 1.8 V, 5 W buck converter. The input voltage of the system is varied between 2.75V and 5.5V emulating behavior of a Li-ion battery cell.

A. Functional verification

To test the ability of the system to keep the ripple at a constant level, the spread spectrum block is temporarily disabled. Figure 6 shows response of the system for sudden variations of the input voltage. The results confirm that the new architecture provides tight control of the current ripple amplitude while adaptively changing the switching frequency depending on the input voltage.

Figures 7 and 8 show input current spectrum measurements for the converter operating in steady state at frequency of 780 KHz before and after the activation of the spread spectrum circuit, respectively. It can be seen that the spread spectrum circuit effectively reduces the low-frequency fundamental component mitigating potential EMI problem. Figure 9 shows the inductor current waveform when the read-spectrum module is enabled.

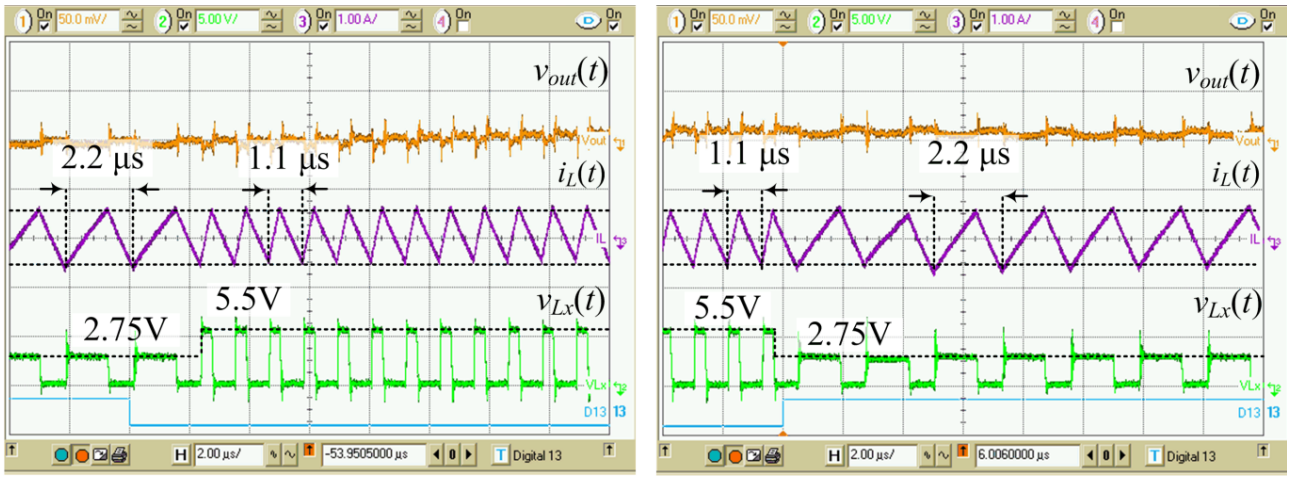

Fig.6: Response of the adaptive switching frequency controller for sudden variations of the input voltage. Ch.1: output voltage of the converter (50 mv/div); Ch.2: inductor current (1A/div); Ch.3: switching node voltage of the buck converter (5V/div); D13: voltage transient control signal (digital signal). The time scale is 2 µs/div.

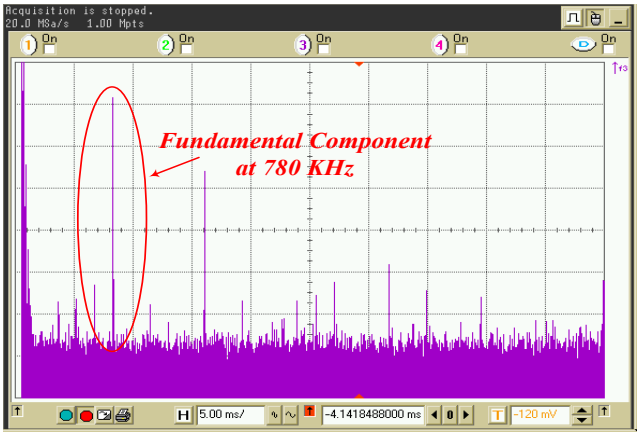

Fig.7: Input current conducted EMI for fixed frequency. FFT operation performed with Y-axis: 5db/div, X-axis: 500 KHz/div.

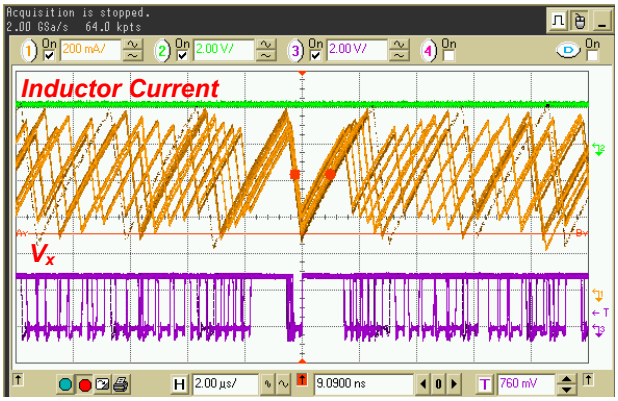

Fig.9: Inductor current waveform and V_x node for spread spectrum. Ch.1: Inductor current (200mA/div); Ch.2: Output voltage (2V/div); Ch.3: V_x node (2V/div). The time scale is 2 µs/div.

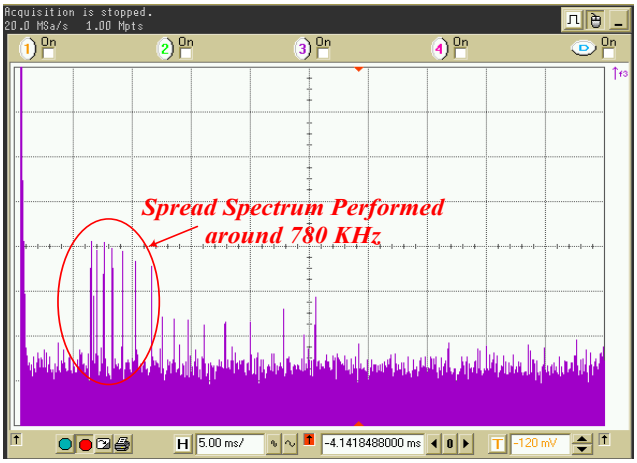

Fig.8: Input current conducted EMI for Spread Spectrum. FFT operation performed with Y-axis: 5db/div, X-axis: 500 KHz/div.

B. Efficiency Improvement

Figures 10 and 11 compare the converter efficiency when the system operates at a constant switching frequency of 2 MHz and when the switching frequency is adaptively varied based on the input voltage. The results are shown for two different output load condition. It can be seen that the adaptive frequency controller results in an up to 2% efficiency improvement, translating into a larger than 18% reduction of the total losses.

Finally, Fig. 12 shows the efficiency comparison over the wide range of load currents for an input voltage of 2.75V. The switching frequency was scaled down to 780 KHz from 2 MHz. The efficiency improvement is around 2% over the entire range of load currents. This observation makes the proposed solution very attractive for portable applications

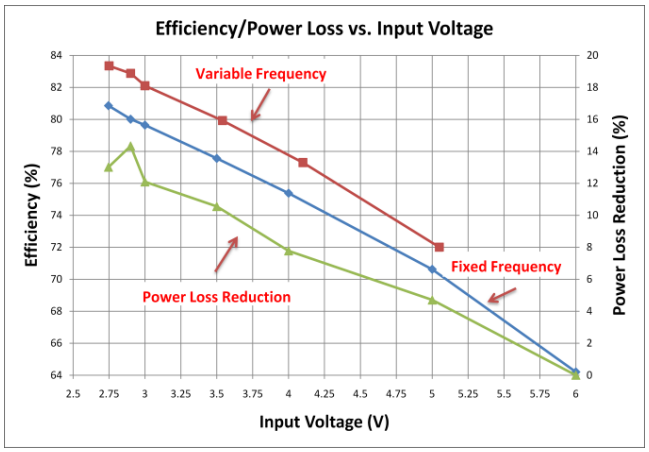

Fig.10: Efficiency comparison for fixed frequency and variable frequency operation for 500 mA load current.

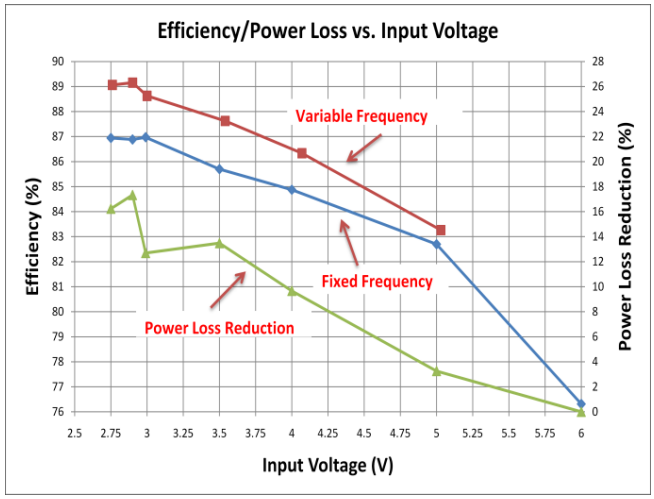

Fig.11: Efficiency comparison for fixed frequency and variable frequency operation for 1.25 A load current.

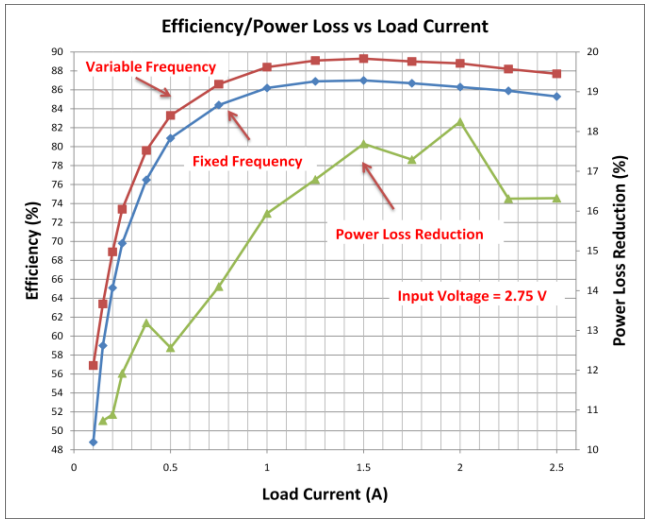

Fig.12: Efficiency improvement over wide range of load currents.

where as the lithium-ion battery discharges, resulting in reduction in input voltage, the efficiency of the converter increases over the entire range of load conditions.

V. Conclusions

An adaptive frequency all-digital controller architecture improving efficiency of dc-dc supplies is presented. The architecture well suited for on-chip integration in the latest CMOS technologies allowing utilization of digital implementation advantages. Depending on the input voltage, the controller adaptively changes the switching frequency reducing losses while minimizing EMI problems related to the variable frequency operation. The key controller element is novel *clock divider and spread spectrum generator* allowing dual modulation of the clock generator, depending both on the spread spectrum and input voltage requirements. Experimental results prove the effectiveness of the system.

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