A 10 MHz Mixed-Signal CPM Controlled DC-DC Converter IC with Novel Gate Swing Circuit and Instantaneous Efficiency Optimization

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***Abstract*— This paper introduces a mixed-signal peak current-programmed mode controlled 10 MHz dc-dc converter integrated circuit (IC) for low-power applications. The IC combines segmented power transistors, gate drivers and the main functional blocks of a multi-mode controller. Based on the information about the peak transistor current, obtained from the voltage loop, the controller instantaneously changes the number of segments, gate drive voltage, or switches to pulse-frequency modulation, such that for each operating point efficiency is optimized. To obtain reliable operation at such a high switching frequency and achieve efficiency optimization novel architecture of gate swing circuit is combined with modifications of known designs of other functional blocks. Experimental verification of a 0.6 W buck converter IC, fabricated in a 0.13 µm process, demonstrate the peak efficiency of an 83%, near time-optimal dynamic response, and up to a 20% efficiency improvement due to the action of the efficiency optimization controller.**

I. INTRODUCTION

Small volume and high power processing efficiency over the full operating range are key requirements for on-chip integrated low-power dc-dc switch-mode power supplies (SMPS) used in battery-powered portable applications. To achieve these goals, operation at high switching frequencies combined with efficiency improving multi-mode control is usually preferred. Based on the load conditions, these multi-mode systems apply techniques such as variation of the number of power switch segments [1-3], non-overlapping dead-time adjustment [4], switching between pulse-width and pulse-frequency modulation (PFM) [5], and gate voltage variation [6-8]. Readily available voltage mode controlled SMPS integrated circuits (IC) operating at switching frequencies beyond 4 MHz [9] allow a small volume implementation but are not best suited for the on-line efficiency optimization, due to the highly dynamic nature of the modern loads. In high-frequency (HF) voltage mode SMPS, the efficiency improving on-line mode changes are usually performed in steady state, based on the estimated/measured output current value [1]. In this way, erroneous mode of operation during transients that can potentially damage the power stage components is avoided. As a consequence, the benefits of the multi-mode operation reduce or, in some cases, completely vanish as the load change frequency increases.

To eliminate the problems of voltage mode implementation, a discrete-implementation of mixed-signal peak current-programmed mode (CPM) dc-dc converter that provides instantaneous efficiency optimization was proposed [6]. It utilizes inherently available current loop reference to determine instantaneous current for each switching cycle and, accordingly, sets up the most efficient mode of operation using digital logic. The major drawback of this system and other solutions that implement efficiency optimization techniques [7] is reliability issues related to floating gate of power transistor or large number of transistor segments. Another important drawback of this solution as well as that of integrated mixed-signal [10] and analog CPM solutions is significantly smaller switching frequency than that of the voltage-controlled systems. The absence of mixed-signal CPM solutions operating at frequencies comparable to the voltage mode ICs is mostly caused by two unsolved implementation problems. The first problem is related to power consumption of the current sensing circuit reducing the SMPS efficiency. The second is related to the design of a digital-to-analog converter (DAC) for the current loop reference setting. It suffers from a tradeoff between power consumption and accuracy, which affects the output voltage regulation.

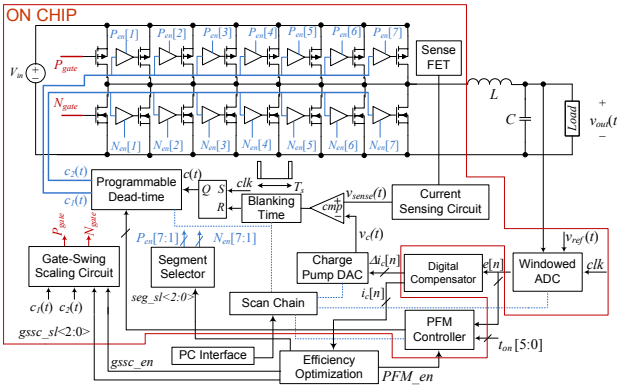

Fig.1:Integrated mixed-signal CPM IC.

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The main goal of this paper is to introduce a mixed-signal CPM dc-dc converter IC of Fig.1 that operates at 10MHz switching frequency and performs instantaneous efficiency optimization, by dynamically changing modes of its operation over a wide load range. In addition to operating at the switching frequency comparable or even higher than the state of the art voltage mode solutions [9], the presented IC is also able to maintain tight output voltage regulation over a wide range of load currents allowing for the implementation of efficiency improvement techniques. Depending on the load current, the dc-dc converter automatically changes the number of segments of the power transistors, dynamically adjusts power transistor gate voltages, and switches between continuous conduction and pulse frequency mode of operation, to maximize efficiency for any given operating point.

As described in the following sections, the high performance of the IC and its efficiency optimization features are obtained by combining novel architectural solutions for the system functional blocks and by modifying previous designs. Namely, the current sensing circuit design is optimized by utilizing advantages of instantaneous power transistor and gate-drive segmentation and a high-resolution current reference adjustment is achieved with a new design of a charge-pump DAC (CP-DAC). Equally important, the IC incorporates a novel gate swing scaling circuit (GSSC) architecture that eliminates the floating gate problem of the previous solutions [6-7] and, at the same time, reduces the need for a high level of transistor segmentation, both of which cause serious reliability problems.

II. System Description

The system of Fig.1 operates as a modification of mixed-signal peak current program mode controller [11], where the voltage loop is digital and the internal current loop is analog. The output voltage error is sampled and converted into its digital equivalent $e[n]$ with a windowed analog-to-digital converter (ADC) [12]. Based on the error signal, a digital compensator creates the differential current reference $\Delta i_c[n]$. This information about upcoming current value is passed to the charge-pump DAC, which sets the limit for the peak inductor current during each switching cycle. The digital compensator also creates the current reference $i_c[n]$ that is used as the control signal for the instantaneous efficiency optimization. The operation of the efficiency optimizer can be described by assuming that the load current changes from its maximum to a very low value. At heavy loads all transistor segments of Fig.1 are active and, as the load reduces the number of segments decreases, so a favorable tradeoff between conduction and switching losses is achieved [2]. For medium-to-light loads only one transistor segment is active and the on-line efficiency optimization is obtained by changing the gate drive voltage, with the GSSC. For even lighter loads the converter switches to pulse-frequency mode of operation further minimizing switching losses.

A. Two-Pulse Controlled Charge-Pump DAC (CP-DAC)

The charge pump DAC of Fig.1 operates as the interface between the digital voltage loop and the analog current loop. The application of a CP-DAC for mixed-signal CPM dc-dc converters was proposed in [10]. Compared to sigma-delta or flash DACs, the CP-DAC allows higher conversion rates without excessive power consumption. The resolution of the previously proposed CP-DAC decreases as the digital input increase. Therefore, it suffers from inherent nonlinearity affecting voltage regulation and the gain of the feedback loop. In the design introduced here, the CP-DAC is modified such that the high resolution is maintained throughout the whole operating range. This modification not only improves the voltage regulation but also allows implementation of fast dynamic response control laws that usually require accurate control signals [13-16].

The CP-DAC of Fig.2 is a modified combination of current-switched DAC and a conventional charge pump circuit[17].It operates as follows: The output voltage, i.e. reference for the current loop, is changed by charging/discharging the output cap C_{cp}, with transistors Q_4 and Q_5 that behave as current sources mirroring the current of the digitally programmable current sink. The amount of charge is regulated by controlling both the charge duration and the current of the sink. In the previously presented design [10] both the current and the timing are regulated in relatively crude discrete steps and the charge amount, determined based on the product of the two, is changed in a single pulse. As a consequence, the minimum amount of charge that can be changed in a single pulse and, hence, the quantization step of the DAC reduces as the charging time increases. To overcome this problem, in this modification of the CP-DAC, the amount of charge is modulated in two steps using the timing controller. In the first step, the 4 least significant bits (LSB-s) of the signed input digital signal $\Delta i_c[8:0]$, i.e. $\Delta i_c[3:0]$ are used to set up the current of the

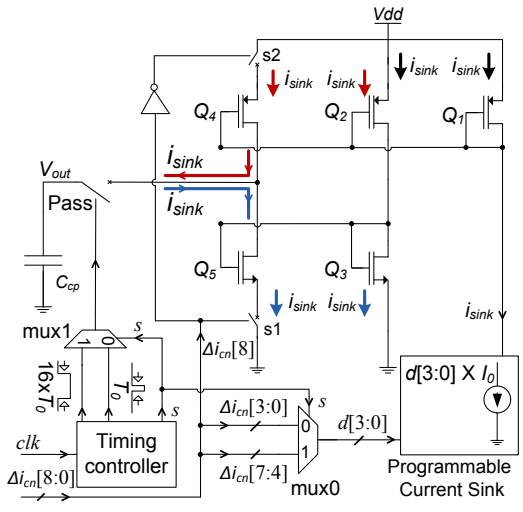


Fig.2: CP-DAC Block Diagram.

current sink and the charging/discharging is performed over T_0 interval. Then, in the following step, the 4 most significant bits (MSB-s), $\Delta i_c[7:4]$, are sent to the current sink and during a $16T_0$-long time interval the capacitor charge is changed. As a result, accurate charge control and high resolution of the DAC over the whole range is obtained.

As mentioned previously, in addition to $\Delta i_c[n]$, the digital compensator also creates the current reference $i_c[n]$ that is used as the control signal for the instantaneous efficiency optimization. One drawback of CP-DAC architecture [10] shown in Fig.2 is that due to mismatches in charging and discharging of output capacitor, the compensator cannot accurately track the $i_c[n]$. This could cause the optimization controller to change modes of operation based on $i_c[n]$ that is not a valid representation of instantaneous peak inductor current. To overcome this problem, the current mirrors used in CP-DAC were designed using cascode transistors in order to reduce the mismatches. An additional mismatch compensation factor was incorporated in the digital compensator design based on measurements of CP-DAC circuit.

B. Current Sensing

In the targeted low-power on-chip integrated converters, SenseFET circuits [18], similar to the one shown in Fig.3, are usually used to create a voltage waveform $v_{sense}(t)$ that accurately replicates the current waveform of the power transistor. To achieve good linearity and accurate measurement over the full range of operation, in

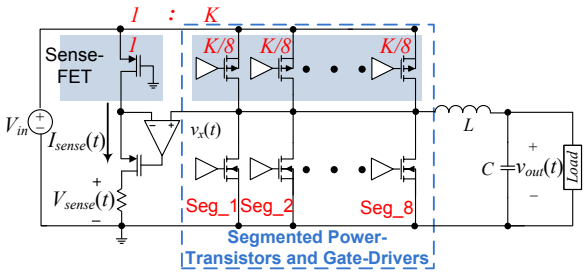


Fig.3:Current sensor with segmented power-transitors

conventional implementations without power stage segmentation, a power hungry amplifier with a very large gain-bandwidth (GBW) is usually required [18]. This requirement is related to the varying properties of the sensed voltage across the power MOSFET, $v_x(t)$. At light loads, it is usually a small signal requiring a strong amplification and at heavy loads the signal contains significant high frequency content pushing the bandwidth requirements of the amplifier. For the amplifier of Fig.3 the existence of the segmented power transistor is utilized to relax GBW amplifier requirements and, consequently, reduce its power consumption allowing CPM implementation at high switching frequencies. In this case, the range $v_x(t)$ variation is reduced, since at light loads the inductor current is passed through a comparatively large resistance. Furthermore, since the signal-to-offset ratio is significantly improved compared to the conventional non-segmented solutions, the amplifier offset requirements are significantly reduced allowing a simpler implementation occupying smaller silicon area.

C. Gate Swing Scaling Circuit (GSSC)

Segmentation of power transistors and gate-drivers in low-power SMPS at light-to-medium loads creates a favorable tradeoff between conduction and gate-drive losses improving converter efficiency [1]. This improvement extends over a wider range of loads as the number of segments increases. However, from the practical point of view, a high level of transistor segmentation causes serious reliability issues. Due to imperfections and timing delays caused by the circuit layout and process, voltage and temperature variation (PVT) , switching of some segments and their gate drivers can be significantly delayed causing large amounts of current to pass through a small portion of the transistor and, result in consequent, failures. To minimize the mismatch effect, an alternative solution based on using a smaller number of segments that are simpler to match and gate voltage variation technique also known as, gate swing scaling, are proposed. In the previous art the gate swing technique was implemented using pulsed-controlled drivers [6-7]. The major drawback of these implementations is that the gate of the power transistor is floating during most of the period that it is on. Since there is no low-

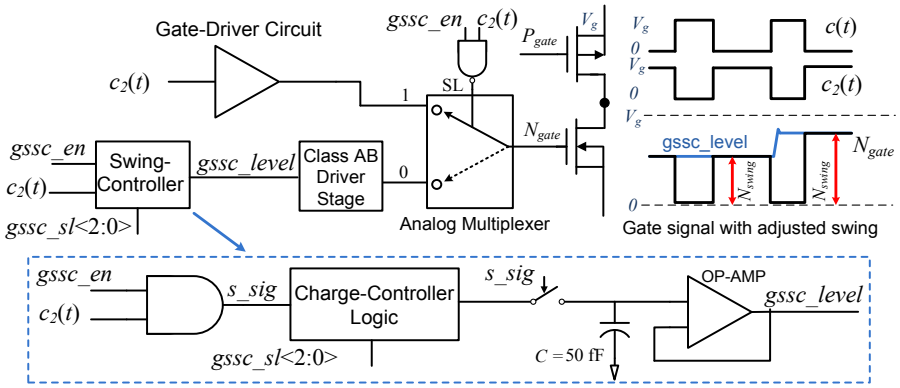


Fig.4: a) Top shows the GSSC architecture with waveforms describing its operatio b) Bottom shows the block diagram of Swing-Controller block.

impedance path driving the gate of the power transistor, it can easily be disturbed by injection of charge from the outside. A new structure for gate-swing scaling circuit (GSSC) is proposed here to overcome this problem. As shown in Fig.4 the new architecture is based on modifying a conventional gate-driver structure such that a gate voltage signal with programmable swing turns on the power transistors. To achieve this three new blocks i.e., the swing-controller, the class AB driver stage and an analog multiplexer switch are used in this new architecture. The structure of Fig.4 shows the implementation of GSSC for low-side power transistor and the implementation is equivalent for the high-side transistor. The operation of GSSC can be described by looking at Fig.1 and Fig.4. The transistor gate can be either driven by the conventional gate-driver or GSSC circuit. When *gssc_en* is enabled by the optimization controller, based on the control signal $c_2(t)$, the gate of the power transistor is either discharged to zero through the gate-driver circuit or charged to *gssc_level* by the class AB driver stage. The swing-controller, shown in Fig.4.b consists of the *charge_controller* logic block, and a simple sample and hold circuit. Based on the efficiency optimization control signal *gssc_sl*<2:0>, the *charge_controller logic* controls the amount of charge transferred to capacitor *C*. It therefore adjusts the *gssc_level* to one of the 8 possible voltage swing levels. In this way, when the gate of the power transistor turns on, it is continuously held at the voltage *gssc_level* by the sample and hold circuit and analog class AB driver stage which provide the low-impedance pass to the gate. Therefore the gate of the power transistor is never floating and reliability problems of the previous designs are avoided.

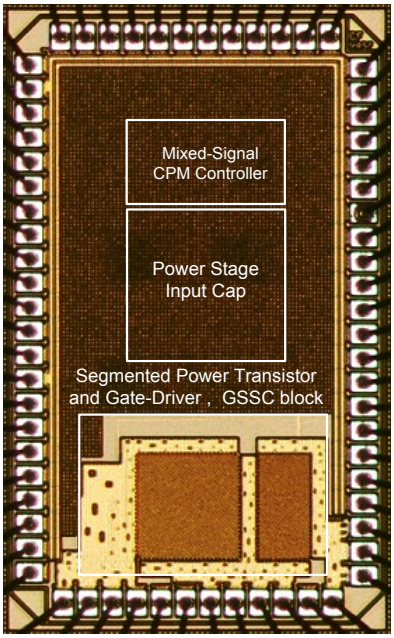


Fig.5: Die Photo of CPM IC

Table I

Specifications	Value	Units
CMOS Process	0.13	µm
Area	3.75	mm2
Input Voltage	2.5	V
Output Voltage	0.8-1.3	V
Rated Load	500	mA
Filter L,C	400, 0.9	nH,µF
Switching Frequency	10	MHz
Ron Pmos , Nmos	0.26 , 0.234	Ω
Supply Analog , Digital	1.2, 2.5	V
Peak Efficiency	83	%
CPM Controller Current	500	µA
PFM Controller Current	10	µA
Digital Core	200	µA

III. On-Chip Implementation and Experimental Results

The integrated mixed-signal CPM of Fig.1 was fabricated in 0.13µm technology. The chip micrograph is shown in Fig.5 and Table I summarizes its main specifications. The die measures 2.5 × 1.5 mm^2, while the total active area of the mixed-signal CPM controller is 0.25 mm^2. The total power consumption of the controller is around 1.45mW in CCM and 10µ in PFM mode. The *efficiency optimization controller* of Fig.1 is implemented on FGPA that is used for testing the mixed-signal CPM IC. The FPGA also programs the scan chain on chip in order to set various configuration signals on IC.

A. ADC

The transfer characteristic of ADC is shown in Fig.6. The steady-state error bin was created to be around 7mV and other error bins are around 12mV. The ADC has a two bit resolution setting that can be set through the scan chain. This allows increasing the steady-state error bin to 9mV. The outputs of ADC's delay-line are converted to e_n[3:0] shown

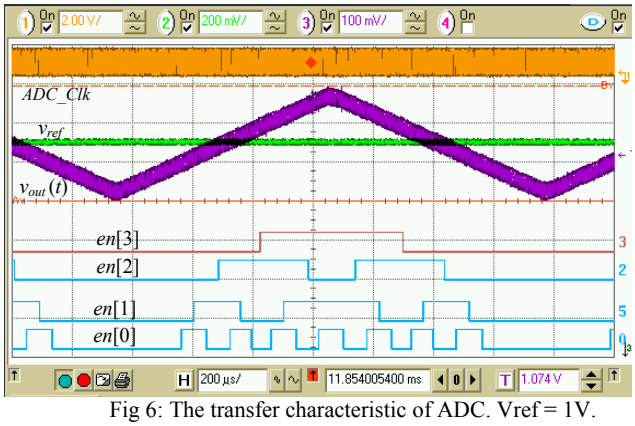


Fig 6: The transfer characteristic of ADC. Vref = 1V.

in Fig.6, using a gray encoder block. This way, the error toggles one bit at the time and encoder design is simplified. The ADC current consumption is around 50µA and it achieves conversion rate of 35ns in normal operating conditions. The ADC is operational for $0.5V < V_{ref} < 1.8V$

B. Closed-Loop Response

To verify the closed loop response of the converter in CPM and fast response of CP-DAC, Fig.7 shows the results of converter operation with near time-optimal controller[13-16] to a 150mA-450mA load step. The light to heavy load transient is shown in Fig.7.a. Upon detecting the load transient, the CP-DAC sets $\Delta i_c[n]$ to the new calculated peak current value and the main switch is turned on. The inductor current rises until it reaches the new current command value. Subsequently the main switch is turned off and the digital compensator resumes the operation. The controller performs similar operation for heavy to light load transient. As shown in Fig.7 the controller recovers the output voltage to the new steady-state value in 500ns with voltage deviation of about 60mV.

C. Efficieny Optimization

The efficiency measurements of the system operating at 10MHz are shown in Fig.8 with the optimization techniques discussed in this paper. While segment adjustment improves efficiency by as much as 3%, i.e. reduces losses by 13%, at medium load currents, GSSC allows for improvements of around 8% (loss reduction of 26%)at light to medium loads. For load currents below 7mA the controller operates the power-stage in PFM mode for additional savings.

The operation of GSSC block with converter running in closed-loop is shown in Fig.9. The output of the GSSC block is directly connected to power transistors of the smallest segment as shown in Fig.1 and Fig.4.a. For the purpose of experimental verification a copy of GSSC block was also implemented on chip. The outputs of this block, $P_{gate}(t)$ and $N_{gate}(t)$ are directly connected to output pads and shown in Fig.9. Before GSSC is enabled both outputs are operating at full swing. It is clear from Fig.9 that the rise time of $N_{gate}(t)$ is larger compared to $P_{gate}(t)$. The GSSC circuit for the low-side transistor is designed with around half the load capacitance of the circuit for the high-side transistor. However in case of Fig.9 both circuits see the same pad capacitance and therefore $N_{gate}(t)$ has a bigger rise time.When GSSC circuit is enabled, *gssc_sl<2:0>* is changed randomly and as shown in Fig.9 the transistor gate swing signals are scaled without causing any perturbations in the output voltage.

The dynamic operation of the converter with optimization controller is shown in Fig.10.

Fig 10.a shows the transient response of the system with a simple PID controller as the load changes from light to heavy. Initially at light load, only one segment is on and the GSSC block is enabled by the optimization controller. When the transient occurs , $i_c[n]$ increases with inductor current. Therefore the optimization controller dynamically scales the gate voltages to full swing, turns off the GSSC and turns on all the segments. For the heavy to light transient shown in Fig10.b, the controller turns off all the segments except the smallest, turns on GSSC block and reduces the gate voltage swing. As the current command $i_c[n]$ reduces below the final load current, the optimization controller scales the gate swings below their final value for a short duration.

The operation of the system in PFM mode is shown in Fig.11. As the load changes from heavy to light, the optimization controller detects the PFM mode based on the $i_c[n]$, disables GSSC block to minimize power consumption and enables the PFM mode.

IV. Conclusion

A mixed-signal peak current-programmed mode controlled 10 MHz dc-dc converter IC has been presented in this work. The IC consists of segmented power transistors and gate drivers, mixed-mode CPM controller and efficiency optimization blocks. An optimization controller, based on inherent current information in control loop, dynamically adjusts the number of segments, scales the gate voltage swing of transistors and switches to PFM mode of operation in order to improve efficiency at different operating points. To obtain reliable operation at such a high switching frequency and achieve efficiency optimization novel

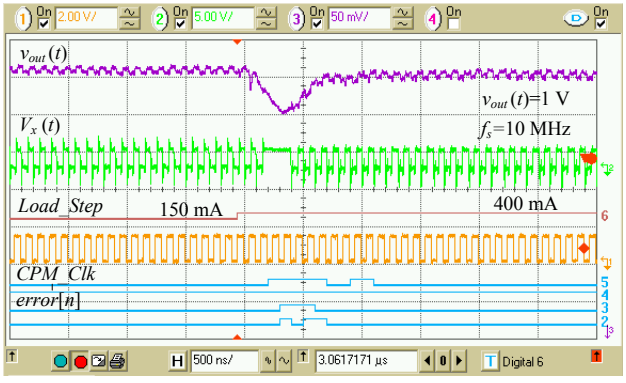
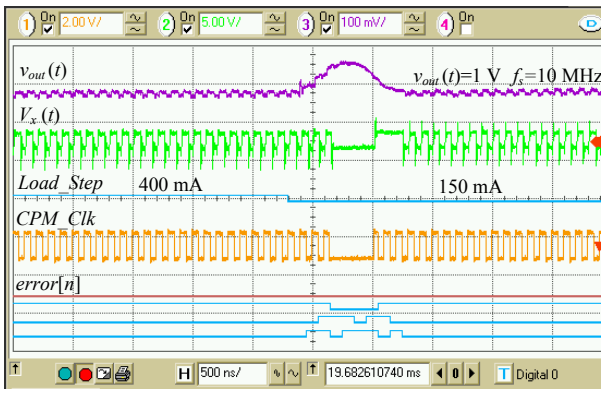


Fig.7: a) Light to heavy transient response with time-optimal controller



b) Heavy to light load transient response

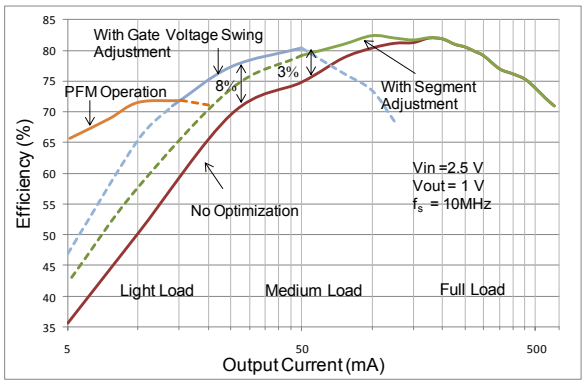


Fig.8: Efficiency measurements of Mixed-Signal IC

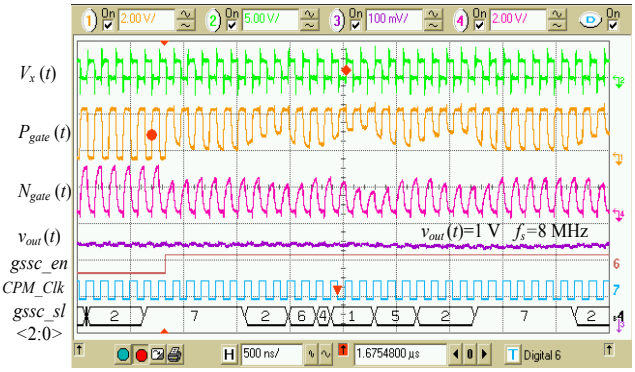


Fig.9: The operation GSSC block with converter in closed loop

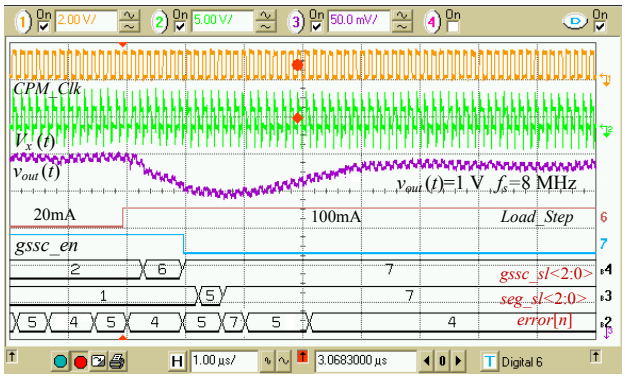
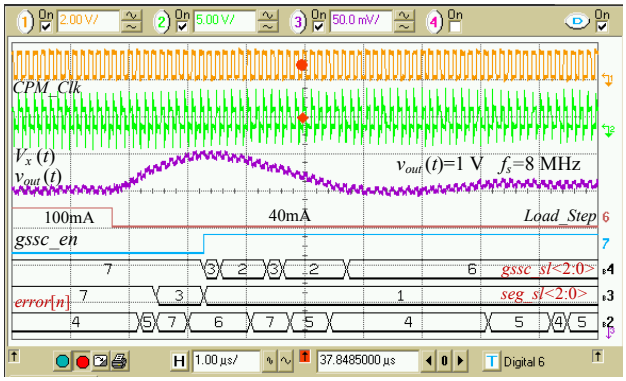


Fig.10: a) Operation of the optimization controller during light to heavy transient response with PID controller



b) Operation of the optimization controller during heavy to light transient response

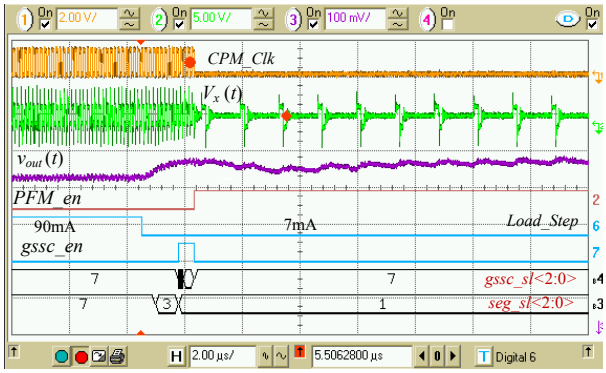


Fig 11: Operation of the system in PFM mode

architecture of gate swing circuit is combined with modifications of known designs of other functional blocks. Experimental verification of a 0.6 W, 10 MHz buck converter IC, fabricated in a 0.13 µm process, demonstrate the peak efficiency of 83%, near time-optimal dynamic response, and up to 20% efficiency improvement due to the action of the efficiency optimization controller.

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