Flyback Transformer Based Transient Suppression Method for Digitally Controlled Buck Converters

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Abstract— **A current-programmed mode (CPM) digitally controlled buck converter with a flyback transformer is proposed in this work. It achieves fast and smooth dynamic response with a smaller area and volume penalty than most of the other augmented converter solutions. During load transient recovery, current slew-rate of the power inductor is boosted to suppress voltage deviation with the help of the secondary winding of a flyback transformer and three small auxiliary switches. Since the auxiliary switches are not in the main power conduction path and only need to handle occasional current pulses, their size can be minimized without degrading the conversion efficiency. Experimental results with a 6V-to-1V, 3W prototype show a 50% reduction in peak voltage deviation when comparing to a conventional CPM buck converter.**

I. INTRODUCTION

Modern switch-mode power supplies (SMPS) used for point-of-load (POL) applications need to meet increasingly stringent requirement on voltage regulation. VLSI manufacturers typically impose tight tolerance on the supply voltage to ensure proper performance [1]. To satisfy these, SMPS are usually required to have small output voltage deviation during transients. The preference for high conversion efficiency and small physical size makes the design of SMPS even more challenging.

Minimization of LC filter and operation at high switching frequencies can improve transient performance but they also degrade efficiency of a buck converter. A number of nonlinear control strategies have been proposed to mitigate this trade-off [2-18]. Time-optimal methods based on state space and capacitor charge balance algorithm have been demonstrated in [2-7]. In these systems, a digital controller determines the turn-on and turn-off times of the power switches, such that the output voltage and the inductor current are restored in a single on/off switching action. The algorithm provides fast transient response with short recovery time. A comparatively simpler solution aiming at optimal voltage deviation was applied to a two-phase buck converter in [8]. The digital controller recovers the inductor current with one on/off switching action to achieve the minimum possible transient voltage deviation. However, the peak overshoot/undershoot of these converters [2-8] is inherently limited by the current slew-rate in the power inductor. To overcome this physical limitation, a buck converter with steered inductor was introduced in [9, 10]. However, this method can only increase inductor current slew-rate during heavy-to-light load transients. It also requires an extra bi-directional switch in the power path. An alternate approach has been proven to be effective in [11-17], where a small auxiliary power stage was connected in parallel with the main output stage. The auxiliary stage is activated during transient recovery to provide high current slew-rate. Yet, it comes with the penalty of a separate inductor [11-15] handling the maximum load current or two extra magnetically coupled inductors [16, 17] and extra switches, which considerably increases cost and consumes PCB real estate.

A single phase voltage regulator module (VRM) with stepping inductance was investigated in [18]. A three-winding transformer replaces the power inductor in a buck converter. Depending on the property of load transient, the secondary or the tertiary winding of the transformer is shorted to a voltage source during transient recovery to generate a constant voltage drop across the primary winding. The equivalent inductance in the power stage is therefore reduced and approximately equal to the leakage inductance of the transformer. This technique allows rapid changes in the inductor current. However the control method in [18] requires multiple switching cycles before the output voltage could return to steady state and results in a relatively long settling time.

In this paper, a digitally controlled current-programmed mode (CPM) buck converter with a flyback transformer is proposed. When a load transient is detected, the current slew-rate in the power stage is increased with the help of the

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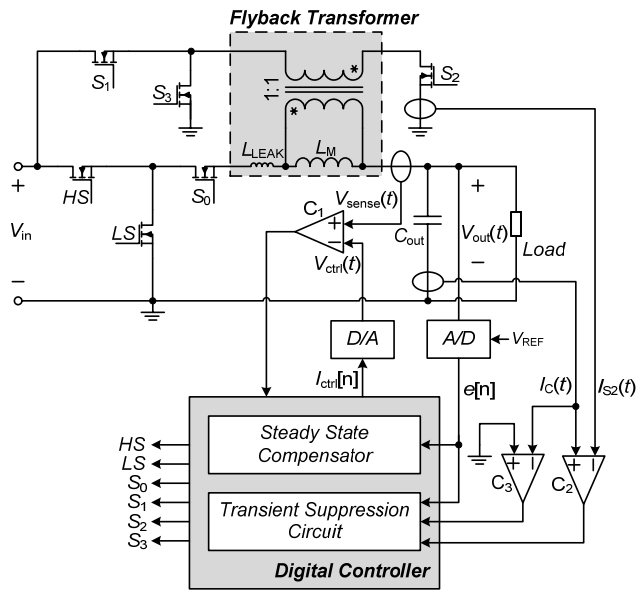

Figure 1. The proposed buck converter with a flyback transformer for load transient suppression.

secondary winding of the flyback transformer and several small auxiliary switches. Peak voltage deviation during both heavy-to-light and light-to-heavy load transients is suppressed without sacrificing settling time. This structure introduces only one extra single-directional switch, S_0 in the power path. It does not increase the total size of inductive components, since the size of the flyback transformer is comparable to that of a conventional inductor.

II. System Structure and Operating Principle

The proposed system is as shown in Fig. 1. The output power stage is a modification of a conventional buck converter, where the inductor is replaced with a flyback transformer. The flyback transformer is modeled as a leakage inductor L_{LEAK} and a magnetizing inductor L_M, which is in parallel with an ideal 1:1 transformer. L_{LEAK} and L_M together serve as the power inductor. The secondary winding of the flyback transformer is connected to three auxiliary switches $S_1 \sim S_3$. These auxiliary switches are used in pairs during transient recovery to control the voltage applied across the secondary winding, which in turn manipulates the current flowing through the primary winding. A two-mode digital controller generates the switching commands for the main and auxiliary switches. In steady state the compensator regulates the system operation while the transient suppression circuit is active during load disturbances.

A. Steady-state Operation

In steady state, S_0 is kept on, the auxiliary switches S_1~S_3 are kept off. The converter functions as a conventional buck with output filtering inductance L_M+L_{LEAK}. The digital controller operates in peak current-programmed mode (CPM). It controls the high-side (*HS*) and low-side (*LS*) switches to maintain output voltage (V_{out}) regulation.

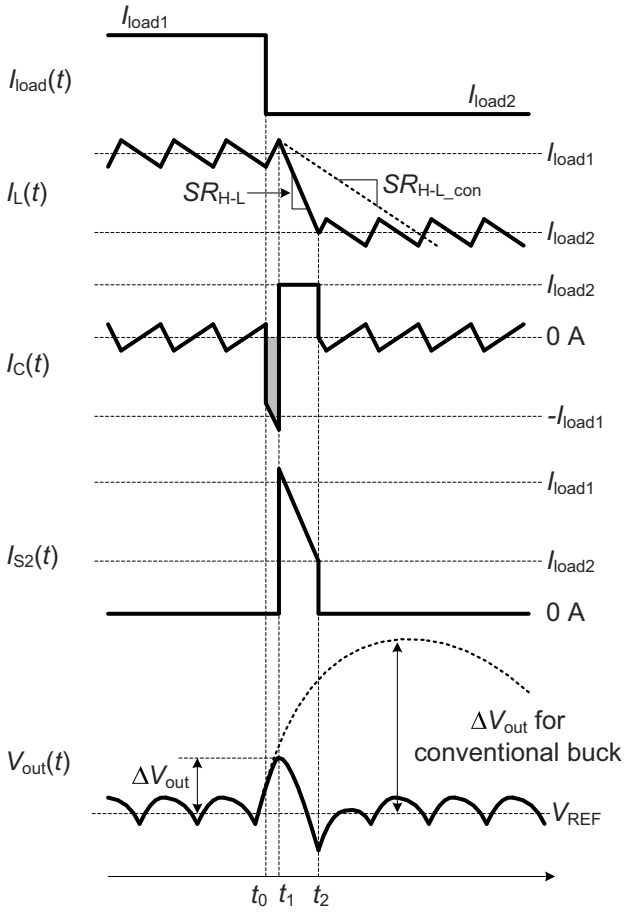

Figure 2. Theoretical current and voltage waveforms during a heavy-to-light load transient recovery process.

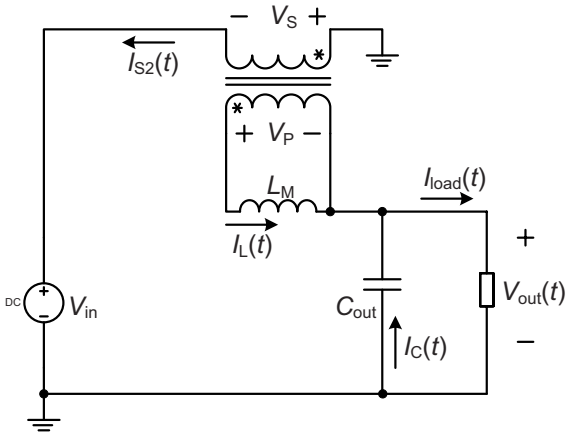

Figure 3. Equivalent circuit during heavy-to-light load transient recovery.

B. Heavy-to-light Load Transient Recovery

Theoretical current and voltage waveforms during a heavy-to-light transient recovery process are illustrated in Fig. 2 and will be described in this section.

At t_0, the load current $I_{load}(t)$ steps from I_{load1} to a lower value I_{load2}. Excess current from the transformer flows into

the output capacitor C_{out} and forms a negative current $I_C(t)$. The output voltage $V_{out}(t)$ rises due to this negative $I_C(t)$. The amount of overshoot ΔV_{out} is proportional to the integral of $I_C(t)$ over time t_0 to t_1, which is represented by the shaded area surrounded by the $I_C(t)$ curve in Fig. 2.

When this transient is detected at t_1, the *HS* and *LS* transistors and S_0 are switched off; S_1 and S_2 are switched on. The equivalent circuit of the power stage is as shown in Fig. 3. As can be seen, a constant voltage V_P is induced across the primary winding of the transformer, and

$$V_P = -V_{in}\,, \tag{1}$$

where V_{in} is the input voltage of the buck converter. This induced voltage changes the voltage across the magnetizing inductance and improves its current slew-rate $SR_{H\text{-}L}$ to

$$SR_{H\text{-}L} = V_P / L_M = -V_{in} / L_M\,. \tag{2}$$

In comparison with the current slew-rate of a conventional buck converter under the same transient condition, $SR_{H\text{-}L\_con}$

$$SR_{H\text{-}L\_con} = -V_{out} / L_M\,, \tag{3}$$

the slew-rate described with (2) is drastically improved, since in the targeted applications V_{in} voltage is usually much larger than V_{out}.

The resulting $I_L(t)$ waveform is shown as the dashed curve in Fig. 2. Since $SR_{H\text{-}L}$ is much higher than $SR_{H\text{-}L\_con}$, the time required for $I_L(t)$ to reach the new steady-state value is shorter than the conventional case, which provides fast transient recovery.

During the recovery period ($t_1 \sim t_2$), the load current is fully supplied by C_{out}. The resulting positive $I_C(t)$ causes V_{out} to drop, thus suppresses further voltage overshoot.

The transient recovery process is terminated at t_2, when the inductor current $I_L(t)$ reaches the new load current I_{load2}. Since I_{load2} equals the current $I_C(t)$ that flows out of the capacitor, and the induced current $I_{S2}(t)$ in the secondary winding of the transformer copies $I_L(t)$, t_2 is simply determined by comparing $I_C(t)$ with $I_{S2}(t)$, as shown in Fig. 1.

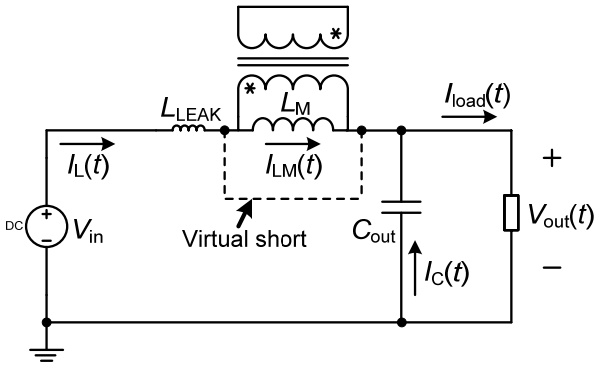

Figure 4. Equivalent circuit during light-to-heavy load transient recovery.

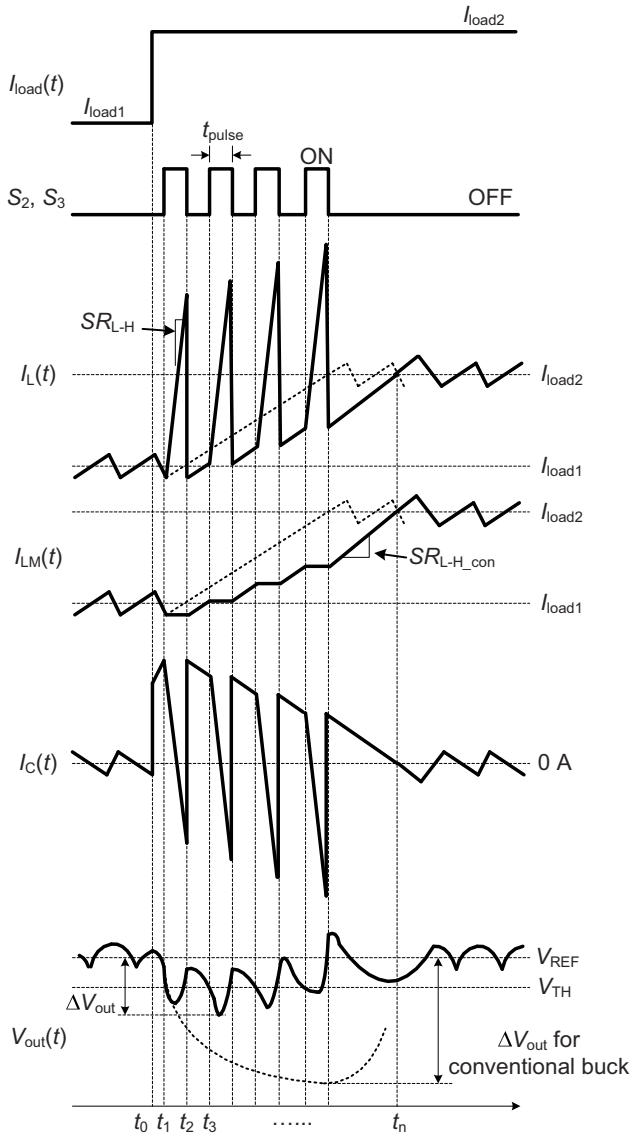

Figure 5. Example current and voltage waveforms during a light-to-heavy load transient recovery process.

C. Light-to-heavy Load Transient

In case of a light-to-heavy load transient, the *HS* transistor and S_0 are kept on and the *LS* transistor is kept off. The voltage across the primary winding is pulled to V_{in}–V_{out}. In the mean time, S_2 and S_3 are switched on to create a short circuit across the secondary winding. The equivalent inductance in the power path is therefore reduced to the leakage inductance L_{LEAK} only, as shown in Fig. 4. Since L_{LEAK} is usually much smaller than the magnetizing inductance L_M, the inductor current $I_L(t)$ ramps up quickly and compensate for the capacitor charges lost due to large load current step [18].

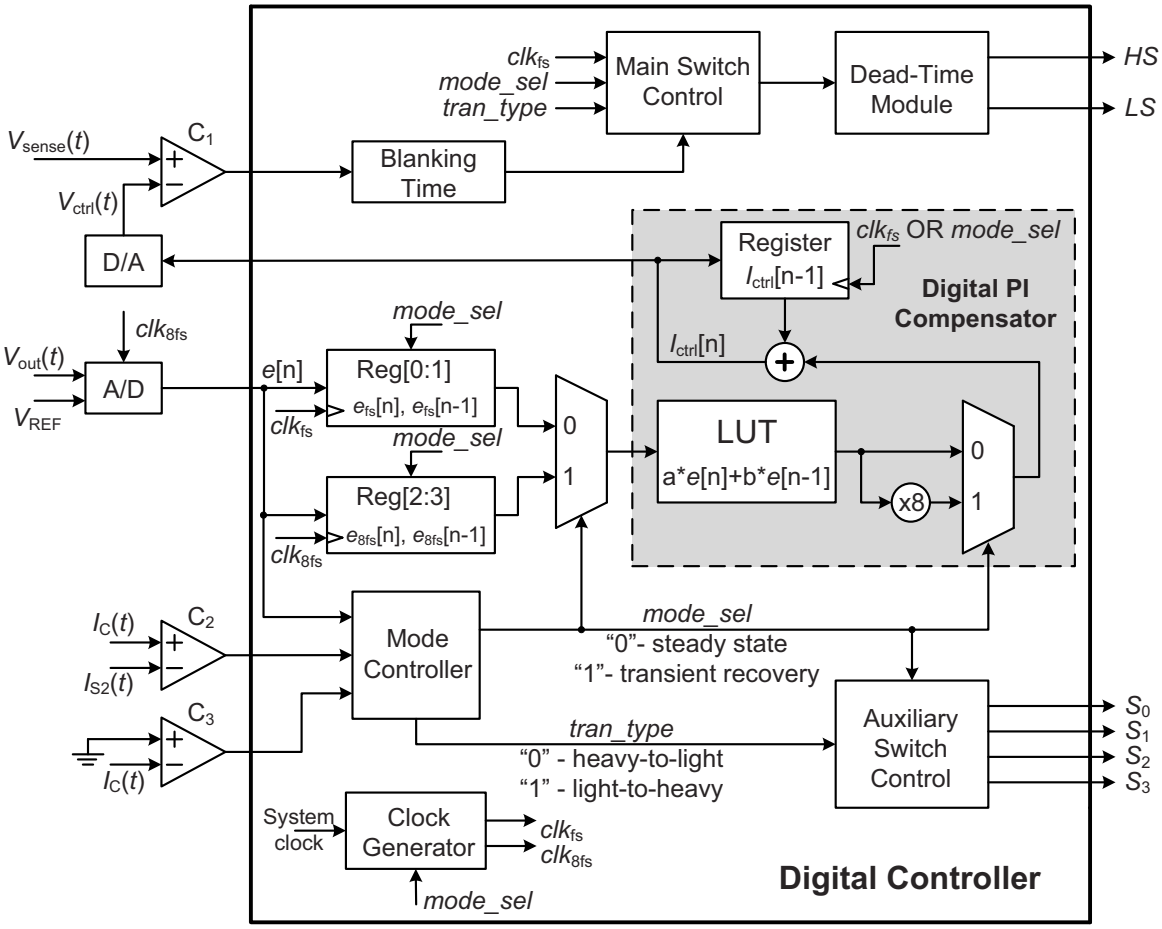

Figure 6. Block diagram of the digital controller.

Theoretical current and voltage waveforms during a light-to-heavy transient recovery process are illustrated in Fig. 5. When the load transient is detected at t_1, both S_2 and S_3 are turned on for a fixed time period t_{pulse}. Inductor current $I_{\text{L}}(t)$ increases with slew-rate $SR_{\text{L-H}}$ determined by

$$SR_{\text{L-H}} = (V_{\text{in}} - V_{\text{out}}) / L_{\text{LEAK}} . \quad (4)$$

This pulsating current suppresses the deviation of $V_{\text{out}}(t)$ during t_1 and t_2. In the meantime, since the voltage across the magnetizing inductor L_{M} is zero, the equivalent current $I_{\text{LM}}(t)$ stays unchanged. At time t_2, when S_2 and S_3 are switched off, the inductor current $I_{\text{L}}(t)$ is dominated by $I_{\text{LM}}(t)$ and starts to rise with slew-rate $SR_{\text{L-H\_con}}$, which is the maximum available current slew-rate for a conventional buck converter under light-to-heavy transient recovery, as expressed in (5).

$$SR_{\text{L-H\_con}} = (V_{\text{in}} - V_{\text{out}}) / (L_{\text{M}} + L_{\text{LEAK}}) \quad (5)$$

Since $I_{\text{L}}(t)$ is still lower than the new load current I_{load2} by the time t_2, $V_{\text{out}}(t)$ starts to drop again until it hits the threshold V_{TH} at t_3 and triggers S_2 and S_3 to turn on for another t_{pulse}. This process repeats until the inductor current $I_{\text{L}}(t)$ equals the new load current I_{load2} and $V_{\text{out}}(t)$ is within the threshold band, as indicated by the time t_{n}. Since the load current is supplied by both $I_{\text{L}}(t)$ and $I_{\text{C}}(t)$ during the recovery period ($t_1 \sim t_{\text{n}}$), t_{n} is the time point when $I_{\text{C}}(t)$ reaches zero while S_2 and S_3 are off.

The inductor current and output voltage waveforms of a conventional buck converter are shown as dashed curves in Fig. 5. In comparison, the proposed method successfully suppresses voltage undershoot but only introduces a small time penalty of one or several short pulses with the length of t_{pulse}.

III. Digital Control Algorithm and Practical Implementation

A digital controller is designed to generate the switching commands during both steady state and the transient suppression process. The top-level block diagram of the digital controller and peripherals are as shown in Fig. 1. The detailed architecture is shown in Fig. 6 and the state diagram in Fig. 7.

The difference of the output voltage $V_{\text{out}}(t)$ and the reference voltage V_{REF} is sensed by an analogue-to-digital converter with an oversampling rate 8 times higher than the steady-state switching frequency f_{s}. This over-sampled error

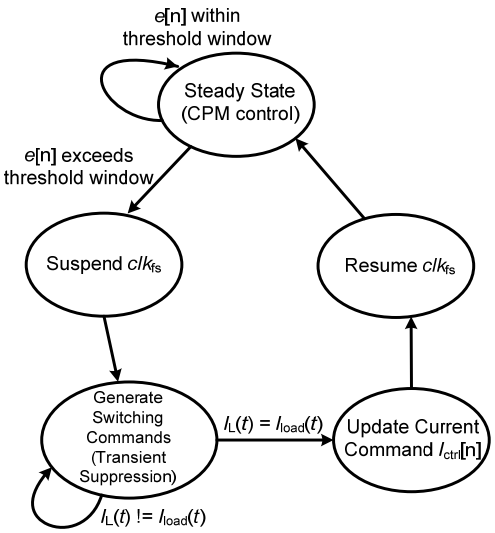

Figure 7. State diagram of the digital controller.

signal e[n] is then monitored by the Mode Controller to determine the operating mode of the converter.

When e[n] is within a pre-determined error threshold window, the converter operates in steady state. Registers Reg[0:1] sample e[n] and e[n-1] at the switching frequency f_s. And the current command I_{ctrl}[n] is generated by a digital PI compensator based on sampled e_{fs}[n], e_{fs}[n-1] and a look-up table (LUT). I_{ctrl}[n] is then sent to a digital-to-analogue converter, whose output $V_{ctrl}(t)$ is compared with the output of inductor current sensor $V_{sense}(t)$ to control the turn-on and turn-off of the *HS* and *LS* transistors.

When e[n] exceeds the error threshold window, the Mode Controller sets the *mode_sel* signal to logic 1 and sets the *tran_type* signal according to the property of the load transient. The converter then enters transient suppression mode while the *HS* and *LS* transistors and the auxiliary switches $S_0 \sim S_3$ are turned on and/or off following the aforementioned algorithm. The Mode Controller continuously monitors the output of comparator C_2 and C_3 to detect the moment when inductor current $I_L(t)$ equals the load current. For heavy-to-light load transients, the recovery process ends when $I_{S2}(t)$ is equal to or less than $I_C(t)$. For light-to-heavy load transient, the recovery process ends when $I_C(t)$ drops to zero during the time when switches S_2 and S_3 are off.

Under transient suppression mode, clock signal clk_{fs} is suspended. Registers Reg[0:1] are reset and registers Reg[2:3] are put on hold. The output of the PI compensator I_{ctrl}[n] is updated based on the over-sampled error signals e_{8fs}[n] and e_{8fs}[n-1], which are stored in registers Reg[2:3] right before the converter starts transient recovery. The gain of PI compensator is temporarily increased so that the resulting I_{ctrl}[n] is approximately equal to the steady-state current command under new load condition. When the Mode Controller detects the end of recovery process and pulls *mode_sel* to logic 0, clock signal clk_{fs} resumes. The gain of PI compensator is reset to normal and the controller

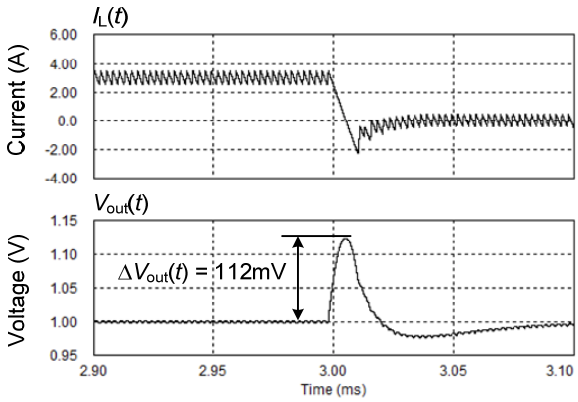

Figure 8. Simulation waveforms of a conventional buck converter under a 3A-to-0A load current transient.

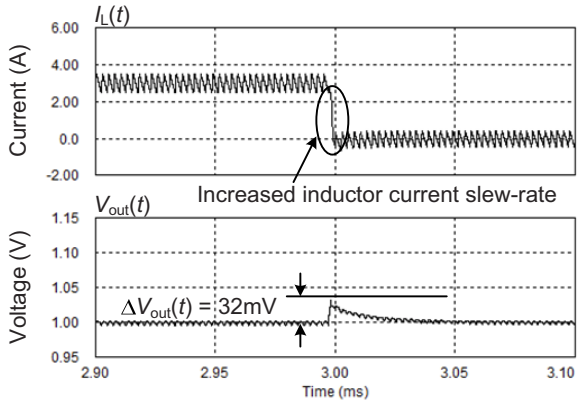

Figure 9. Simulation waveforms of the proposed buck converter under a 3A-to-0A load current transient.

starts operating with the updated I_{ctrl}[n]. Thus a seamless mode transition is achieved.

IV. Simulation and Experimental Results

The functionality of the proposed digitally controlled buck with flyback transformer is confirmed both through simulations and with an experimental prototype. The simulations are performed with PSIM.

The simulated converter operates with 6V input and generates a fixed output of 1V. The flyback transformer is realized using the model described in section II, where the magnetizing inductance is set to be 2.2μH and the leakage inductance 0.2μH. The output capacitor of the converter is 100μF with ESR of 1mΩ. In steady state, the switching frequency is 390kHz.

Fig. 8 and Fig. 9 compare the inductor current and output voltage waveforms of a conventional current-programmed mode (CPM) buck converter and that of the proposed converter during a heavy-to-light load transient. The conventional buck converter recovers the inductor current within one switching cycle and achieves minimum possible voltage deviation for the given topology [8]. The threshold

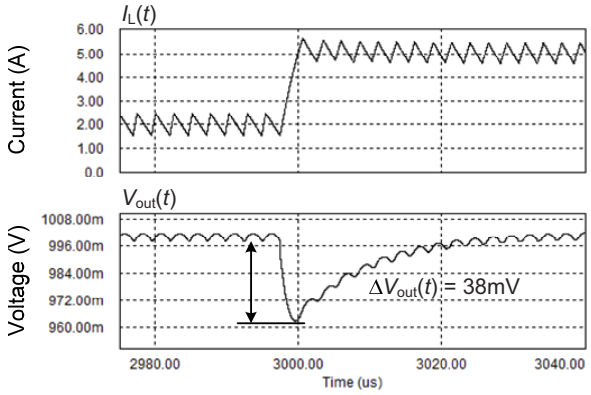

Figure 10. Simulation waveforms of a conventional buck converter under a 2A-to-5A load current transient.

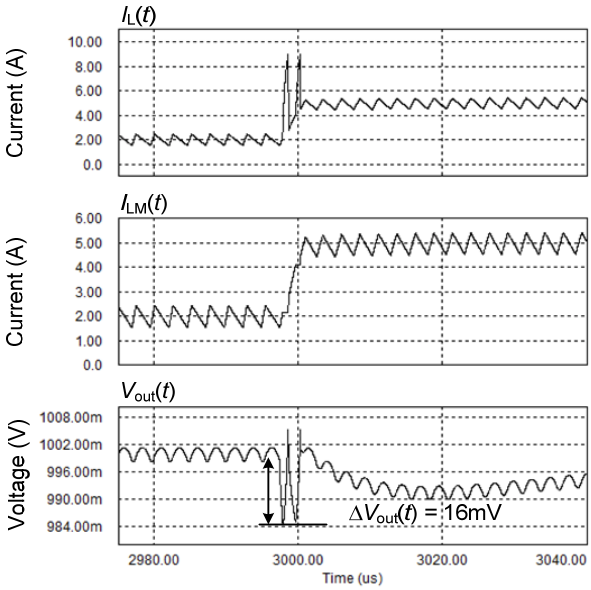

Figure 11. Simulation waveforms of the proposed buck converter under a 2A-to-5A load current transient.

voltage for the proposed converter to enter transient suppression mode is set to be V_{out}+30mV. As can be observed, with higher inductor current slew-rate compared to that of the conventional buck converter, the output voltage deviation of the proposed converter is reduced from 112mV to 32mV. The time required for $V_{out}(t)$ to return to steady-state is reduced by over 50%.

Fig. 10 and Fig. 11 demonstrate the inductor current and output voltage waveforms of a conventional current-programmed mode (CPM) buck converter and that of the proposed converter during a light-to-heavy load transient. The equivalent current of magnetizing inductor L_M is also illustrated. The threshold voltage for the proposed converter to enter transient suppression mode is set to be V_{out}–15mV. t_{pulse} is arbitrarily selected to be 160ns. As can be observed in Fig. 10, the pulsating current suppresses the deviation of V_{out} from 38mV to 16mV and the inductor current $I_L(t)$

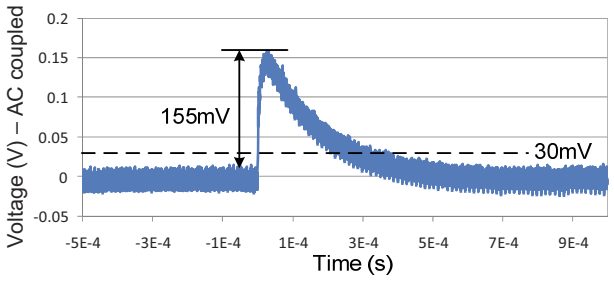

Figure 12. Measured output voltage waveform under 2.5A-to-0.5A load step with transient suppression circuit disabled.

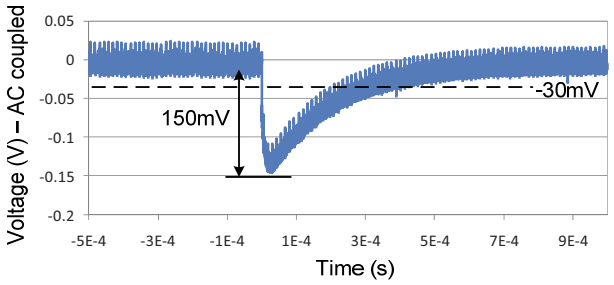

Figure 13. Measured output voltage waveform under 0.5A-to-2.5A load step with transient suppression circuit disabled.

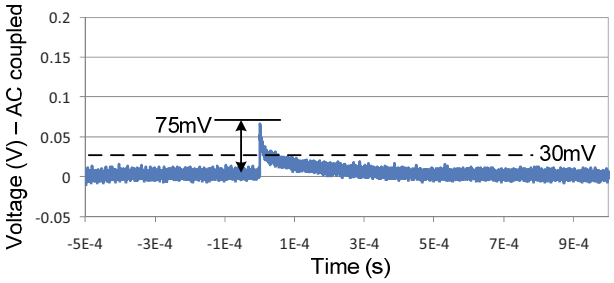

Figure 14. Measured output voltage waveform under 2.5A-to-0.5A load step with transient suppression circuit enabled.

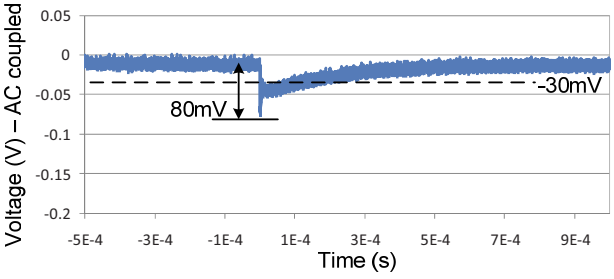

Figure 15. Measured output voltage waveform under 0.5A-to-2.5A load step with transient suppression circuit enabled.

reaches the steady-state value within approximately the same time as the conventional buck.

A prototype buck converter is implemented using discrete off-the-shelf components. The design parameters

TABLE I. SUMMARY OF DESIGN PARAMETERS

Parameter	Value
V_{in}	6 V
V_{out}	1 V
I_{out}	Max. 3 A
$L_{winding}$	2.4 µH
L_{LEAK}	Approx. 0.2 µH
C_{out}	200 µF
ESR	Approx. 20 mΩ
Switching Frequency	390 kHz
ΔI_{out}	Switch between 2.5 A and 0.5 A

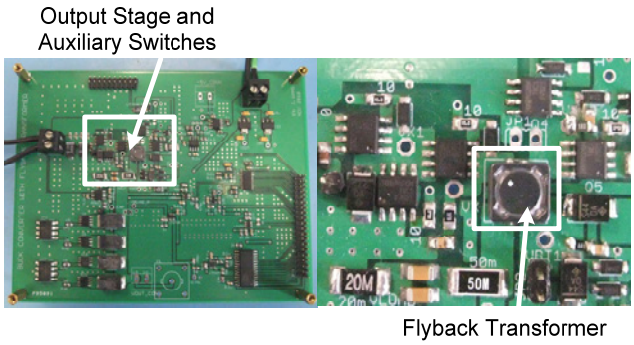

Figure 16. Prototype buck converter with a flyback transformer (left) and close-up picture of the output stage (right).

are as summarized in Table I. An FPGA development board is used to create the digital controller.

Transient performance of the buck converter is firstly examined with the transient suppression circuit disabled. The converter operates only in peak current-programmed mode (CPM) governed by a PI compensator. The control loop bandwidth is designed to be 1/10th of the switching frequency. The transient voltage waveforms are shown in Fig. 12 and Fig. 13.

Fig. 14 and Fig. 15 demonstrate the transient output voltage waveforms when the transient suppression circuit is enabled. The threshold voltages for the converter to enter transient suppression mode are set to be V_{out}+30mV for heavy-to-light load transient and V_{out}–30mV for light-to-heavy load transient. About 50% reduction in peak voltage deviation is observed. And the time required for the output voltage to return to within the threshold window is largely shortened.

Picture of the prototype buck converter is shown in Fig. 16. The rated current of the flyback transformer is 4.2A per winding. Its footprint is approximately 7.5mm×7.5mm, which is comparable to the size of a conventional inductor with the same current rating.

In this prototype, the power switches *HS*, *LS* and auxiliary switches S_0 ~ S_3 are implemented with the same type of NMOS transistors. However, since the auxiliary switches S_1 ~ S_3 are not in the main power conduction path and only need to handle occasional current pulses, higher on-resistances are acceptable without degrading the overall efficiency. As a result, the size of these switches can be minimized as long as it can handle the peak current. The total area occupied by the converter can be further reduced if all the switches are integrated in the same package so that some of the PCB routing can be realized on silicon to achieve miniaturization.

V. CONCLUSIONS

A digitally controlled buck converter with a flyback transformer is introduced. The converter operates in peak current-programmed mode (CPM) in steady state. During load transient recovery, current slew-rate of the power inductor is boosted to suppress voltage overshoot and undershoot with the help of the secondary winding of the flyback transformer and several small auxiliary switches. Since the auxiliary switches are not in the main power conduction path and only need to handle temporary current pulses, their sizes can be minimized. A 6V-to-1V, 3W prototype converter was built with discrete components. Experimental results show a 50% reduction in peak voltage deviation for both heavy-to-light and light-to-heavy load transient cases compared to a conventional current-programmed mode (CPM) buck converter. The proposed architecture achieves same level of transient response improvement with half the size of inductive component compared to the buck converter with an auxiliary stage for transient suppression [13].

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