HIGH-FREQUENCY DIGITAL CONTROLLER IC FOR DC/DC CONVERTERS

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Abstract – **This paper describes a complete digital controller IC for high-frequency switching converters. Novel architecture and configurations of the key building blocks: A/D converter, compensator and digital pulse-width modulator, are introduced to meet the requirements of tight output voltage regulation, high-speed dynamic response, and programmability without external passive components. The implementation techniques are experimentally verified on a prototype chip that takes less than $1\ mm^2$ of silicon area in a standard 0.5μ digital CMOS process and operates at the switching frequency of 1 MHz.**

1 Introduction

Digital controllers could be very attractive in high-frequency, low-to-medium power DC-DC converters because of the inherently lower sensitivity to process and parameter variations, programmability, reduction or elimination of passive components for tuning, and ease of integration with digital systems [1]-[3]. With programmability of compensator and protection features without passive components for tuning the same controller hardware could be used with a range of power converter configurations and power-stage parameter values. In addition, with digital controller implementation, it is possible to implement control schemes that are considered impractical for analog realizations. For example, the ability to precisely match phase-shifted duty ratios has been applied to a simple, robust control for voltage-regulator modules (VRMs) using a dedicated digital controller IC [4, 5]. In transformer-isolated DC-DC converters, digital signal transmission through the isolation can be used to address limited bandwidth and/or large gain variations associated with standard analog approaches. In general, more sophisticated control methods could be used to achieve improved dynamic responses.

From the standpoint of the controller IC design, the main advantages of the digital approach are that the well-established and automated digital design approaches can be applied. The design is described at the functional level using a hardware description language (HDL). From HDL description, synthesis, simulation and verification tools are available to target the design to implementation to standard-cell ASICs or FPGAs. The design can then be easily moved to a

This work was supported by National Semiconductor Corporation through Colorado Power Electronics Center. The authors would like to thank Neal Horovitz and Mike Tamburrino for valuable assistance, and National Semiconductor Corp. for fabricating the prototype chip.

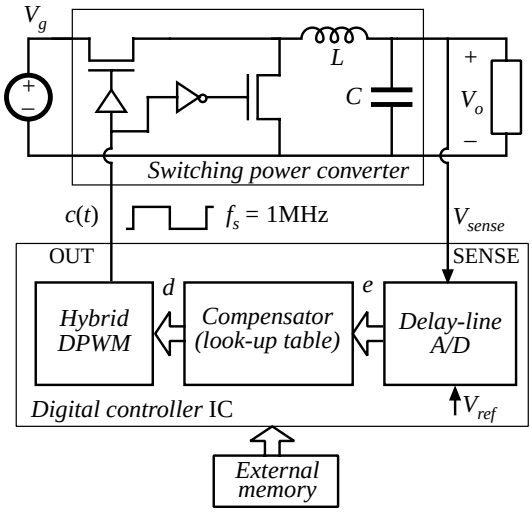

Figure 1: Block diagram of the digital PWM controller IC for a DC-DC switching converter.

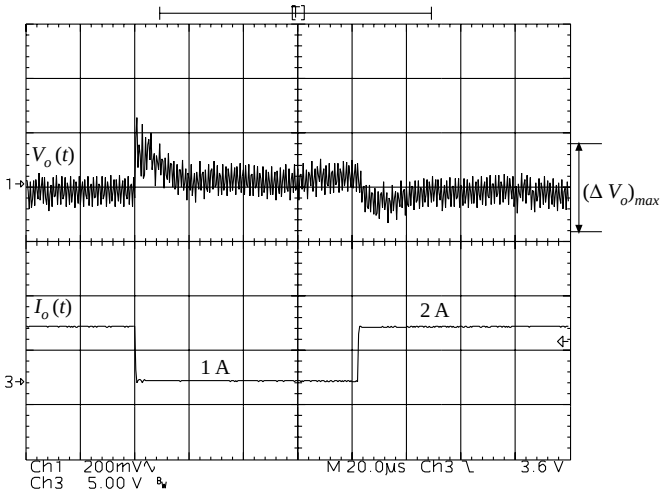

Figure 2: Experimental 50-to-100% load transient response for the closed-loop voltage regulator of Fig. 1: $V_g = 5$ V, $V_o = 2.7$ V, $L = 1\mu$H, $C = 100\mu$F, $f_s = 1$MHz.

different process, integrated with other digital systems, or modified to meet a new set of specifications. In contrast to analog IC controller realizations, the digital controller design can scale well, and can thus take advantage of advances in fabrication technologies.

In spite of the apparent potential benefits, broader acceptance of digital techniques in high-frequency low-to-medium power DC-DC applications is still hampered by a combination of issues including cost/performance, availability, and/or ease of use. Available DSP systems or micro-controllers either lack the performance to even match what is readily available with standard analog controller ICs, or are exceedingly complex for the given application.

The purpose of this paper is to describe implementation techniques aimed at constructing complete, programmable digital controller ICs capable of operating at high switching frequencies (in the 100KHz to MHz range) and having silicon area, power consumption and complexity comparable to or lower than standard analog ICs. The block diagram of the digital PWM controller IC around a synchronous buck converter is shown in Fig. 1 [9]. The IC implements the constant-frequency PWM control by (1) sampling the output voltage using a novel delay-line A/D converter, (2) processing the error signal through a programmable digital compensator based on look-up tables, and (3) generating a constant-frequency PWM waveform to control the power switches using a hybrid digital pulse-width modulator (DPWM). Figure 2 shows an experimental load transient response obtained with this closed-loop voltage regulator.

The paper is organized as follows: the controller architecture is described in Section 2. Architecture and realization of the hybrid DPWM are described in Section 3, together with experimental results obtained from the fabricated prototype chip. The delay-line A/D converter and experimental results illustrating its operation are presented in Section 4. The controller design and additional experimental results obtained with the buck voltage regulator are summarized in Section 5.

2 Digital Controller Architecture

The power converter and the controller form a closed-loop feedback system, the purpose of which is typically to regulate the output voltage V_o to match a precise, stable voltage reference V_{ref} (or a scaled version of the reference) over a range of input voltage values and load currents, and over a range of process and temperature variations. In the basic voltage-mode PWM control method, the output voltage is sensed and compared to the reference. The error signal is passed to the compensator (i.e. the "error amplifier"). The output of the compensator is the input to the pulse-width modulator, which in turn produces the constant-frequency variable duty-ratio signal to control the switching power transistors. The proposed digital controller architecture to implement this control scheme is shown in Fig. 3.

In general, the sensed voltage is a scaled version of the output voltage, $V_{sense} = HV_o$, but in this paper we assume that $H = 1$. The output voltage is sampled by an A/D converter, to produce the digital error signal $e(n)$. The sampling occurs once per switching period T_s. Here, the index n refers to the current switching period. To justify the A/D conversion characteristic shown in Fig. 3, it is useful to examine typical voltage regulation requirements. The dynamic voltage regulation requirement implies that the output voltage $V_o(t)$ must always (including load or input voltage transients) stay in a specified range around the reference V_{ref}, from $V_{ref} - (\Delta V_o)_{max}/2$ to $V_{ref} + (\Delta V_o)_{max}/2$. In addition, the static voltage requirement usually means that in steady state the DC output voltage must equal the reference voltage, with some allowed tolerance, $V_o = V_{ref} \pm \Delta V_o/2$. To meet these requirements, we conclude that the analog equivalent of the least significant bit (LSB) in the A/D characteristic must not be greater than the specified ΔV_o, but also that the conversion range must include only a relatively small range $(\Delta V_o)_{max}$ of voltages around the reference. In practice, the specifications for ΔV_o and $(\Delta V_o)_{max}$ are such that only a few digital values are needed to represent the values of the error signal $V_{ref} - V_o$. In the configuration of Fig. 3, the digital representation of the error signal takes one of only nine possible values, from -4 to $+4$ (decimal). In general, although the A/D converter must have a fine voltage resolution to maintain the ability to regulate the output voltage precisely, only a few bits are needed to represent the digital error signal $e(n)$. A flash A/D converter that meets these requirements has been proposed in [5]. A novel delay-line A/D configuration that takes advantage of the required static A/D characteristic, and lends itself to a simple digital implementation is described in Section 4.

In addition to relaxing the requirements for the A/D converter itself, the fact that the error signal can be represented with only a few bits leads to a simpler implementation of the next building block – the compensator. The purpose of the compensator is to take the current ($e(n)$) and previous ($e(n-1)$, $e(n-2)$, etc.) samples of the error signal and compute the new value of the duty ratio d, which is the variable that controls the power converter through the pulse-width modulator. The computation (i.e. the control law) in the compensator can be designed according to digital control theory well described in literature (see [8], for example). However, standard implementation of linear control laws in the compensator requires digital adder(s) and digital multiplier(s), which increases the area and/or the clock frequency requirements in a practical chip implementation. Taking advantage of the fact that only a few bits are used to represent the error signal e, we instead implement the computation using look-up tables and an adder, as shown in Fig. 3. The current and the previous values of the digital error signal serve as address(es) to read the corresponding location(s) in the look-up tables. Since the error signal e can take only a few different values, the number of entries in the look-up tables is relatively small, and as a result the implementation area is also small. In addition, the computation can be done in a single or in a few clock periods, so that the clock frequency requirements are also low. Details of the compensator implementation on the prototype test chip can be found in [9].

The look-up table compensator can be programmed to perform different control laws simply by programming the entries in the look-up tables. The most general control law supported by the configuration shown in Fig. 3 is given by:

$$d(n+1) = d(n) + \alpha(e(n)) + \beta(e(n-1)) + \gamma(e(n-2)) \quad (1)$$

where $\alpha(\cdot)$, $\beta(\cdot)$ and $\gamma(\cdot)$ are linear or nonlinear functions of the digital error signal. A variety of control laws can be implemented. For example,

$$d(n+1) = d(n) + ae(n) + be(n-1) + ce(n-2)\,, \quad (2)$$

where a, b, and c are constants, corresponds to the basic PID control law. In the controller design, once the coefficients a, b and c are selected (to achieve a desired closed-loop bandwidth and adequate phase margin, for example), the produces $a \cdot e$, $b \cdot e$, and $c \cdot e$ are precomputed for all possible values of the error e and programmed into the look-up tables from an external memory, as shown in Fig. 3. As

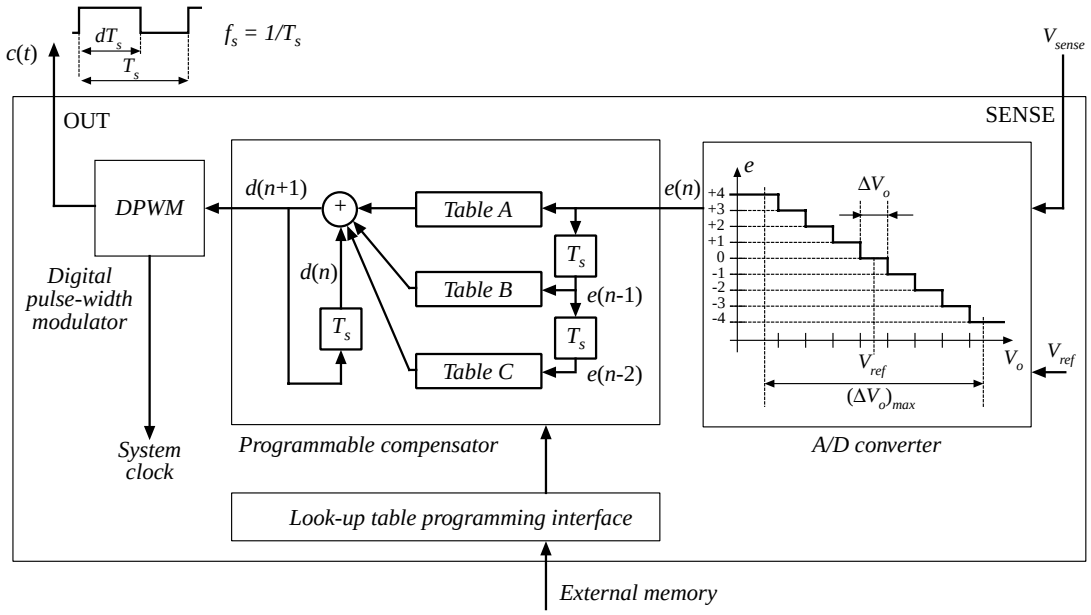

Figure 3: Architecture of the digital PWM controller IC.

alternatives to the external memory, the tables could be easily preprogrammed and hard-wired on the chip at design time, or programmed from other system components via a suitable interface at run time.

The programmable feature of the compensator means that the same controller hardware can be used with different power-stage configurations and different power-stage parameters, without the need for external passive components to tune the compensator response. In addition, using the same configuration, it is possible to explore the use of various nonlinear control laws.

The digital pulse-width modulator (DPWM) completes the controller architecture. The DPWM takes the digital value d of the duty ratio and produces the pulsating waveform $c(t)$ that controls the power transistor(s) in the power converter. A high-resolution, high-frequency DPWM is needed to achieve the required operation at high switching frequency and tight regulation of the output voltage. Our implementation of the DPWM is described in Section 3.

3 Hybrid Digital Pulse-Width Modulator

In the system where a power converter and a digital controller form a feedback loop, the digital pulse-width modulator serves the purpose of a D/A converter. The discrete set of duty ratios and ultimately the discrete set of achievable output voltages depends on the DPWM resolution. If the DPWM resolution is not sufficiently high, an undesirable limit-cycle oscillation can occur [4, 6, 7]. In particular, if none of the achievable output voltages fall into the range of ΔV_o around the reference, in steady state the duty ratio must oscillate through a range of two or more values. A necessary condition to avoid the limit-cycle oscillation is that the output voltage increment that corresponds to the least-significant bit of the duty ratio command d must be smaller than ΔV_o. This condition has been evaluated as a function of the steady-state input and output voltages for different converter configurations [7]. The requirement for a high-resolution, high-frequency DPWM is an important consideration in practical realizations of digitally controlled high-frequency power supplies.

A high-resolution, high-frequency digital pulse-width modulator (DPWM) can be constructed using a fast-clocked counter and a digital comparator [1, 4]. To achieve $n-$bit resolution at the switching frequency f_s, the required clock frequency is $2^n f_s$. This can easily result in more difficult timing constraints, and increased power consumption. For example, an 8-bit resolution at the switching frequency of $f_s = 1$MHz would require a clock frequency of 256MHz. It has been shown that the fine time resolution and much lower power consumption can be achieved using a tapped delay-line scheme similar to a ring oscillator that operates at the switching frequency [2, 5]. However, this implementation requires a larger-area digital multiplexer. The DPWM architecture we selected is based on hybrid delay-line/counter approach [3]. In this approach, an n-bit resolution is achieved using an n_c-bit counter ($n_c < n$), whereas the remaining $n_d = n - n_c$ bits of resolution are obtained from a tapped delay line.

Figure 4 shows a simplified diagram and operating waveforms of the hybrid DPWM, for the case where 4-bit ($n = 4$) resolution is obtained using a 2-bit counter ($n_c = 2$) and a 4-cell ring oscillator ($n_d = 2$, $2^{n_d} = 4$), which consists of resettable flip-flops as delay cells.

At the beginning of a switching cycle, the output SR flip-flop is set, and the DPWM output pulse $c(t)$ goes high. The pulse that propagates through the ring at the frequency $2^{n_c} f_s = 4 f_s$ serves as the clock for the counter. The complete switching period is divided into $2^{n_d} 2^{n_c} = 16$ slots. At the time when the counter output matches the top n_c most significant bits of the digital input (i.e. the duty ratio command) d, and a pulse reaches the tap selected by the n_d least significant bits of d, the output flip-flop is reset and the output pulse goes low. In the example waveforms of Fig. 4, the duty ratio of the output pulse is $11/16$. The basic delay cell in the ring oscillator of Fig. 4 consists of a single resettable flip-flop. The cell delay and the number of cells in the ring determine the switching frequency f_s. To adjust the switching frequency, the cell can be modified by inserting additional delay elements between the flip-flop output and the next cell. The additional delay elements can be standard logic

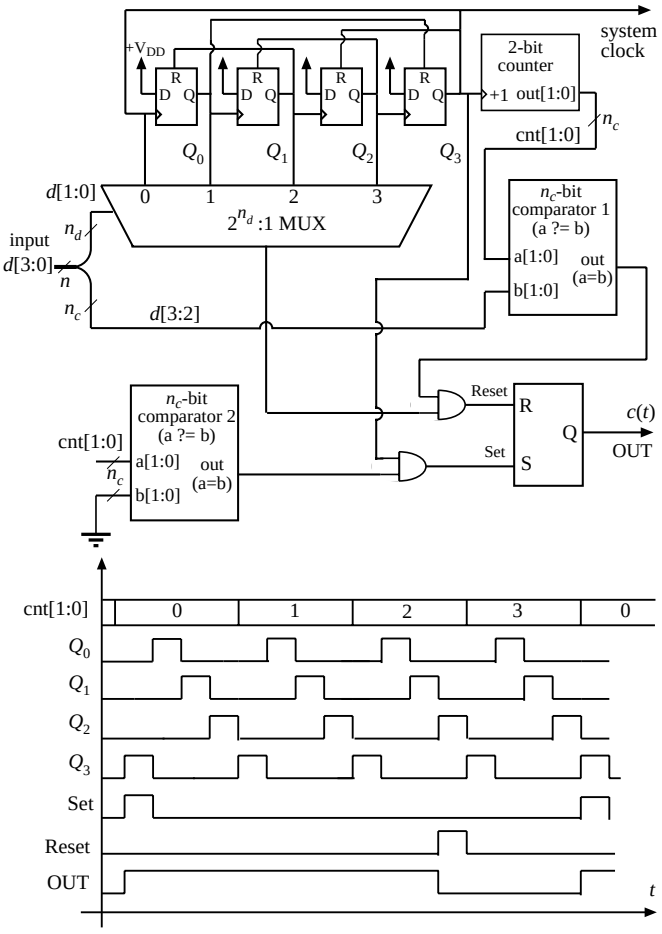

Figure 4: Simplified diagram of the 4-bit hybrid DPWM, together with operating waveforms.

gates, or gates with adjustable delay, if switching frequency tuning or synchronization with an external clock are desired.

The self-oscillating DPWM implementation shown in Fig. 4 has several desirable properties: simple HDL description, even number of time slots in a period, ability to stop and restart the oscillations on command (by gating the propagation of the signal through the ring), and relatively small size.

In the experimental prototype chip, the DPWM was designed for 8-bit resolution ($n = 8$) using a 3-bit counter ($n_c = 3$), and a 32-cell long ring ($n_d = 5$). The DPWM operates at the switching frequency $f_s = 1$ MHz. The ring oscillates at $2^{n_c} f_s = 8$ MHz. This 8 MHz signal is used as the system clock for the entire chip.

Experimental results of Fig. 5 show the measured duty ratio of the output pulses as a function of the 8-bit digital input d. The minimum (3.1%) and the maximum (97.3%) duty ratios are set by design [9].

4 Delay-line Analog-to-Digital Converter

As discussed in Section 2, static and dynamic output voltage regulation capabilities depend on the characteristics of the A/D converter. Conventional high-speed, high-resolution A/D converters consume power and chip area, and require precision analog components. Also, in the switching power supply, the sensed analog voltage V_{sense} comes

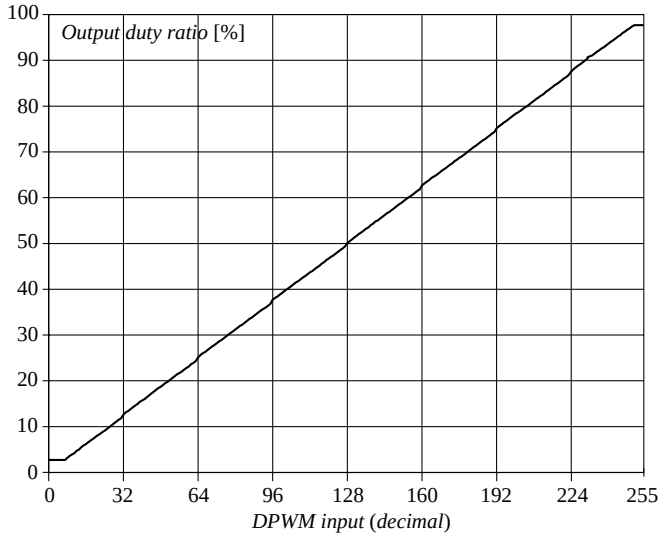

Figure 5: Measured duty ratio of the output pulses as a function of the digital input d for the experimental prototype controller chip.

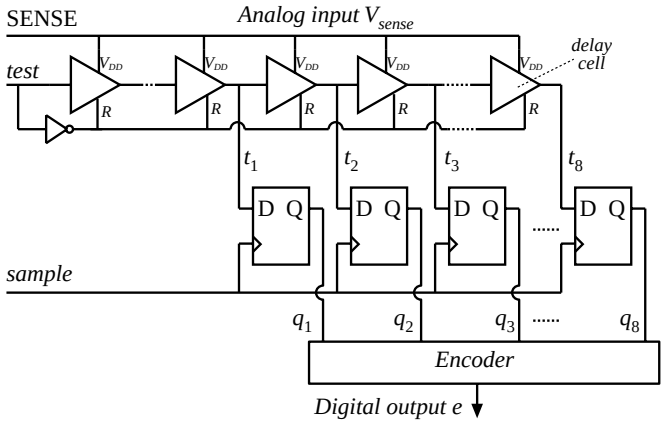

Figure 6: Basic delay-line A/D converter configuration.

from the output of a switching power converter. This signal has large switching noise, which can be a problem for many conventional A/D converters such as the basic flash configuration.

Taking into account the specific requirements discussed in Section 2, we propose a novel delay-line A/D configuration shown in Fig. 6.

The delay-line A/D converter is based on the principle that the propagation delay of a logic gate in a standard CMOS process increases if the gate supply voltage is reduced. To the first order, the propagation delay t_d as a function of the supply voltage V_{DD} is given by [10]:

$$t_d = K \frac{V_{DD}}{(V_{DD} - V_{th})^2}, \qquad (3)$$

where V_{th} is the MOS device threshold voltage, and K is a constant that depends on the device/process parameters, and the capacitive loading of the gate. It can be observed that increasing V_{DD} results in shorter delay. For the supply voltages higher than the threshold V_{th}, the delay is approximately inversely proportional to V_{DD}.

As shown in Fig. 6, a string of delay cells (consisting of logic gates) forms a delay line supplied from the sensed analog voltage,

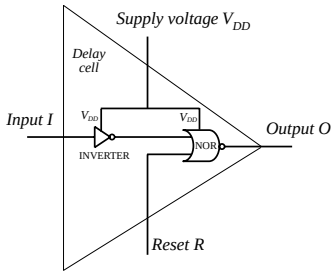

Figure 7: A possible implementation of the delay cell for the delay-line A/D converter.

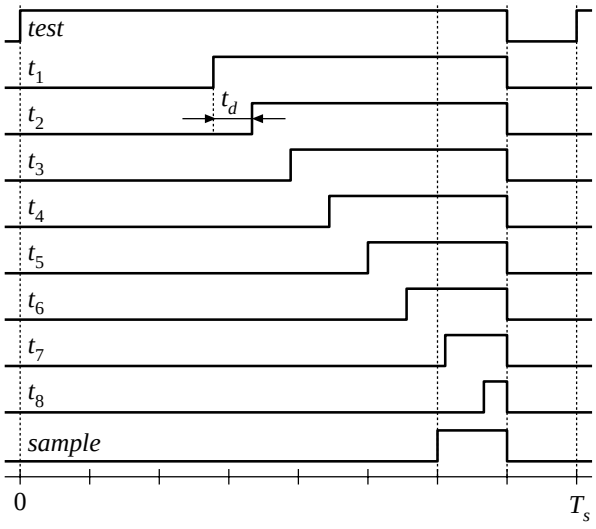

Figure 8: Timing waveforms in the basic delay-line A/D converter.

$V_{DD} = V_{sense}$. Each delay cell has an input, an output, and a reset input R. When the reset input is active high, the cell output is reset to zero. A possible implementation of the delay cell is shown in Fig. 7. To control the cell delay, additional gates can be added to the cell implementation. Also, in the configuration of Fig. 6, the taps do not have to be taken from consecutive cells, giving an additional degree of freedom in designing the A/D conversion characteristic.

Typical timing waveforms in the delay-line A/D converter are shown in Fig. 8. To perform a conversion, at the beginning of a switching cycle, a test pulse *test* is propagated through the delay line. After a fixed conversion-time interval, which is equal to $(6/8)T_s$ in the example waveforms of Fig. 8, the taps (t_1 through t_8) are sampled by the signal *sample*, which is the clock for the D-type flip-flops. The result at the output of the flip-flops (signals q_1 to q_8) is passed to a digital encoder to produce the digital output signal e. The last portion of the switching cycle is used to reset all cells in the delay line, to prepare for the next conversion cycle.

If the analog input voltage (i.e the sensed converter output voltage V_{sense}) is lower, the cell delay t_d is longer, and the test pulse propagates to fewer taps along the delay line. For a higher sensed voltage, the cell delay is shorter and the test pulse propagates further along the delay line. The sampled tap outputs (q_1 to q_8) give the A/D conversion result in the "thermometer" code, similar to the output of the well-known flash A/D converter. For example, for the case illustrated by the waveforms of Fig. 8, the test pulse propagates to the taps t_1 through t_6, but not to the taps t_7 and t_8, so that the flip-flop outputs are $(q_1, q_2, \cdots, q_8) = 11111100$. Ideally, when the sensed voltage V_{sense} equals the reference V_{ref}, the test pulse propagates to the first half of the tapped delay cells. In the delay-line A/D converter of Fig. 6, this zero-error case corresponds to the flip-flop outputs equal to $(q_1, q_2, \cdots, q_8) = 11110000$. The encoder is used to produce the output e in the desired code. The digital output e gives the digital error between the sensed voltage and the reference. The desired steady state operation of the power supply corresponds to the digital error signal equal to zero. Details of the encoding scheme we implemented on the prototype chip can be found in [9].

In the delay-line A/D converter design, the length of the delay line effectively determines the reference value V_{ref} around which the A/D conversion characteristic is centered. The number of taps and the tap delay determine the range $(\Delta V_o)_{max}$ and the effective LSB resolution ΔV_o of the A/D converter. In the experimental prototype chip, the delay-line length and the tap delay were designed (by simulation) to result in $V_{ref} \approx 2.5$V, and $\Delta V_o \approx 40$ mV. Eight taps are used to result in the A/D voltage conversion range $(\Delta V_o)_{max} = (8+1)\Delta V_o \approx$ 360 mV.

A unique advantage of the proposed delay-line A/D converter is that it's basic configuration does not require any precision analog components, and that it can be implemented using standard logic gates. Therefore, it scales well, and can be based on HDL description. Sampling at high switching frequencies (in the range from hundreds of KHz to several MHz) can be easily accomplished in modern submicron CMOS processes. Furthermore, the configuration has a built-in noise immunity: the sampling can extend over a large portion of the switching period over which the input analog signal V_{sense} is effectively averaged. Therefore, the digital output is not affected by sharp noise spikes in the output voltage of a switching converter.

The delay-line A/D conversion characteristic measured on the experimental prototype chip is shown in Fig. 9. The shaded portions of the characteristic indicate the voltages where the output code is flipping between the adjacent values. It can also be observed that the A/D characteristic exhibits some nonlinearity. Most importantly, however, the conversion characteristic is monotonic, and the widths of the code "bins" are approximately equal to the desired ΔV_o value. In a power supply application, the A/D imperfections (code flipping, and nonlinearity) have very little effect on the closed-loop operation. In steady state, the output voltage simply converges to the zero error bin ($e = 0$). On a set of 10 prototype chips, we measured the average of the zero-error bin width to be equal to 53 mV, with a standard deviation of 3.6 mV. The measured reference voltage is $V_{ref} = 2.7$ V, while the measured current consumption of the A/D converter is only about 10μA.

4.1 Calibration of the delay-line A/D converter

The basic delay-line A/D converter results in a reference voltage V_{ref} that is indirectly determined by the length of the delay line and by the delay versus voltage characteristic of the delay cell. In practice, because of process and temperature variations, the reference value obtained by the basic delay-line A/D configuration cannot be precisely controlled. Variations in the effective V_{ref} result in variations of the regulated output voltage, and the power supply may fail to meet the specified static and dynamic voltage regulation. Precise calibration of the delay-line A/D converter against process and temperature variations can be accomplished in a number of ways. One possible approach is to apply a stable, precise V_{ref} (generated using

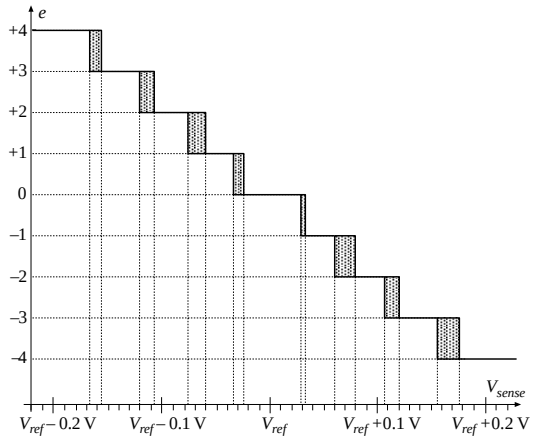

Figure 9: Measured static characteristic of the delay-line A/D converter in the experimental prototype controller IC.

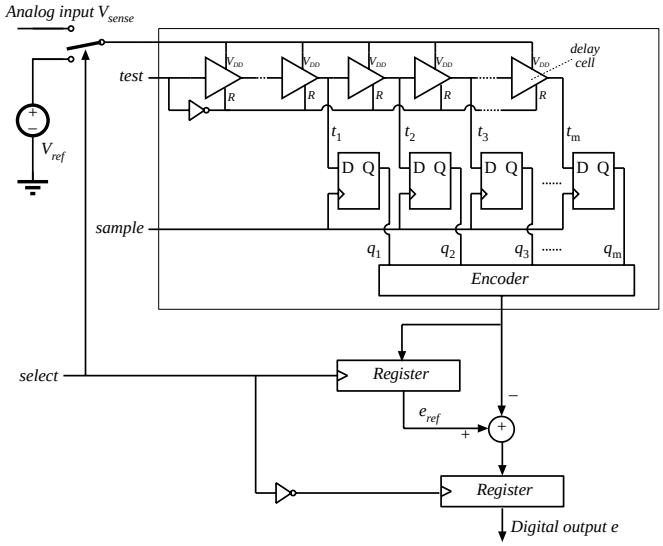

Figure 10: Delay-line A/D converter configuration with digital calibration.

standard bandgap techniques) to the input of the A/D converter, and to subtract (digitally) the conversion result from the value obtained when the actual analog input voltage V_{sense} is applied. The delay-line A/D converter with this digital calibration scheme is shown in Fig. 10, together with possible timing waveforms in Fig. 11.

Two conversions are performed in each switching period. In one half of the switching period, the reference voltage V_{ref} is applied to the A/D converter. The result of the reference conversion e_{ref} is ideally 0, but the actual value can be different because of process and temperature variations. The reference conversion result e_{ref} is stored in a register. In the second part of the period, the input analog voltage V_{sense} is applied to the A/D converter, and the result is subtracted from e_{ref} to obtain the (precisely calibrated) value of the error signal. If desired, the reference conversion for the purpose of calibration of the delay-line A/D converter does not have to be performed in every switching period. Other calibration schemes are possible based on delay-locked loop (DLL) principles.

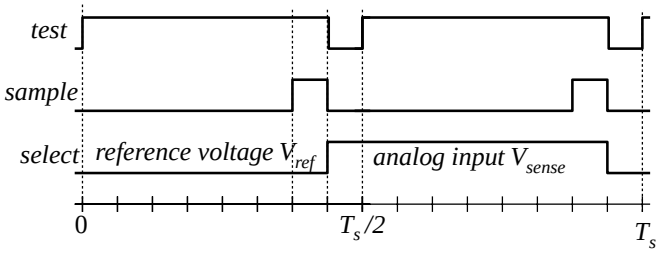

Figure 11: Timing waveforms in the delay-line A/D converter with digital calibration.

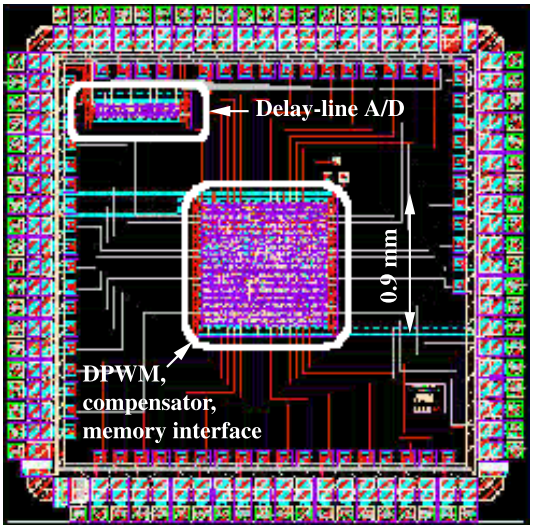

Figure 12: Layout of the prototype chip.

5 Digital Controller Design and Experimental Results

The digital PWM controller described in Sections 2, 3 and 4, was designed and implemented in a standard 0.5μ CMOS process. The chip design was described in Verilog HDL. Synopsys synthesis and timing verification tools were used to reduce the design to standard-cell gates. Digital and mixed-signal simulations were performed using Cadence tools. Given the standard-cell based digital design, the chip layout was automated to large extent using Avanti's place and route tools, and Cadence LVS (layout-versus-schematic) and DRC (design rule check) tools.

The chip layout is shown in Fig. 12. The chip has 84 pins, most of which are used only for test purposes. The only I/O pins essential for operation are OUT, SENSE, the supply and ground, as well as the pins needed to interface with the external memory. Less than $0.2mm^2$ is taken by the delay-line A/D converter. The total active chip area is less than $1mm^2$.

The compensator includes 3 tables (for $e(n)$, $e(n-1)$, and $e(n-2)$). The error signal generated by the delay-line A/D converter can have 9 possible values. The table outputs are 8, 9 and 8-bit values, respectively. Therefore, the total on-chip memory storage is 234 bits. The bit-lengths of the table entries are determined by the range of error signal values (± 4), and by the desired precision of pole-zero placement [7]. The adder produces a 10-bit signed value which is reduced to the 8-bit duty ratio command d by eliminating the sign bit, and by truncating the least significant bit.

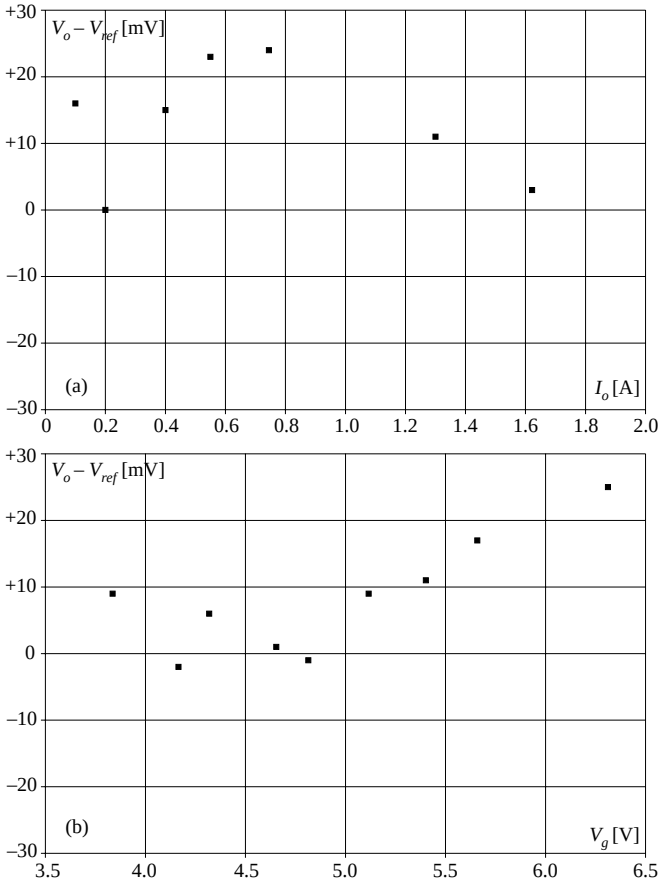

Figure 13: Measured (a) load and (b) line voltage regulation in the closed-loop voltage regulator of Fig. 1.

To demonstrate closed-loop operation, the controller chip is used with a synchronous buck converter as shown in Fig. 1. The input voltage V_g is between 4 V and 6 V, the output voltage is regulated at $V_o = 2.7$V, the load current is from 0 A to 2 A, and the switching frequency is 1 MHz. The filter components are $L = 1\mu$ H and $C = 100\mu$ F. Based on the standard averaged model of the converter [11], the digital compensator was designed using the pole-zero matched method [8], to achieve the loop cross-over frequency of approximately 50 KHz, and a phase margin of about 50^o. When the converter is powered up, it loads the compensator table entries from the external memory, and then starts to sample the output voltage and produce the pulsating waveform $c(t)$.

Experimental $50 - 100\%$ load transient waveforms are shown in Fig. 2. It can be observed that the output voltage stays regulated inside the $(\Delta V_o)_{max}$ range. Measured static load and input voltage regulation results are shown in Fig. 13. The output voltage stays within the zero-error bin of ΔV_o.

6 Conclusions

This paper describes a complete digital controller IC for high-frequency DC-DC switching converters. Novel controller architecture and configurations of the key building blocks: the A/D converter, the compensator and the digital pulse-width modulator (DPWM), are introduced to meet the requirements of high-speed dynamic response, tight output voltage regulation and programmability without external passive components. The DPWM has 8-bit resolution and generates the switching frequency of 1 MHz, and a system clock frequency of 8 MHz. The delay-line A/D converter has 1 MHz sampling rate, a 50 mV resolution, high noise immunity, and a small-size, low-power implementation based on digital logic gates without the need for precision analog components (other than a bandgap reference). The control law is implemented in a small-area, low-power compensator with look-up tables. The table entries are programmable so that the control law can be redesigned for various converter configurations and parameters without the need for external passive components. The complete design is based on hardware description language (HDL) description, and takes advantage of the modern tools for digital ASIC design.

The controller architecture and the implementation techniques are experimentally verified on a prototype IC that takes less than 1 mm^2 of silicon area in a standard 0.5μ digital CMOS process, and operates at the switching frequency of 1 MHz.

References

[1] G. Wei, M. Horowitz, "A low power switching power supply for self-clocked systems," International Symposium on Low Power Electronics and Design, ISLPED 1996.

[2] A. P. Dancy, A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," IEEE PESC 1999.

[3] A. P. Dancy, R. Amirtharajah, A. P. Chandrakasan, "High-efficiency multiple-output DC-DC conversion for low-voltage systems," IEEE Trans. On VLSI Systems, Vol.8, No.3, June 2000.

[4] A. M. Wu, J. Xiao, D. Marković, S. R. Sanders, "Digital PWM Control: Application in Voltage Regulator Models," IEEE PESC 1999, pp. 77-83.

[5] J. Xiao, A. V. Peterchev, S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," IEEE PESC 2001, pp. 38-47.

[6] A. V. Peterchev, S. R. Sanders, "Quantization resolution and limit cycle in digitally controlled PWM converters," IEEE PESC 2001, pp. 465-471.

[7] A. Prodić, D. Maksimović, R. Erickson, "Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter," IEEE IECON 2001.

[8] G. F. Franklin and J. D. Powell, *Digital Control of Dynamic Systems*, Addison-Wesley Publishing Company, Inc: 1998.

[9] B. J. Patella, *Implementation of a High Frequency, Low-Power Digital Pulse Width Modulation Controller Chip*, M.S. Thesis, University of Colorado, Boulder, December 2000.

[10] A. Bellaouar, M. I. Elmasry, *Low-Voltage Low-Power VLSI CMOS Circuit Design*, Kluwer Academic Publishers: 1996. (pp. 124-129).

[11] R. W. Erickson, D. Maksimović, *Fundamentals of Power Electronics*, 2^{nd} edition, Kluwer Academic Publishers: 2000.