PROGRAMMABLE-OUTPUT PFC RECTIFIER WITH DYNAMIC EFFICIENCY AND TRANSIENT RESPONSE OPTIMIZATION

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Abstract—This paper introduces a digitally-controlled 2-stage single-phase rectifier with power factor correction (PFC) that is well suited for emerging low-power applications requiring programmable supply voltage. The rectifier is a modification of a flyback-buck cascaded configuration where the intermediate energy storage capacitor is replaced by a non-symmetric capacitive divider with independent control of tap voltages. The voltages are dynamically controlled through a single secondary winding, such that the optimized efficiency and reduced size of the downstream stage are achieved without sacrificing dynamic response. Results obtained with a 30W universal-input experimental prototype confirm fast transient response during efficiency optimization, operation with a near unity power factor, and about a 50% reduction in the flyback capacitor value, as compared to single-stage solutions.

I. INTRODUCTION

Single-phase rectifiers with power factor correction (PFC) providing power up to approximately 100 W are widely used as chargers for mobile devices or dedicated supplies. The applications include personal computers, consumer electronics, telecommunication devices, and avionics equipments. In addition to providing close to unity power factor (PF) and low total harmonic distortion (THD), emerging standards and applications also require programmable output voltage. For example, the IEEE-UPAMD standard [1], which defines a connection between a charger (adapter) and supplied mobile device, defines a communication link that sets up required output voltage level as well as voltage transition times. Similarly, in adaptive voltage bus system [2], a programmable dc bus voltage is changed quickly based on the load requirements.

A number of single-phase ac-dc solutions with power factor correction have been proposed [3-7]. Generally, they can be divided into single [8-11] and two-stage [12] systems. In a typical low power application, where the cost is a dominant factor, single stage solutions employing a flyback converter [13] are frequently used. This is mostly due to the controller and system simplicity as well as due to the existence of galvanic isolation. However, these systems usually suffer from voltage regulation problems [14] and require a bulky output capacitor to compensate for low frequency line harmonics in the output voltage [15]. More complex two-stage solutions have better voltage regulation [12]. There, the first stage provides ac-dc rectification and the second dc-dc step-down stage keeps the output voltage well regulated [12]. In these systems, the intermediate voltage between the two stages is usually selected based on output voltage and design tradeoffs between the converter efficiency and dynamic response [16]. In general, by reducing the difference between the input and output voltages the efficiency of the downstream stage can be improved. However, this improvement comes at the expense of the dynamic response and, consequently larger output capacitance value. In the ac-dc applications with programmable output voltage that require fast transient response this tradeoff is a serious concern.

The primary objective of this paper is to present the simple flyback-based two-stage solution of Fig.1 that is well suited for emerging ac-dc applications requiring programmable output voltage. The converter operates with a relatively small flyback capacitor, has tight output voltage regulation, and provides fast transient response while operating at the optimized efficiency point.

The following section provides the system description and explains the principle of operation of the proposed converter architecture. Practical implementation is discussed in Section

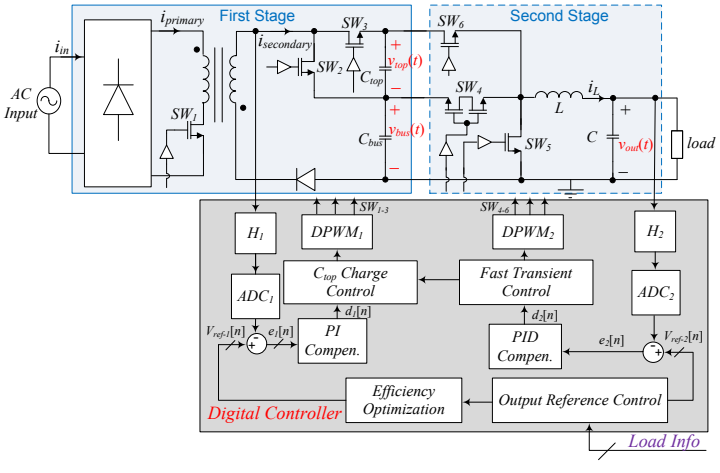

Fig.1: Programmable-output PFC rectifier and complementary digital controller.

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III and Section IV presents experimental results verifying the proper operation of the implemented power supply.

II. System Description and Principle of Operation

The system of Fig.1 is a 2-stage converter, where the first stage is a modified flyback and the second stage is a conventional buck with an extra switch, SW_6. The flyback is modified such that the output capacitor is replaced with a non-symmetric capacitive divider of a smaller equivalent capacitance, where the voltages of the two capacitors are independently regulated. The divider centre tap voltage $v_{bus}(t)$, i.e. bus voltage, is the input of the buck during regular steady-state operation. This voltage is allowed to have relatively large ripple at twice the line frequency, to minimize the capacitor (C_{bus}). As described below, the dc value of the bus voltage is dynamically adjusted, based on the desired output voltage level, such that the efficiency is maximized. The top capacitor of the divider is used during transients to improve the dynamic response, i.e. to step up inductor current slew rate. Both stages are regulated with a digital controller that has two interactive control loops. The front-end controller regulates operation of the flyback converter such that close to unity factor is achieved and, at the same time, regulates the average values of divider tap voltages, based on information from *efficiency optimization* block. The controller of the buck provides tight output voltage regulation and fast dynamic response. During transients the buck controller employs a minimum deviation control algorithm [17], recovering the current in a single on-off switching cycle with the minimum possible output voltage deviation.

A. Programmable Intermediate Bus Voltage for Efficiency Optimization

The efficiency of 2-stage converters with a wide range of operating conditions can be optimized by changing the voltage difference between the intermediate bus voltage and the output voltage, as demonstrated in [16]. This allows optimizing the converter conduction and switching losses depending on the output power level of the converter. For the optimum efficiency, this results in much lower than maximum intermediate bus voltage, due to significant reduction of switching losses. This reduction of voltage difference reduces component stress on the second stage dc-dc converter and results in a lower inductor ripple, allowing possible reduction of the inductor size [18]. Hence, to optimize the efficiency and at the same time to minimize the value of the buck inductor while maintaining a constant ripple, the intermediate bus voltage is dynamically changed based on the operating condition.

B. Improving Dynamic Performance of the Downstream Stage

The reduction of the input voltage described in the previous subsection optimizes efficiency of the downstream buck stage but, at the same time, degrades dynamic performance. Consequently, the output capacitor is increased. A larger output capacitor is required even though the buck inductor is reduced. This is due to even a larger drop in the inductor current slew rate during light-to-heavy load transients, resulting in slower charging of the output capacitor.

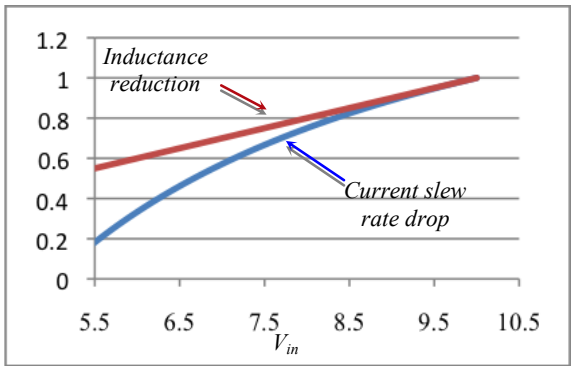

Fig.2: Reduction in inductor size vs. inductor current slew rate for a 5V buck converter which bus voltage changes between 5.5 V and 10 V.

This can be demonstrated by the example depicted in Fig.2 showing maximum possible reduction in the inductance and, for the reduced inductance, the drop in the inductor current slew rate for a 10 V- to - 5 V rated buck converter, as its supply voltage changes between the output and maximum value. The diagrams are obtained from simple equations [19] for the inductor current ripple and current slew rate during a light-to-heavy load transient.

In order to improve transient, a second capacitor, C_{top} of Fig.1, is incorporated. This capacitor is charged at a higher voltage than the bus voltage and used during light-to-heavy load transients, to improve the inductor current slew rate. As described in the following section the average voltage value of this capacitor is regulated independently of the bus voltage, with the modified flyback converter. It should be noted that the value of this capacitor is much smaller than that of C_{bus} (Fig.1) allowing for cost-effective implementation. The low value of C_{top} is possible, since it only provides energy during transients and is not used to supply the difference between the time varying input and constant output power [19]. The following calculation, along with Fig.3, shows how the size of C_{top} is selected to improve the transient response of the second stage.

Charge transferred from C_{top} to output capacitor, C during a Δi step transient can be calculated as:

$$\Delta Q = \frac{1}{2} * T_c * \Delta i \qquad (1)$$

Where T_c is the time to reach the new steady state current value:

$$T_c = \frac{\Delta i}{\frac{Vtop + Vbus - Vout}{L}} \qquad (2)$$

where V_{top} and V_{bus} are the top capacitor and bus capacitor voltages, respectively and V_{out} is the output voltage. L is the value of the inductor. Substituting (2) in (1) we get,

$$\Delta Q = \frac{1}{2}\frac{L\cdot\Delta i^2}{(Vtop+Vbus-Vout)} \qquad (3)$$

Now since the top capacitor, C_{top} is much smaller than C_{bus}, we can assume that the entire voltage drop due to this charge transfer ΔV, occurs across the top capacitor. Hence, the top capacitor value can be calculated as:

$$C_{top} = \frac{1}{2}\cdot\frac{L\cdot\Delta i^2}{(Vtop+Vbus-Vout)\cdot\Delta V} \qquad (4)$$

The large difference in the capacitor values is used to implement practically independent control of the output voltages, as described in the following section.

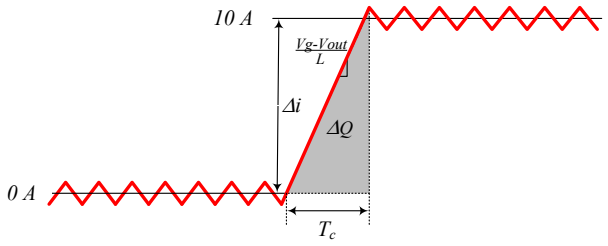

Fig.3: Charge transfer from C_{top} during transients.

III. Practical Implementation

The controller of Fig.1 consists of a PI compensator to regulate the intermediate bus voltage $v_{bus}(t)$ and a fast transient controller, incorporated with a PID compensator, to regulate the output voltage $v_{out}(t)$. Two analog-to-digital converters (ADC) are utilized to sample the outputs of the two stages and to compare them with the corresponding references. The load information, which can be obtained through inductor current measurement, estimation [20], or directly from the load, sets the reference for the bus voltage based on the load requirement. The reference for the bus voltage is selected such that optimum efficiency is achieved for the given operating condition. For achieving a high power factor, the flyback converter is operated at the boundary conduction mode (BCM), similar to the system presented in [21]. As shown there, the BCM operation minimizes current stress and results in a relatively low electromagnetic interference. Fig.4 shows the current waveforms on the primary side ($i_{primary}$), secondary side ($i_{secondary}$) and the input current (i_{in}). As explained in the following subsection, ADC_1 is utilized in controlling both voltages of the capacitive divider, i.e. the bus voltage, $v_{bus}(t)$ and the voltage across C_{top} capacitor, $v_{top}(t)$. The fast transient control block utilizes charge stored at C_{top} by momentarily turning on SW_6 during transients, to improve the inductor current slew rate in the second stage.

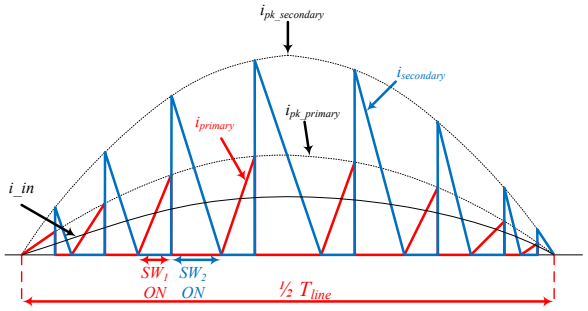

Fig.4: Flyback converter boundary conduction mode (BCM) current waveforms.

A. Dual output control through flyback secondary winding

To provide voltages for both taps of the capacitive divider, a flyback transformer with two secondary windings could be used [19]. However such a solution suffers from cross-regulation problem [22] that affects output voltage regulation and might require a custom flyback transformer design. To eliminate these problems and simplify system implementation, a novel simple method for providing two independent voltages

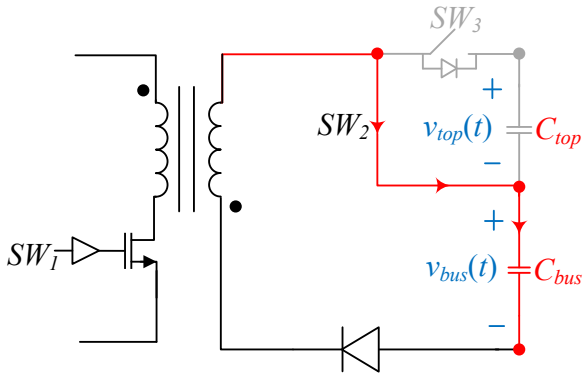

Fig.5: Charging of the bus capacitor.

is developed. Here, both divider taps are controlled from the same secondary winding of the flyback converter. As shown in Fig.5, when SW_2 is on, the secondary winding current (Fig.4) charges the bottom capacitor. During this time the

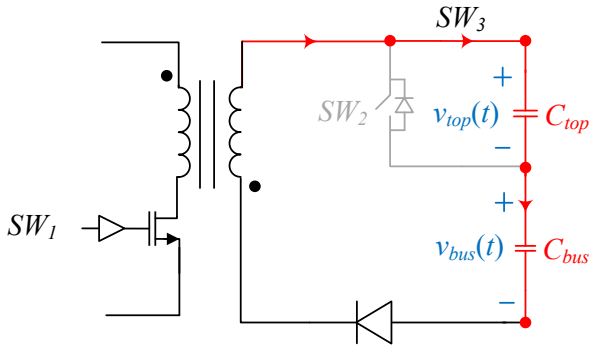

Fig.6: Charging of the top capacitor.

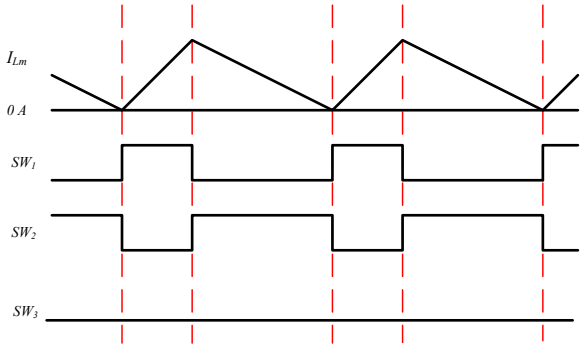

Fig.7: Timing diagram of bus capacitor charging.

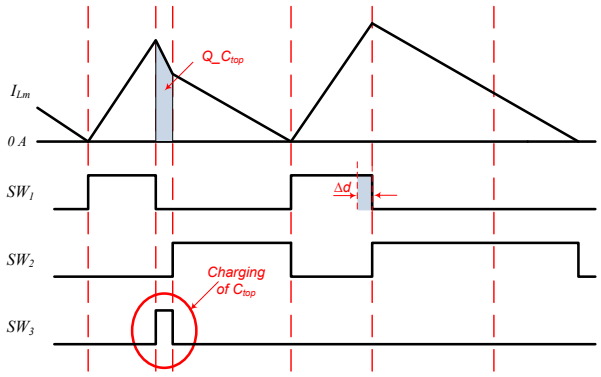

Fig.8: Timing diagram of top capacitor charging.

body diode of SW_3 is reversed biased. In this case ADC_1 samples the voltage stored at the bus capacitor, i.e. $v_{bus}(t)$.

Similarly, as Fig.6 shows, by turning on SW_3 the series connection of both capacitors is charged. In this case the ADC_1 samples the sum of voltages stored across both capacitors. Since as described in the previous section, the top capacitor is much smaller than the bottom one, the voltages across them are not changed equally. The voltage of the smaller, i.e. top, capacitor is primarily affected, practically allowing the two capacitor voltages to be controlled independently. This is performed over a portion of one switching period, as shown in timing diagrams of Figs. 7 and. 8.

Fig.7 shows the conventional operation, i.e. boundary conduction mode, without charging of the top capacitor, where the total inductor current is used to supply the bottom capacitor. Fig.8 illustrates the switching cycle with a portion of the secondary conduction period used to charge up C_{top}. This is shown as charge Q_C_{top} when SW_3 is on. Since a portion of the charge is given to C_{top}, the controller increases the on-time, in the following cycle, for SW_1 (Δd in Fig.7), to maintain steady bus voltage.

B. *Increased Conduction Loss and Light Load Efficiency Improvement*

Compared to a conventional flyback, the proposed first stage converter has an extra switch (SW_2) in the conduction path. However since the switch is rated for half the voltage now, the increase in the conduction loss in minimized. This is due to the fact that the channel length, hence the on resistance, of semiconductor devices is proportional to the component rating [23]. Similarly, addition of SW_6 will now require blocking in both directions for SW_4. As a result, SW_4 needs to be replaced by two switches in series with half the voltage rating, as shown in Fig.1. The size of the SW_3 and SW_6 is significantly smaller compared to other switches, as the rms current through them is much smaller. Furthermore, during light load operation, to improve the efficiency of the converter, only SW_3 and SW_6 can be used to regulate the output voltage.

IV. Experimental System and Results

To verify the operation of the system shown in Fig. 1 an experimental prototype was built. The universal input, 2-stage 30-W ac-dc converter with power factor correction and programmable bus and output voltages was designed. Switching frequency of the first stage varies between 50 kHz and 200 kHz, depending on the operating condition, and the second stage operates with 500 kHz fixed switching frequency.

Figs. 9 and 10 show steady-state operation of the system. The power factor of the input current waveform of Fig.9 is about 0.98 and stays in 0.95 to 0.99 range over all operating conditions.

Fig.10 shows the bus voltage and the output voltage regulations. Even though a 600 µF bus capacitor is used, which is at least 50% smaller than that of the state of the art single phase solutions [15], [24], the output voltage is well-regulated. As mentioned before, this is achieved by allowing bus voltage to contain a relatively high ripple of $1.5V_{p\text{-}p}$ at twice the line frequency. However the output voltage of the converter shows tight regulation with 20mV ripple at 2V output voltage across a 220 µF output capacitor.

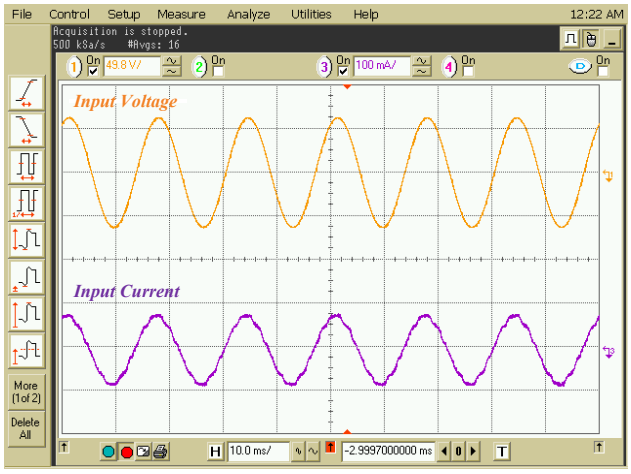

Fig.9: Input voltage and current waveform of the proposed converter– Ch1: input voltage (50V/div); Ch2: input current (100 mA/div).

Fig.11 shows a step voltage change of the top capacitor, to demonstrate independent charging. As the figure illustrates, once the reference for the top capacitor is updated, the top capacitor is charged to 8V (i.e. the sum of bus voltage and top capacitor voltage is increased to 12V) in 150ms without affecting constant 4V across the bus capacitor.

Fig.12 shows the transient response comparison between the introduced converter architecture and a conventional downstream buck stage. For the proposed architecture case, the bus voltage was regulated at 4V, to minimize switching losses of the downstream converter, and the top capacitor was charged to 8V. On the other hand, the conventional buck was operating with a fixed 12V input voltage. As the waveform shows, both result in similar voltage deviations during the transients. In other words, the proposed architecture allows efficiency optimization without sacrificing the transient response. For 2V output and 4V bus voltage the efficiency of the second stage is measured to be 87% for 4A output current, compared to 81% efficiency for 12V fixed bus voltage. In case of lighter loads this improvement is expected to be even larger, due to reduction of more dominant switching losses.

V. CONCLUSIONS

A single-phase rectifier with power factor correction well suited for emerging applications requiring quickly changing programmable voltage is introduced. The 2-stage solution is a modification of a flyback-buck topology where a non-symmetric capacitive divider with practically independent control of two tap voltages is used. The centre tap, i.e. bus voltage, is adaptively regulated such that the efficiency of the downstream stage is optimized. The top capacitor of the divider, with a much smaller value than that of the bottom one, is used to increase current slew rate during transients canceling negative effects of the efficiency optimization. A practically independent regulation of divider voltages is performed with a single secondary winding, eliminating the need for a custom flyback inductor design, as well as cross-regulation problem existing in two winding solutions. The regulation is based on the current steering and utilization of a large difference in the divider capacitance values. Experimental results confirm system advantages and proper operation.

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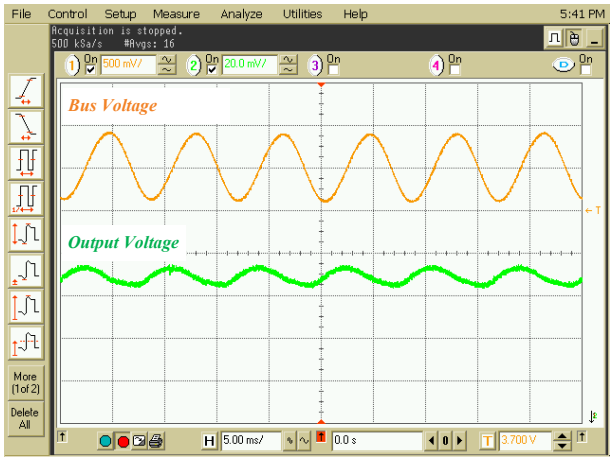

Fig.10: Regulation of bus voltage and output voltage – Ch1: Bus voltage (500mV/div); Ch2: Output voltage (20mV/div).

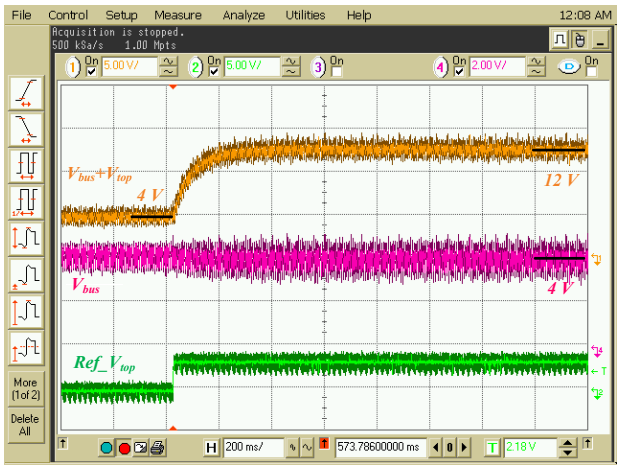

Fig.11: Charging of top capacitor – Ch1: Bus + top cap voltage (5V/div); Ch2: Bus voltage (2V/div);Ch3: Change reference for the top capacitor.

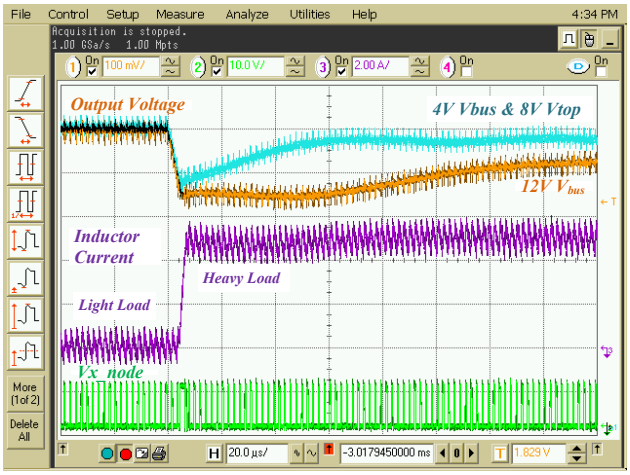

Fig.12: Transient response comparison – Ch1: Programmable v_{bus} and v_{top} (100mV/div); Ch2: Buck with 12V V_{in} (100mV/div); Ch3: Inductor current (2A/div); Ch4: V_x node voltage (10V/div)

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