Digitally Controlled Multi-Phase Buck-Converter with Merged Capacitive Attenuator

Behzad Mahdavikhah, Parth Jain, Aleksandar Prodic
ECE Department University of Toronto, 10 King's College Road,
Toronto, ON, M5S 3G4, CANADA

***Abstract*— This paper introduces a new topology that combines a capacitive divider and an interleaved buck to reduce the volume of multi-phase step-down converters. The size reduction is obtained with a low penalty in conduction losses, input filter size, and controller complexity. At heavy loads, the converter efficiency is comparable to that of a conventional buck and at light to medium loads it is improved. The volume reduction is obtained by utilizing the inductors of the buck stage to regulate the tap voltages of the capacitive divider. This eliminates a bulky energy transfer capacitor existing in other switch capacitor (SC) circuits, reduces the number of switches in the conduction path, and simplifies control of the converter.**

Experimental results obtained with a 7V-to-1V, 10A, 1 MHz prototype demonstrate that the merged capacitor converter has 15% smaller inductor, 13% reduction in output capacitor value and up to 35% reduction in power losses, and 15% faster transient response than a time-optimal controlled buck.

I. INTRODUCTION

In portable devices, such as tablet computers and gaming consoles among the main targets are volume reduction of dc-dc converters [1], [2] and improvements in their efficiency. In these systems the reactive components of the power supplies often occupy more than 25% of the overall volume and are among the largest contributors to the overall device weight [3]. Those supplies are usually required to step down the voltage of a single or two serially connected battery cells to a 1V or even lower voltage [4], for digital loads. Due to the quickly changing nature of the load, which often depends on the software application, the supplies are also required to have a high efficiency over the full range of operation and fast dynamic response.

Most of the converters used for the targeted applications are single-stage multi-phase buck topologies [5]. Recent publications [5]-[7] show that a cascade connection of a switch-capacitor (SC) and a buck converter results in a significant increase in power density. Those 2-stage structures result in a significant reduction of the overall volume but at the same price introduce a relatively large number of extra switches in the conduction path. As a consequence, the conduction losses of those topologies are often preventing their use in higher current applications. In addition, the cascaded topologies also use separate controllers for each of the two stages increasing hardware complexity.

The main goal of this paper is to introduce a new merged switch-capacitor multi-phase switch-capacitor buck converter topology shown in Fig.1 that further reduces the volume of the step-down converters with a lower penalty in conduction losses compared to other 2-stage solutions [5]-[7]. At heavy loads, the proposed structure has approximately the same efficiency as the conventional interleaved buck and at light to medium loads the efficiency is improved. Furthermore, the merged topology has a larger inductor current slew rate resulting in a significantly faster transient response. This converter operates on the same principle as the single-phase topology consisting of a capacitive divider and a downstream buck converter introduced in [8]. There the switches of both stages are shared to minimize conduction losses and the buck inductor is used for the capacitor voltage balancing eliminating a bulky intermediate capacitor existing in other SC-based solutions [5]-[7]. An extension of the single-phase system to a multi phase operation is not a straightforward task. Mostly, due to a strong interaction between the upstream and the downstream stage as well as due to the phase interactions. Hence, a simple parallel connection of the buck stages for the topology shown in [8] cannot be used. The multi-phase topology of Fig.1 shows a solution for those problems allowing for a significant extension of the power rating.

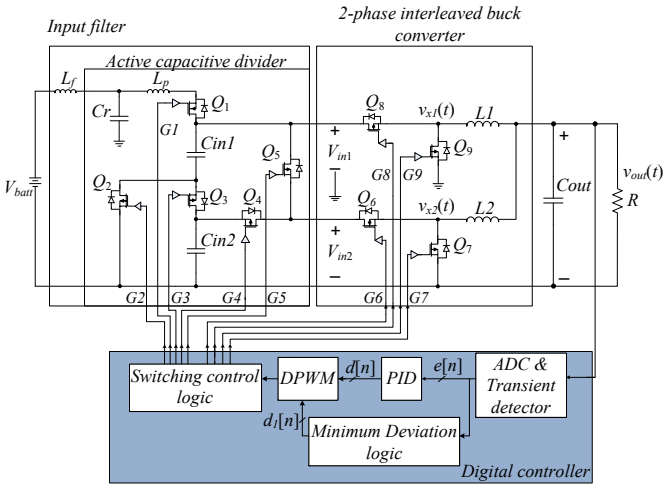

Figure 1. Block diagram of a 2-phase merged switch capacitor buck (MSCB) converter and its digital controller.

This work of Laboratory for Power Management and Integrated SMPS is supported by Texas Instruments Incorporated, Santa Clara.

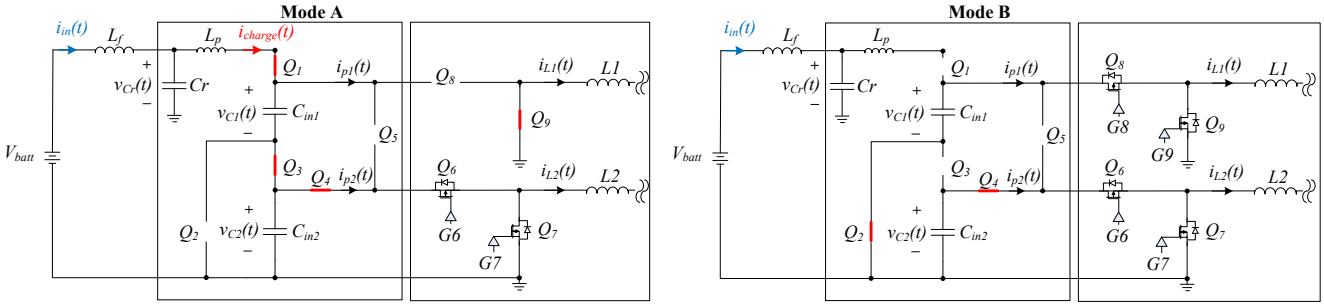

Figure 2. Operating modes of the capacitive attenuator.

II. Principle of Operation and System Description

The converter introduced here operates on the same principle as the other 2-stage solutions [5]-[8]. Namely, the input battery voltage V_{batt} is reduced with a front-stage switch-capacitor converter and supplied to the downstream buck stage. The effect of this input voltage reduction can be quantitatively described through the expression for the inductor current ripple of a buck converter [9]

$$\Delta I_{ripple} = \frac{V_{out}}{2L} \cdot \left(1 - \frac{V_{out}}{V_{in}}\right) \cdot \frac{1}{f_{sw}} \qquad (1)$$

where V_{out} is the output voltage, L is the inductance value, and f_{sw} is the converter switching frequency. It can be seen that a decrease of the V_{out}/V_{in} ratio allows for reduction of the L without paying a penalty in the inductor and output capacitor ripple values. In addition to allowing for filter minimization, the input voltage reduction also minimizes switching losses of the buck stage, which are proportional to the power transistor switching voltages [9].

In the system of Fig.1, the reduction of the input voltage for the downstream buck converter is achieved by modifying the input filter and replacing its capacitor with a switch capacitor circuit of an approximately the same volume. This switch-capacitor circuit acts as a capacitive divider providing two input voltages for the buck stage $v_{in1}(t)$ and $v_{in2}(t)$, which values are approximately equal to a half of the input battery voltage V_{batt}. Since the volume of a capacitor depends on its energy storage capacity [10], i.e. $We = ½CV^2$, the total volume of the divider capacitors is no larger than that of the conventional input filter capacitor, even though their individual capacitances are larger. Operation of the converter is controlled with a single voltage mode digital pulse-width modulation controller where, as will be described in this section, the regulation of the attenuator tap voltages $v_{in1}(t)$ and $v_{in2}(t)$ is provided through an inherent feedback loop existing in this topology. For small values of error signal $e[n]$ the converter operates in steady-state mode. The output voltage is regulated with a PID regulator, digital pulse width modulator (DPWM) [11], [12], and a *switch selector* that sets the transistor switching sequence as described below.

A. Steady-state operation and elimination of the output capacitor of the SC stage

The operating modes of the attenuator, i.e. SC stage, and the key converter waveforms are shown in Figs.2 and 3. The converter operates such that the upper buck phase of Fig.1 (controlled by Q_8 and Q_9) is always supplied by the voltage across C_{in1}, i.e. $v_{in1}(t)$, and the lower buck phases (controlled by Q_6 and Q_7) by $v_{in2}(t)$. The SC stage operates in synchronization with the buck and, in each switching cycle, it goes through two modes, shown in Fig.2. In *mode A* it charges the cascade connection of C_{in1} and C_{in2}, through a quasi resonant circuit formed of a small capacitor C_r, a parasitic pcb inductor L_p, and switches Q_1 and Q_3.In this mode transistors Q_2, Q_5 and Q_8 are open and the upper phase of the buck converter operates in synchronous rectification mode, i.e. the transistor Q_9 is turned on. During this time the lower buck phase can be in any of the two switching states.

As described later, the quasi-resonant switch is used to obtain zero current switching eliminating switching losses of switches Q_1 and Q_3.

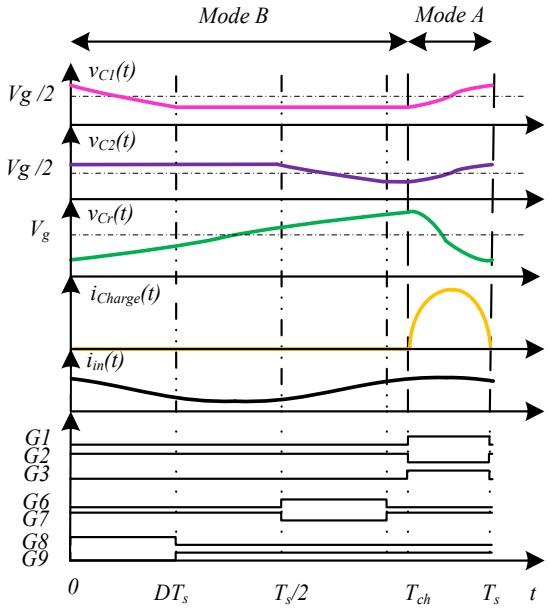

Figure 3. Key waveforms of the MSCB converter.

In *mode B* the *switch control logic* changes the circuit configuration such that C_{in1} is only connected to the upper phase and C_{in2} to the lower one. During this mode the buck phases can be in either of the two switching states and discharge the capacitors during the times when their main switches (Q_6 and Q_8) are on, through the inductors of the downstream stages.

A.1. Inherent centre tap voltage regulation

The previously described operation inherently provides regulation of the SC tap voltages, eliminating the need for a relatively large charge-balancing output capacitor existing in the front stages of other SC based 2-stage solutions [5]-[7].
The voltage regulation as well as the current sharing between the phases can be described through an analysis of the dc equivalent circuit of the converter shown in Fig.4. In this case the source I_{charge} represents the average current provided to the divider over one switching cycle, i.e. during *mode A* (Fig.2). The equivalent resistances of the phases modeling the losses are R_{eq1} and R_{eq2}. To simplify explanation it is assumed that both phases operate with the same effective duty ratio D.
Capacitor charge balance equations [10] for the input capacitors result in

$$DI_{L1} = DI_{L2} = I_{charge} \tag{2}$$

where I_{L1} and I_{L2} are dc values of the phase inductor currents. By using (2) and solving the circuit of Fig.4, the following expression for the difference in the tap capacitor voltages can be obtained:

$$V_{c1} - V_{c2} = \left(R_{eq1} - R_{eq2}\right) I_{L1/2} / D \tag{3}$$

These equations show that the current sharing is achieved and that for the targeted applications where R_{eq1}-R_{eq2} is relatively small, the tap voltages in steady state remain approximately the same. The equations also show that the current and voltage sharing is not affected by the mismatches in the inductor and capacitor values. In other words, an inherent feedback for maintaining the same currents in both phases exists. The phase with a large equivalent resistance will also have a higher tap voltage so that its current is the same as in the other one.

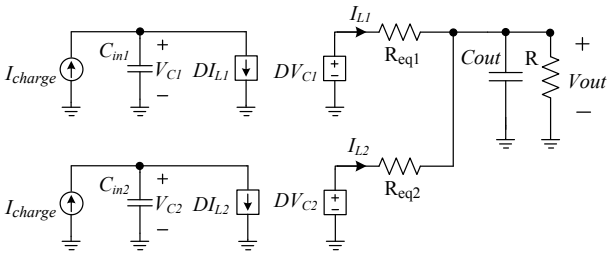

Figure 4. Approximate Dc equivalent circuit of the converter.

Taking duty ratio mismatches into account, (2) and (3) will be transformed into (4) and (5).

$$D_{eq1} I_{L1} = D_{eq2} I_{L2} = I_{charge} \tag{4}$$

$$D_{eq1}.V_{c1} - D_{eq2}.V_{c2} = I_{Charge}.\left(\frac{R_{eq1}}{D_{eq1}} - \frac{R_{eq2}}{D_{eq2}}\right) \tag{5}$$

where D_{eq1} and D_{eq2} represent effective duty ratios of upper and lower buck phases respectively. As shown by (4), the inductor currents will only be affected by the mismatch in the duty ratios proportionally.

A.2. Soft-switching

The SC converters often suffer from excessive switching losses due to direct energy transfer between the capacitors [7]. To eliminate this problem, a quasi-resonant switch is used. The switch is formed by a parasitic inductance of the pcb, L_p, and a small capacitor C_r in series with C_{in1} and C_{in2} (Fig.2b), and transistors Q_1 and Q_3. The resonant circuit parameters are chosen such that the charging of C_{in1} and C_{in2} is completed over the duration of *mode A,* as shown in Fig.3.

This period can be expressed as

$$T_s - T_{ch} \approx \pi \sqrt{L_p C_r}\ , \tag{7}$$

and should not exceed the conduction time of the synchronous rectifier, Q_9, to maintain the low voltage at the input of the upper buck phase.

B. Transient mode

Sudden load changes are captured by the *transient detector* of Fig.1. It triggers the *minimum deviation block* that implements a minimum deviation control algorithm [13]. During large light-to-heavy load transients this block also changes operation of the *switch control logic*, such that the capacitive divider is bypassed and the equivalent circuit of Fig.5 is formed. In this mode the inductor slew rate is increased because the full battery voltage supplies the buck phases.

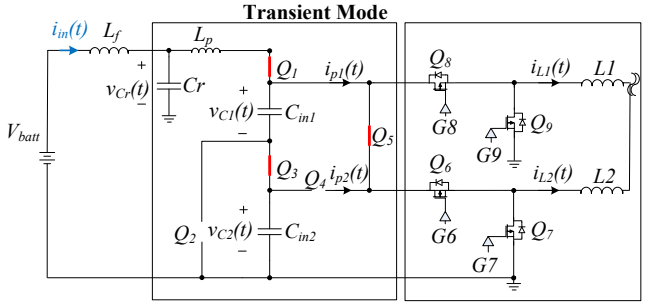

Figure 5. Converter configuration during a light-to-heavy load transient.

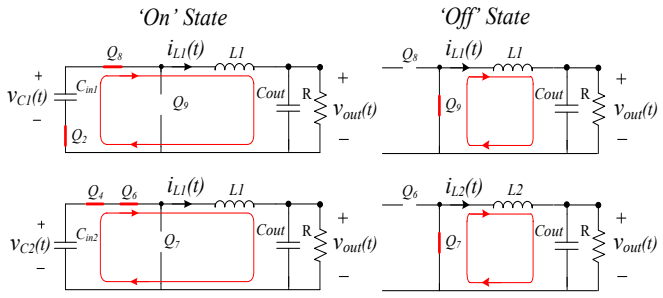

Figure 6. Equivalent circuits of the top and bottom phase of the downstream buck for the both portions of a switching interval.

III. Practical Implementation

A. Output filter reduction

By looking at (1) it can be seen that, in comparison with the conventional buck, the 2-stage converter topology allows the output filter inductor to be reduced by the ratio $(V_{batt}-2V_{out})/(V_{batt}-V_{out})$, where V_{batt} is the input battery voltage. Theoretically, this reduction results in an equivalent improvement of the inductor current slew rate and, consequently, proportional minimization of the output capacitor. However, as shown in [8], the linearly proportional reduction is not feasible in practice, due to the finite delays of the control circuit.

B. Conduction losses and switch selection

The elimination of the energy storage capacitor of the SC stage also brings another main benefit of this circuit compared to other SC-based solutions. Since the extra switches needed for the control of energy storage capacitor are eliminated, the conduction losses are reduced. This converter has just a minor increase in conduction losses compared to the conventional single-stage buck. When Q_7 and/or Q_9 are turned on, the downstream stage has the same conduction losses as the conventional buck and only one low resistance switch is added during the other portion of the switching interval. Also, since the switches Q_1 and Q_3 conduct relatively small current, their conduction losses are relatively small. It can be seen that the new topology introduces only one extra transistor during the "on states" of the buck phases and does not increase the conduction losses during the "off" states. As seen from Fig.2 and Fig.5, the blocking voltage of the extra transistors (Q_2 and Q_4) is $V_{batt}/2$. Hence, their R_{on} resistances can be smaller than that of the main switches Q_8 and Q_6 bringing a small extra contribution to the conduction losses. In comparison with most other two stage solutions [5]-[7] this penalty in conduction losses is minor.

Table I. Filter components parameters.

Parameter	L*f*	C_r	L_p	C_{in2}/C_{in1}	L_1 , L_2	C_{out}
MSCB	100nH	1.6 µF	3n	18.8µF	400nH	35µF
Buck	100nH	-	-	18.8µF	470nH	40µF

IV. Experimental System and Results

To validate the advantages of the introduced 2-stage converter topology a 7V-to-1V, 10A, 1 MHz experimental prototype was built and its performance compared to that of an equivalent interleaved buck.

The output filters of the both converters are selected so that current ripples are the same as well as the output voltage deviation during zero to maximum current load transients. In both cases an optimal controller [13], [14] resulting in theoretically minimum possible voltage deviation is used. Also, the input filters are designed such that the input current ripple is the same.

The parameters of both converters are shown in Table I. It can be seen that the new topology reduces the output filter inductor by 15% and the output capacitor by 13%. The operation of SC stage and gating signals during steady-state can be observed in Fig. 7.

The light-to-heavy transient responses are compared for 2 A to 8 A load steps (Figs.8 and 9). As shown, the 2-stage converter has the same voltage deviation and about 15% faster settling time than the buck. It can also be seen that, as predicted by (2), the current is shared equally between the buck phases during steady state. The efficiency results of both converters are shown in Fig.9. The 2-stage topology improves efficiency by up to 9% at light loads (reduces losses by 35%) and by 3% for medium loads, due to reduced switching losses.

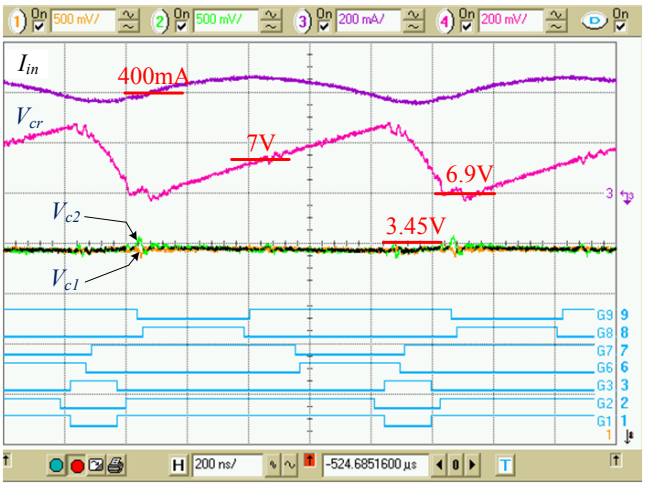

Figure 7. SC stage waveforms and gating signals during steady state operation.

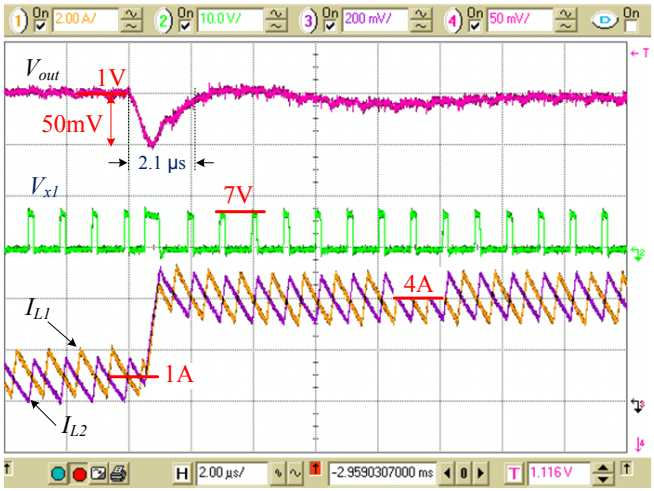

Figure 8. Transient response for buck converter

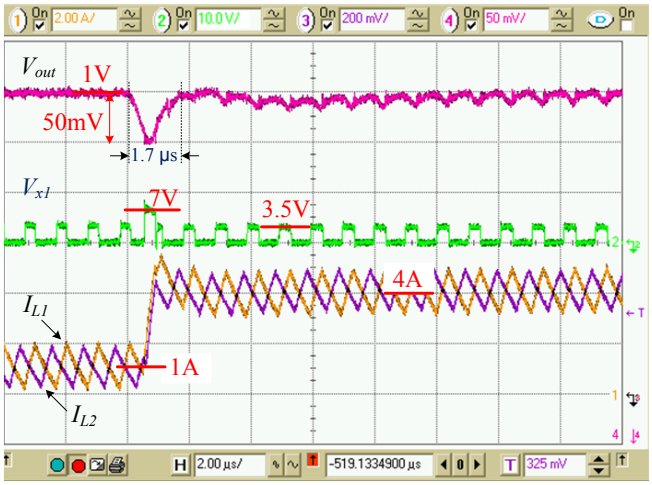

Figure 9. Transient response for MSCB converter

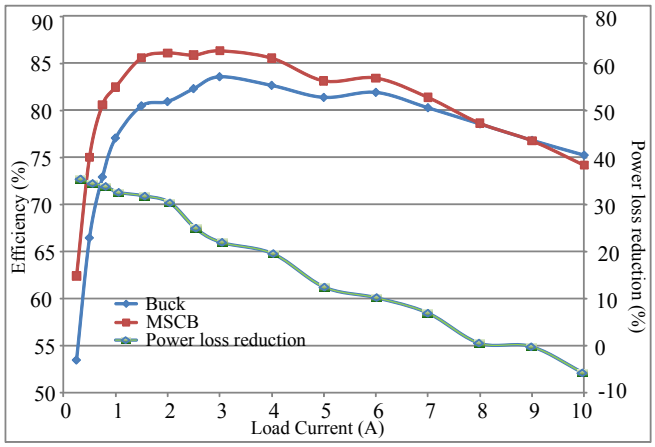

Figure 10. Efficiency and loss comparison of buck and MSCB converters.

V. Conclusions

A 2-stage digitally controlled converter that merges a switch capacitor converter (SC) with an interleaved buck is introduced. Through utilization of buck inductors for SC tap balancing, the new converter eliminates a bulky energy transfer capacitor existing in other 2-stage SC solution reducing conduction losses and controller complexity. To minimize switching losses of the SC a quasi resonant switch is employed. At heavy loads the efficiency of the MSCB is comparable to the conventional buck and at light and medium loads it is improved. The effectiveness of the MSCB is verified experimentally by comparison with a conventional buck, where the improvements in efficiency, filter volume, and dynamic response are demonstrated.

References

[1] N. Rahman, A. Parayandeh, K. Wang, and A. Prodić, "Multimode digital SMPS controller IC for low-power management," in *Proc. IEEE International Symposium on Circuits and Systems*, 2006, pp. 5327 – 5330.

[2] J.Xiao, A.V. Peterchev, J. Zhang, and S.R. Sanders, "A 4-µA Quiescent-Current Dual-Mode Digitally Controlled Buck Converter IC for Cellular Phone Applications," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2342–2348, Dec. 2004.

[3] Y. Kaiwei, "High-frequency and high-performance VRM design for the next generations of processors," Ph.D. thesis, Virginia Polytechnic Institute and State University, 2004.

[4] "Intel Atom Processor 230 Series," Intel Corp., Oregon, USA, April 2010.

[5] J. Sun, M. Xu, and F. C. Lee, "Transient Analysis of the Novel Voltage Divider," in *Proc. IEEE Applied Power Electronics Conf.*, 2007, pp. 550–556. Feb. 2007.

[6] Julu Sun; Ming Xu; Yucheng Ying; Lee, F.C.; , "High Power Density, High Efficiency System Two-stage Power Architecture for Laptop Computers," Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE , vol., no., pp.1-7, 18-22 June 2006

[7] R.C.N. Pilawa-Podgurski, D.M. Giuliano, D.J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in Proc. IEEE Power Electronics Specialist Conf., 2008, pp. 4008-4015, June 2008.

[8] A. Radić, A. Prodić, "Buck converter with merged active charge-controlled capacitive attenuation," IEEE Transactions on Power Electronics, in press.

[9] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics. New York, NY: Springer Media Inc., 2001.

[10] R. Aparicio, A. Hajimiri. "Capacity limits and matching properties of lateral flux integrated capacitors," in *Proc. IEEE* Customs Integrated Circuits Conf., 2001, pp. 365-368, May 2001.

[11] A. Prodić, D. Maksimović, "Design of a digital PID regulator based on look-up tables for control of high-frequency DC-DC converters," in *Proc. IEEE Computers in Power Electronics Conf.*, June 2002, pp. 18-22.

[12] Syed, A.; Ahmed, E.; Maksimovic, D.; Alarcon, E.; , "Digital pulse width modulator architectures," Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, vol.6, no., pp. 4689- 4695 Vol.6, 20-25 June 2004

[13] A. Radić, Z. Lukić, A. Prodić, and R. de Nie, "Minimum deviation digital controller IC for single and two phase DC-DC switch-mode power supplies," in *Proc. IEEE Applied Power Electronics Conf.*, 2010, pp. 1–6. Feb. 2010.

[14] A. Radić, A. Prodić, and R. de Nie, "Self-tuning mixed-signal optimal controller with improved load transient detection and smooth mode transition for dc-dc converters," in *Proc. IEEE Energy Conversion Congress and Exposition Conf.*, 2010, pp. 3096–2010. Sep. 2010