Noninvasive Self-Tuning Output Capacitor Time Constant Estimator For Low Power Digitally Controlled DC-DC Converters

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***Abstract*— A passive and hardware efficient output capacitor time-constant estimator for digitally controlled dc-dc converters is introduced. The estimator emulates the equivalent RC circuit of the output capacitor with a much smaller version, placed in parallel, and adjusts its own resistance until the two circuits have the same time-constant. The adjustment is based on a very simple zero voltage crossing detection and synchronization with the digital pulse-width modulator operation.**

The effectiveness of the proposed estimator is illustrated using a 5V-to-1V/5A, 500kHz buck converter demonstrating accuracy within a few tens of ns in the detection of capacitor zero current crossing points.

I. INTRODUCTION

In realistic dc-dc converters the output capacitors often have a non-negligible equivalent series resistance that, together with the capacitance value, form the output capacitor time constant [1]. An accurate estimation of that constant and/or emulation of the realistic capacitor behavior is of a key importance for fast transient response control methods [1]-[4] and implementation of the power stage health monitoring systems [5]-[7]. In the fast transient response methods allowing for the output capacitance reduction, emulation of the realistic capacitor behavior is often used to determine the output capacitor current and, consequently, produce near time-optimal dynamic response [1]-[4]. The monitoring of the output capacitance time constant in power stage health-monitoring systems drastically improves system reliability [5]-[7]. It enables early fault detection, timely repairs, and consequent prevention of one of the main sources of drastic power supply failures [7].

Due to these potential advantages a number of non-invasive [1]-[7] and invasive [9], [10] output capacitor time-constant estimators have been previously proposed. The non-invasive estimators, which usually consist of a small RC filter placed in parallel with the output capacitor, can generally be divided into static and self-tuning. In static solutions [1]-[4] the time constant of the filter is matched with that of the power stage capacitor, assuming nominal operating conditions. These solutions often exhibit significant estimation error as the conditions change [4]. The self-tuning solutions presented in [5]-[7] are not sensitive to operating conditions. However, they require fairly complex hardware, such as a fast analog-to-digital converter (ADC), to obtain digital representations of the input current, load current, or the output voltage. As such, they are not most suitable for the targeted cost-sensitive low-power dc-dc supplies. The invasive solutions, presented in [9], [10], eliminate the RC filter and the need for a dedicate ADC. However, they usually introduce significant perturbations in the output voltage and require complex calculations, i.e. powerful processing unit. Such perturbations affect voltage regulation and may cause stability problems during frequent load transients, commonly found in the targeted applications.

The main goal of this paper is to introduce a hardware-efficient self-tuning estimator that does not have drawbacks of the previously presented solutions. The new solution that in Fig.1 is labeled as $R_{esr}C$ *estimator*, builds upon the non-invasive estimator used in [1], [3], [4], where a small high-

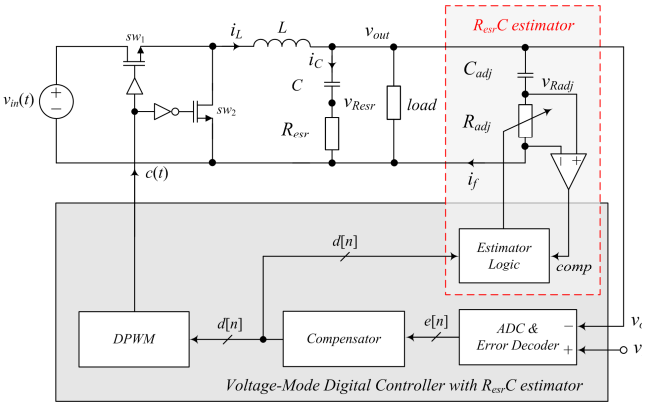

Figure 1: A block diagram of a digitally controlled buck converter that incorporates self-tuning non-invasive $R_{esr}C$ estimator.

impedance RC circuit is placed in parallel with the output capacitor. In this case, to provide self-tuning capability, this RC circuit has an adjustable resistor, R_{adj}, which is tuned continuously using only the knowledge of the two steady-state capacitor zero-current crossing points and synchronization with the digital pulse width modulator.

In the following section, the operation of the introduced output capacitor time-constant estimator is presented. Section III discuses issues related to the practical implementation. Section IV presents experimental verification.

II. Principle of Operation

The self-tuning time constant estimator of Fig. 1 operates on the well-known time constants matching principle utilized in non-invasive estimation methods [1]-[4] and in the RC based inductor current estimation methods [11], [12]. In these systems, an RC filter is placed in parallel with a non-ideal element whose current is estimated. For the case when the time constants of the output capacitor and the filter are the same, the currents going through both elements have the same waveshapes and no delay between them can be noticed.

The system of Fig.1 utilizes a miniature filter consisting of a capacitor C_{adj}, which is much smaller than the power stage capacitor C, and a variable resistor R_{adj} whose value is much larger than the equivalent series R_{esr}. This estimator periodically adjusts the R_{adj} value, such that $C_{adj}R_{adj} = CR_{esr}$. The estimation is performed during converter steady state only. During transients the operation of the estimator is suspended, i.e. it is placed in a sleep mode.

In order to match the $C_{adj}R_{adj}$ and CR_{esr} time-constants, this estimator takes advantage of the buck converter steady-state capacitor current waveform. Namely, the fact that during steady-state the capacitor current, $i_c(t)$, shown in Fig.2, has a triangular waveform with two well-defined zero crossing points. The first zero crossing occurs at $dT_{sw}/2$ and the second at $(1+d)T_{sw}/2$, with respect to the beginning of the switching cycle [13], where d is the duty ratio value and $T_{sw} = 1/f_{sw}$ the switching period. For the case when $C_{adj}R_{adj} = CR_{esr}$, the small current going through the filter, $i_f(t)$, will have the same wave-shape and zero crossing points. This also means that *the voltage drop across* R_{adj} (v_{Radj} in Fig1) *will only have the zero crossing points at* $dT_{sw}/2$ *and* $(1+d)T_{sw}/2$ *when the two time constants are matched*.

This observation is used in the self-tuning process of the estimator shown in Fig.1. It has a synchronous comparator that monitors the voltage drop across R_{adj} This comparator is triggered by the digital pulse-width modulator (DPWM), at one of the output capacitor zero crossing points, and, accordingly, the R_{adj} is adjusted until the zero value at the input of the comparator, i.e. time constants matched condition, is detected. In this way, the need for costly capacitor current sensing and actual comparison of $i_c(t)$ and v_{Radj} is eliminated.

When the two time-constants are not equal the resistor voltage v_{Radj} takes one of the two forms shown in Fig. 2. For the case when $R_{adj}C_{adj} < R_{esr}C$, the zero crossing of v_{Radj} occurs before the output capacitor current zero crossing and for $R_{adj}C_{adj} > R_{esr}C$ it happens later.

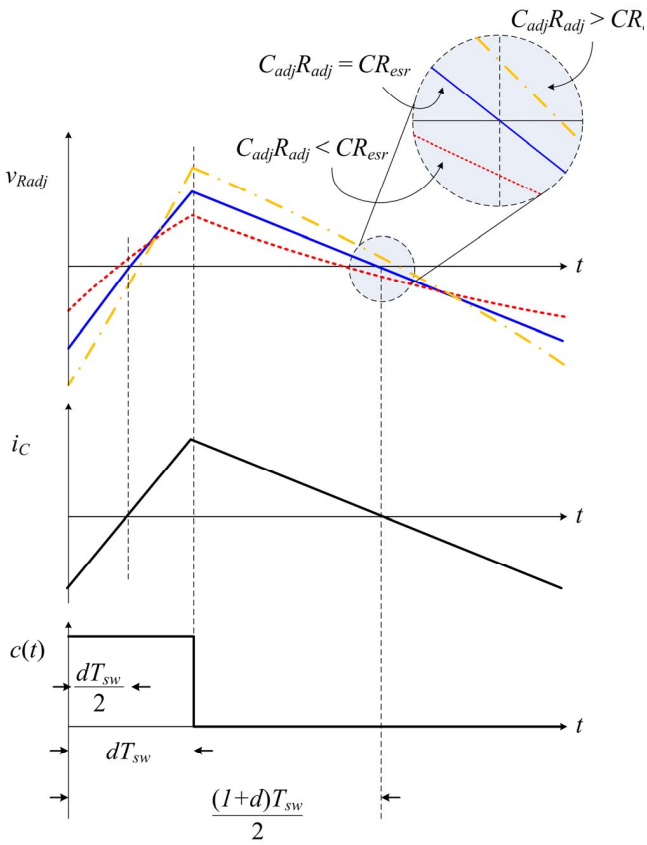

Figure 2: Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: v_{Radj} - voltage across the estimator resistor, $i_c(t)$ – the output capacitor current and $c(t)$ – signal produced by the DPWM.

Therefore, by simply measuring the polarity of the v_{Radj} value at one of the two zero crossing points, the time-constant can be adjusted such that it converges to a value equal to the output capacitor.

III. Practical Implementation

A practical realization of the estimator is shown in Fig. 3. It consists of an operational amplifier, a binary-weighted resistive network, four small transistors, a comparator, a sample and hold circuit *S/H*, and simple digital logic.

The amplifier with a relatively low-gain and a low-bandwidth is used to eliminate the high frequency switching noise and increase the estimator input when operating with low output voltage converters. This amplification improves the zero crossing point detection, reducing comparator speed and, consequently, power requirements.

The polarity of v_{Radj} at the zero capacitor crossing points is determined through sampled comparator value $comp_s$. The comparator is sampled once per cycle, using information about the digital equivalent of the duty-ratio value, $d[n]$, from the control loop (Fig.1). Accordingly, the equivalent R_{adj} value is adjusted using the binary-weighted resistive network and the estimator logic of Fig.3 [14].

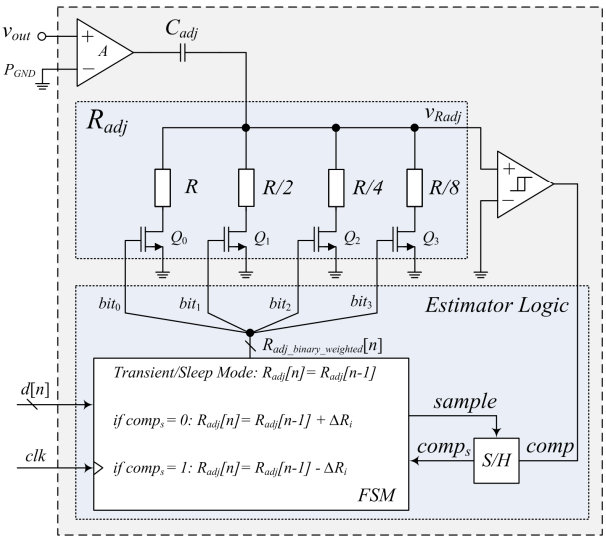

Figure 3: Practical implementation of the estimator.

In order to minimize any switching noise effects, the second sampling point, $((1+d)T_{sw}/2)$, is used when the duty ratio is less than 0.5. In most of the targeted applications the duty ratio is significantly smaller than 0.5; therefore, for the following analysis the second sampling point is used.

When $comp_s$ is low, the R_{adj} is increased and when $comp_s$ is high, the R_{adj} value is reduced. In order to speed up the tuning process, during the start-up, when a large initial time-constant error is likely, a binary search algorithm is utilized [15]. The binary search algorithm changes the resistance in larger steps, significantly reducing the worst case tuning time, from 15 cycles for the linear search to 4 cycles for the binary search [15]. Once the start-up mode is finished a linear, finer, search algorithm is applied until the time-constants are matched. This condition is indicated by hi-lo or lo-hi transition of the S/H output. At this point the estimator enters *sleep* mode and only occasionally is re-engaged upon the exit of a transient or after a pre-defined wait time.

In order to minimize the estimation error due to the gate driver transmission delay a simple delay measuring circuit, shown in Fig. 4, can be utilized. It counts the number of clock cycles, t_{clk}, between the *DPWM* control signal, $c(t)$, and the switching node rising edge, $v_x(t)$. The digital representation of the total gate driver and converter turn-on time delay, $t_{delay}[n]$, is then added to the nominal sampling point, thus eliminating its effect.

IV. Experimental Results

To verify the operation of the estimator a 5V-to-1V, 5A, 500 kHz, digitally controlled, buck converter prototype was built based on the diagrams of Figs. 1 and 3. The converter has a 1.5µH output filter inductor and a 100 µF ceramic output capacitor with $R_{esr} \approx 25m\Omega$. To form the estimator filter, a small 2 nF capacitor and a resistive network covering 640 to 9600 Ω range of values are used.

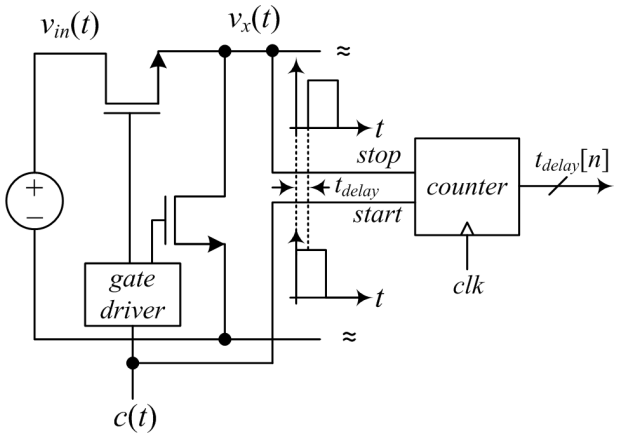

Figure 4: Circuit for estimating gate driver and converter turn-on delay.

This network allows for variation of the estimator time constant over the full range of expected CR_{esr} variations. The results of experimental system verification are shown in Figs. 5 and 6. Figure 5 illustrates how the $R_{adj}[n]$ control value, described in the previous section, is changing during the auto tuning process. It can be seen that, unlike invasive solutions, this estimation method does not affect the output voltage regulation and that the system stability is maintained throughout the full operating range. Figure 6 shows zoomed-in capacitor current and the estimator voltage before and after the tuning, respectively.

The results demonstrate the effectiveness of the estimator. It can be seen that the delay between zero crossings of $i_c(t)$ and $v_{adj}(t)$ has been reduced from 500 ns, indicating a large mismatch in time constants, to 40 ns, corresponding to practically perfectly tuned filter. In the full version of the paper additional experimental results showing filter operation and demonstrating the effect of the filter tuning on the converter transient performance will be given.

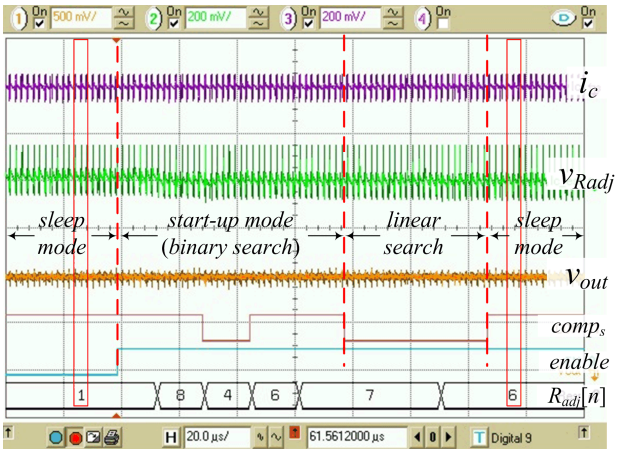

Figure 5: Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: $i_c(t)$ (10 A/div), v_{Radj} (200 mV/div), output voltage of the converter v_{out} (500 mV/div), $comp_s$ - sampled comparator output, *enable*- estimator enable bit, and $R_{adj}[n]$ binary resistor control value. Time-scale (20µs/div).

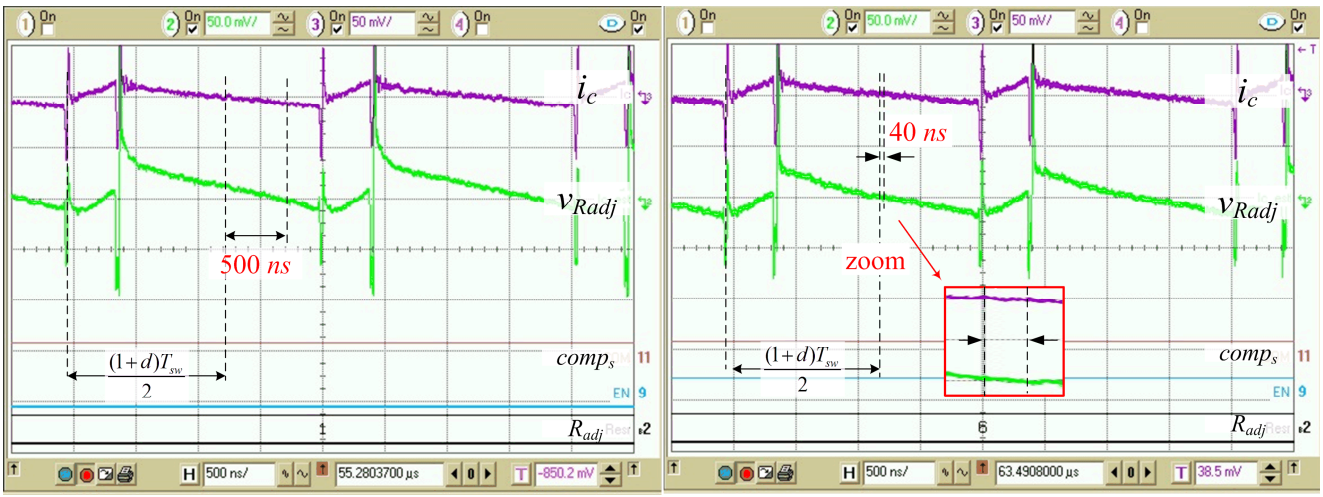

Figure 5: Actual and estimated output capacitor ESR voltage before (left) and after (right) the tuning process. Top-to-bottom: $i_c(t)$ – the output capacitor current (2.5 A/div), v_{Radj} - voltage across the estimator resistor (50 mV/div), $comp_s$ – sampled comparator output, $R_{adj}[n]$ – binary-weighted representation of the resistor. Time-scale – 500ns/div.

V. Conclusions

A hardware-efficient noninvasive output capacitor time-constant estimator for low-power digitally controlled dc-dc converters is presented. The estimator operates on a simple principle of detecting the mismatch between the estimator output and the output capacitor zero value crossings. To eliminate the need for costly capacitor current sensing the mismatch detection is performed through synchronization with the digital pulse-width modulator. Experimental results verify accurate on-line tuning that is not affecting the output voltage regulation.

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