Mixed-Signal CPM Controlled DC-DC Converter IC with Embedded Power Management for Digital Loads

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***Abstract*— This paper presents a novel system and a method for dynamic minimum power point tracking of digital loads in portable applications. The system combines a dc-dc power stage converter IC and the supplied digital load. The dc-dc converter IC employs a mixed-signal current mode (CPM) controller to regulate the supply voltage of an on-chip integrated digital load. The CPM controller is also utilized to obtain information about the input current of the system in real-time, eliminating the need for a dedicated power sensing circuits. The obtained information about the current is utilized by a minimum power point tracking (MiPPT) controller. The MiPPT sets the supply and threshold voltages for the digital load to minimize its power consumption while maintaining a targeted frequency. The dc-dc converter IC, providing 600mW of power, and its digital load IC are fabricated in a 0.13 µm process. Experimental results verify that the introduced system results in up to a 30% lower power consumption.**

I. INTRODUCTION

In recent years, the demand for more features in consumer electronics has led to rapid growth of smart devices that offer convergence of various technologies in a single product. For example, mobile smart phones now combine video streaming, camera, MP3 capacity, global positioning system (GPS) navigation, and different software services in a single device. As a result, the power consumption of digital signal processing circuits has increased drastically. Consequently, obtaining a fairly long battery-powered operation has become a major challenge [1-7].

The power consumption of a digital processor is dominated by leakage and dynamic components [7]. The dynamic power is dissipated through charging and discharging gate capacitances [8], while the leakage component is caused by the dc current flowing through transistors when they are turned off [9]. The dynamic consumption can be reduced quadratically, by scaling down the supply voltage [1]. This voltage reduction also slows down the processing speed. To compensate for speed reduction, the threshold voltage can also be scaled down, through the silicon body biasing. However, this biasing process increases the leakage current [9].

Optimizing the trade-off between the dynamic and leakage power consumption is named minimum power point (MiPP) tracking. Since the target speed is maintained during the optimization process, MiPP also corresponds to the minimum energy point of the circuit. Consequently, the minimum power point can be defined as an optimal combination of supply and threshold voltage, where the total energy usage for desired operation of the digital circuit is minimized [2, 4-6, 10-23]. The MiPP is not a fixed point. It changes with the workload and the operating conditions of the digital load. For this reason, a real-time system for minimum power point tracking (MiPPT) is required.

An important challenge in implementing the MiPPT systems is measurement/estimation of the digital circuit power consumption in real-time. In the previous art, various estimation and measurement techniques have been proposed [2, 4, 15, 20, 22]. A common estimation technique is to use replica circuits that mimic the leakage and dynamic power consumption of the actual circuit [4-6, 15]. A major drawback of this technique is that it cannot accurately track the behaviour of the actual circuit as the process and operating conditions change [14]. A more accurate method is to measure the total power consumption directly, using a sense resistor. However, this approach requires an additional dedicated

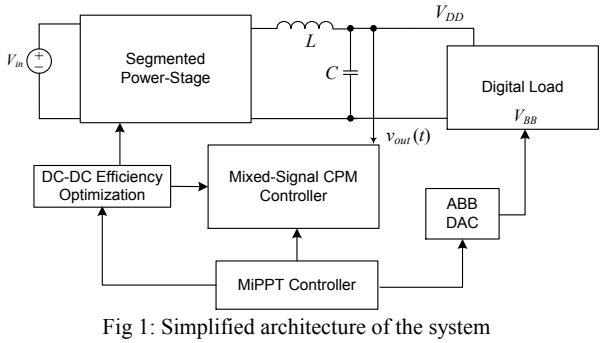

Fig 1: Simplified architecture of the system

analog circuit [10], causes extra losses and, therefore, is rarely used. An additional problem is that the previously presented solutions do not take into account efficiency of the dc-dc converter supplying the load, hence, they open a possibility for sub-optimal energy consumption. If at the selected load MiPP the converter efficiency is significantly degraded, the overall energy consumption of the system could be suboptimal, even in the case when the load takes the minimum amount of power.

In the system introduced here, the dc-dc converter is utilized in measuring the power consumption of the entire system and for implementing the MiPPT algorithm. The system shown in Fig.1 performs a real-time minimum power tracking that takes into account both the efficiency of the dc-dc converter and the digital load consumption. For any given operating condition, it results in the minimum energy consumption from the source.

In the system of Fig.1, both the supply voltage, V_{DD}, and the body-bias voltage of the digital load, V_{BB}, can be changed. The integrated dc-dc converter utilizes a mixed-signal controller to provide a tight regulation of the digital load supply voltage V_{DD}. The body-bias voltage V_{BB} is adjusted using a digital-to-analog converter (DAC). The mixed-signal CPM controller retains the information about the instantaneous load current as well as the supply voltage in the digital domain. The retained information eliminates the need for a dedicated measurement circuitry attached to the load. This information is used to calculate the overall power consumption of the system in real-time. Based on the information available in the dc-dc converter, the MiPPT controller sets V_{DD} and V_{BB} and selects the most efficient mode of operation for the dc-dc converter minimizing the power consumption at the targeted frequency.

II. System Description

A simplified block diagram of the MiPPT system implemented in this work is shown in Fig.2. Its key functional blocks are described in the following sub-sections.

A. Mixed-Signal CPM controlled dc-dc Converter

The dc-dc converter regulates the supply voltage of the digital load and is based on the architecture presented in [24]. The converter performs instantaneous efficiency optimization by dynamically changing modes of its operation over a wide load range. The power transistors and gate-drives are divided into equivalent segments [25]. The controller is a modification of mixed-signal peak current program mode controller [26], where the voltage loop is digital and the internal current loop is analog. A simple Σ-Δ DAC sets the reference for the windowed analog-to-digital converter (ADC) [27]. The ADC compares the sampled output voltage with the reference voltage and converts the error into its digital equivalent, $e[n]$. Based on the error signal, a digital compensator creates the differential current reference, $\Delta i_c[n]$. This information is passed to the DAC, which creates the analog current reference for the SR latch comparator. The digital compensator also creates the

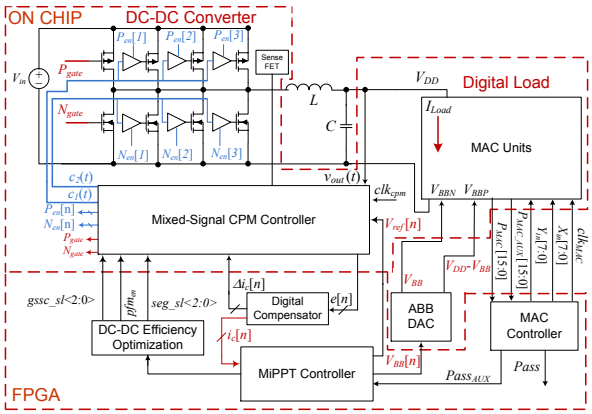

Fig 2: Block diagram of the implemented system.

current reference $i_c[n]$ that determines the instantaneous current for each switching cycle and is used for two purposes. The MiPPT controller of Fig.2 uses the current reference $i_c[n]$ and the converter output voltage reference $V_{ref}[n]$ to measure the power consumption of the load. Therefore the need for an extra power sensing circuitry is eliminated. Additionally the current reference is used by the dc-dc efficiency optimization controller to dynamically improve the efficiency of the converter as the load conditions change.

The dominant sources of loss in high frequency dc-dc converters are switching and conduction losses associated with gate-capacitances and on-resistances of the power transistors [28]. By trading off conduction loss versus switching loss as the current changes, the efficiency can be improved [25]. This is achieved by dynamically adjusting the number of power transistor segments and gate-voltage swing scaling [29]. Based on the instantaneous current reference $i_c[n]$, the efficiency controller of Fig.2 governs the efficiency optimization operation as follows: At heavy loads all power transistor segments of Fig.2 are active and, as the load current reduces, the number of segments decreases, so a favorable tradeoff between conduction and switching losses is achieved. For medium-to-light loads only one transistor segment is active and the instantaneous efficiency optimization is obtained by changing the gate drive voltage swing with the gate swing scaling circuit (GSSC) [24]. For even lighter loads the converter switches to pulse-frequency mode (PFM) of operation further minimizing switching losses and improving the overall efficiency. A more detailed discussion of various blocks of Fig.2 and the efficiency optimization algorithm is presented in [24].

B. The Digital Load

In CMOS digital circuits, the dynamic power is given by [7]

$$P_{Dynamic} = \alpha C V_{DD}^2 f, \qquad (1)$$

where α, the activity factor, accounts for the fact that most gates do not switch every clock cycle , f is the clock

frequency, C is the total gate capacitance and V_{DD} is the supply voltage. The leakage current can be attributed to various components but the dominant component is subthreshold leakage given by [7]

$$I_{Leakage} = I_{ds0}10^{(V_{gs}-V_{th}+\eta V_{ds})/S}, \quad (2)$$

where I_{ds0} is a constant that depends on process and device geometries, η is the drain-induced barrier lowering (DIBL) coefficient, V_{gs} and V_{ds} are gate-to-source and drain-to-source voltages of the transistor and S is subthreshold slope. The dynamic power can be reduced by lowering clock frequency, f , as (1) shows. However this will not result in lower energy consumption from the source since the desired operation will simply take longer to complete. To avoid this situation, an alternative approach is to reduce the power consumption while keeping the frequency constant. Since the time required to complete the operation is constant, minimizing the power consumption, directly results in lower energy consumption. This can be achieved by reducing the supply voltage as shown in (1). Consequently, in order to retain the performance of the circuit, V_{th} also needs to be lower. However based (2) a lower threshold voltage will increase the leakage current and consequently the leakage power [9]. This trade-off between the dynamic power and leakage power will lead to the minimum power point (MiPP) for the digital circuit operating at a certain frequency.

The threshold voltage of a transistor can be tuned by changing the body-bias voltage. This technique, shown in Fig.3, is called adaptive body biasing (ABB) [7, 22]. The V_{BBP} and V_{BBN} refer to the PMOS (nwell) and NMOS (pwell) body-voltages respectively and V_{DD} is the supply voltage of the digital circuit. For the NMOS and PMOS when V_{BBN} is below Gnd and V_{BBP} is above V_{DD} respectively, the devices are in *Reverse Body Bias* (RBB) mode where the threshold voltage increases [7]. On the other hand when V_{BBN} rises above Gnd and V_{BBP} is below V_{DD} respectively, the transistors are in *Forward Body Bias* (FBB) mode which reduces the threshold voltage [7].

A digital test load IC is developed to explore the benefits of supply and threshold voltage scaling in reducing the power consumption of the circuit. The load IC consists of 12 multiplier-accumulator (MAC) units [7] that replicate the interaction between leakage and dynamic power in a real processor or DSP core. The digital load is custom designed such that the body-bias of both NMOS and PMOS transistors (V_{BBN}, V_{BBP}) and consequently their threshold voltages can be adjusted.

C. The MAC Controller

The system shown in Fig.2 uses two MAC ICs as the digital load. The operation of the MAC units is controlled by the MAC controller block. The target clock frequency is generated by the MAC controller. The input vectors X_{in} and Y_{in} are created using pseudo-random bit sequence (PRBS) generators [7] and are continuously sent to the MAC blocks. The MAC controller compares the outputs of the MAC units, P_{MAC} and P_{MAC_AUX} with the output of an ideal MAC block implemented on the FPGA, and generates the *pass* and $pass_{aux}$ signals. If for a given input vector, P_{MAC} or P_{MAC_AUX} do not match the correct output value, *pass* or $pass_{aux}$ are set to zero. However to generate a pass signal, the MAC controller will check the outputs for a sufficiently large set of input vectors. The $pass_{aux}$ is sent to the MiPPT controller of Fig.2. It is used to track the operation at the target speed as the MiPPT controller changes the digital load parameters. The supply voltage of the main MAC unit is slightly higher than the auxiliary MAC unit. This is to insure that the main MAC unit always functions properly (*pass* =1) even as the auxiliary MAC output fails briefly ($pass_{aux}$ =0) due to the operation of the MiPPT controller. For on-chip implementation, the MAC controller block can be considerably simplified. The input vectors can be generated using PRBS circuits that are implemented on chip. Additionally critical path replica method [2, 4-6, 10, 14, 19, 22] can be used to track the circuit speed and eliminate the need for the ideal MAC block. The implementation of the MiPPT algorithm is discussed in the next section.

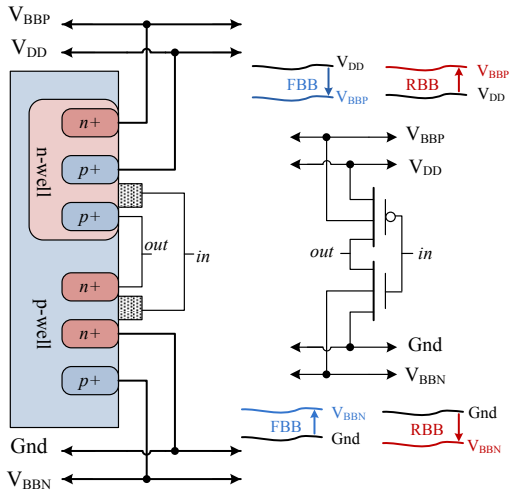

Fig 3: Schematic of an Inverter with ABB

III. MiPPT Controller and Algorithm

The operation of a simple digital load running at a fixed-frequency is shown in Fig.4 across the V_{DD}-V_{th} plane. Each point represents the pass/fail operation of the circuit for the given supply and threshold voltage.

The dynamic power consumption of the circuit can be reduced by lowering the supply voltage as shown in (1). This corresponds to moving to the left from point A in Fig.4 Since the digital logic also becomes slower, the operation of the

circuit fails. Consequently, in order to maintain the target frequency, V_{th} also needs to be reduced. This is achieved by increasing V_{BB} and operating the digital load in FBB. However based on (2) a lower threshold voltage will increase the leakage current and consequently the leakage power [9]. This trade-off between the dynamic power and leakage power will eventually lead to the MiPP at point B.

Based on the information available in the dc-dc converter, the objective of the MiPPT controller is to minimize the power of the load by moving from point A to B shown in Fig.4. The

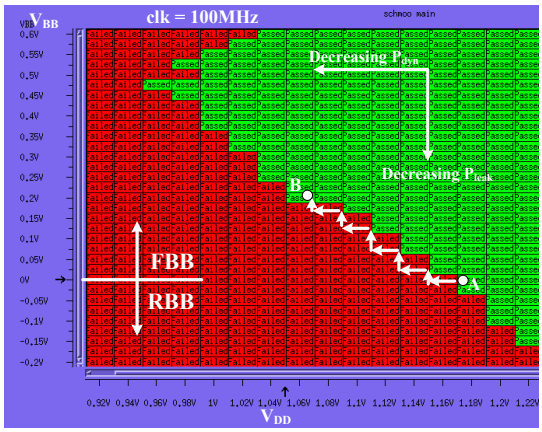

Fig 4: Operation of the digital load across V_{DD}-V_{th} plane

implementation of the MiPPT controller is described in the following sub-sections.

A. ABB Loop

A critical element of the MiPPT algorithm is the ABB loop. The function of this loop is to set the optimal threshold voltage that enables the load to operate at the target frequency (*Pass* =1 and $Pass_{aux}$ =1). The MiPPT controller continuously sets the $V_{BB}[n]$. Based on this value the *ABB_DAC* generates the body bias voltages for PMOS and NMOS transistors.

When the ABB loop is enabled, zero-body-biasing (ZBB) is applied. The controller then checks the value of $Pass_{aux}$. If the auxiliary MAC is working properly ($Pass_{aux}$ =1), V_{BB} is decremented by 1 LSB unit, and the digital load is biased in RBB mode. In other words, the threshold voltage increases and the leakage current of the load slightly decreases.

This operation continues until the auxiliary MAC fails ($Pass_{aux}$ =0), indicating that the MAC has reached the Pass/Fail boundary in Fig.4. At this point, the threshold voltages are set to the previous value (V_{BB} is incremented by 1 LSB unit) and Freq_lock signal is set to high. This indicates that at the current supply voltage, the load is operating with minimum leakage current (maximum threshold voltage allowed for target frequency). On the other hand if upon start-up the load is in fail state ($Pass_{aux}$ =0), the controller increments V_{BB}, thereby reducing the threshold voltage until either $Pass_{aux}$ turns high or it reaches the maximum FBB voltage allowed.

B. The MiPPT Algorithm

The flowchart shown in Fig.5 demonstrates the operation of the MiPPT loop. When the MiPPT controller is enabled, initially the ABB loop is activated. After the body-bias voltages are set, the power consumption of the load is calculated based on the real-time information obtained from the CPM controller of the dc-dc converter IC. The supply voltage, V_{DD}, is then decremented (perturbed) by changing the voltage reference of the dc-dc converter loop, $V_{ref}[n]$. At lower supply voltage the digital load is slower, therefore, the operation of the auxiliary MAC fails ($Pass_{aux}$ =0, although the actual MAC remains operational since its supply voltage is 1 LSB above the auxiliary MAC). At this point, the ABB loop is activated again. To meet the target frequency it adjusts the body-biases and lowers the threshold voltage. When the operation of the ABB loop is completed, the power consumption of the load is measured and compared with the

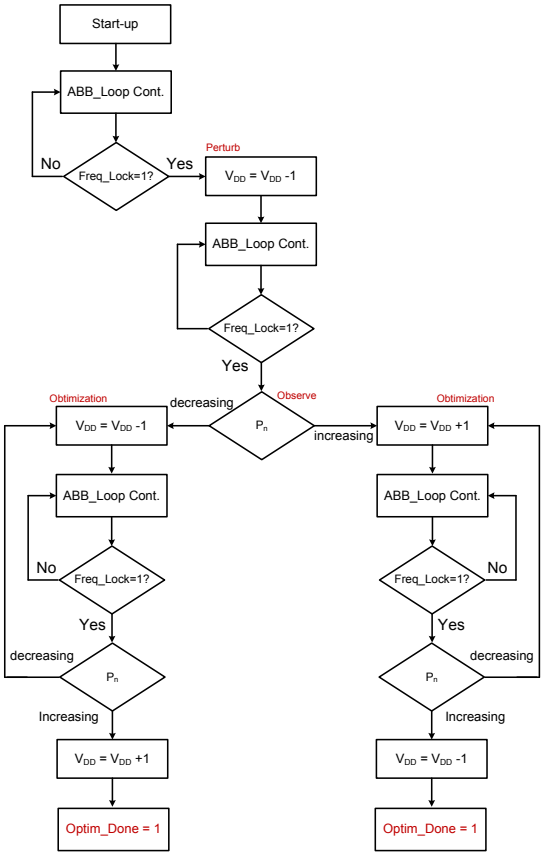

Fig.5: Flowchart showing the operation of the MiPPT loop

initial stored value. If the power of the load is decreasing, the supply voltage is further decremented by the controller. The ABB loop, is activated again, and the threshold voltage is scaled lower. This cycle repeats until the power of the load begins to rise. At this point, the loop stops and sets the previous values for the supply and threshold voltage to operate the load at the minimum power point.

If the initial supply voltage is lower than the optimal supply voltage, then the load power increases when the supply voltage is decremented. The controller detects this and changes direction to move toward the MiPP. Now the supply voltage is incremented, and ABB loop increases the threshold voltage. The loop stops when the power of the load starts increasing.

The MiPPT controller also governs the operation of the dc-dc efficiency optimization controller. As long as the digital load is operational (*Pass* =1 and $Pass_{aux}$ =1), the efficiency controller continuously reconfigures the dc-dc converter to minimize converter losses for the given load current. Therefore, when the MiPPT loop settles to the minimum power point and the dc-dc converter efficiency is maximized, the power taken from the battery source will be minimized.

IV. Experimental Results

An experimental setup based on the system shown in Fig.2 is built. The integrated dc-dc converter with the mixed-signal CPM controller and the digital load are fabricated on separate ICs in 0.13µm IBM technology. The core supply voltage of the MAC is 1.2V. The operation of the MAC is verified for supply voltages as low as 0.4V. Fig.4 also shows the MAC running at 100MHz across the V_{DD}-V_{th} plane. The maximum clock frequency of the circuit is 125MHz at 1.3V. The MiPPT algorithm and the ABB loop have simple implementations in FGPA. They can also be easily implemented on-chip. To verify this, both blocks where synthesized in 0.13µm IBM process using 500 logic gates. The total area of the MiPPT controller is about 0.0078 mm^2 and its power consumption is estimated around 200µA. Since no additional circuitry is used for power sensing, the overall power and area over head of the minimum power tracking controller remains small.

A. DC-DC Converter

Fig.6 shows the efficiency measurement of the dc-dc converter IC. The dc-dc efficiency controller applies different optimization techniques based on the load current and

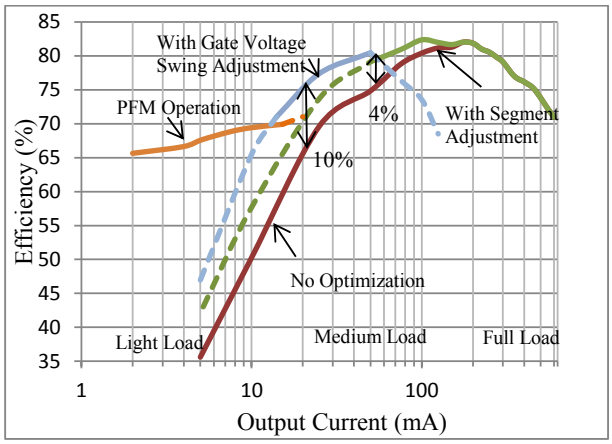

Fig.6: Efficiency measurements of the mixed-signal CPM IC [24]

improves the efficiency over a wide load range. While segment adjustment improves efficiency by as much as 3%, i.e. reduces losses by 13%, at medium load currents, gate voltage swing scaling allows for improvements of around 8% (loss reduction of 26%)at light to medium loads. For light load currents the controller operates the converter in PFM mode for additional savings.

B. MiPPT Controller

The closed-loop operation of the ABB loop is shown in Fig.7. The supply voltage of the digital load is at 1.2V. Initially zero-body-bias (ZBB) is applied to the MAC IC. Since the MAC is functional at this voltage when the ABB loop is enabled, the controller decrements the value of $V_{BB}[n]$. Consequently the ABB_DAC block generates the bias voltages for the MAC chip. The PMOS and NMOS bias voltages, V_{BBP} and V_{BBN} are adjusted in equal steps of 30mV based on the value of $V_{BB}[n]$. Since the load is biased in RBB mode now, the threshold voltage increases, lowering the leakage current of the digital load. The loop continues decrementing $V_{BB}[n]$ until the auxiliary MAC fails ($pass_{aux}$ =0) indicating that the threshold voltage has increased above the optimum value. At this point V_{BB} is incremented by 1 LSB unit and Freq_lock signal is set to high. This indicates that the load is operating at the most energy-efficient point for the given supply voltage. As shown, the output of the main MAC IC does not fail (*pass* =1) during the operation of the ABB loop.

The closed-loop operation of the system of Fig.2 with the MiPPT controller is shown in Figures 8-9. The measured input power of the system is also shown in the figures. Since the digital load operates at constant target frequency, reducing the input power will result in true energy savings from the battery source. In Fig.8, when the controller is enabled, the ABB loop is first activated to adjust the body-bias voltages. When the Freq_Lock signal is set to high, the supply voltage is decremented, and the power of the load is measured. The operation of the auxiliary MAC fails ($Pass_{aux}$ =0) at the lower supply voltage, and ABB loop is enabled again to adjust the threshold voltages. Since the power consumption of the load is decreasing, this process is repeated until it reaches the MiPP. This results in about 30% reduction in the power consumption from the source.

In Fig.9 the initial supply voltage is below the optimal supply voltage. After the ABB loop adjusts the body bias voltages by applying FBB, the supply voltage is lowered. This results in a higher power taken by the digital load as shown in Fig.9. The controller detects this, changes direction and instead increases the supply voltage to reduce the load power. With each V_{DD} step, the ABB loop also adjusts the body biases (increases the threshold voltage). When the load power begins to raise again, the loop shuts down. As a result of the loop operation, the power consumption is reduced by 12%.

The speed of the minimization algorithm is primary limited by the length of input vectors that the MAC controller processes before generating a Pass signal for the auxiliary MAC. Finally, as shown in Fig.8 , the operation of the actual MAC is not disrupted (*Pass* =1) during the minimization process.

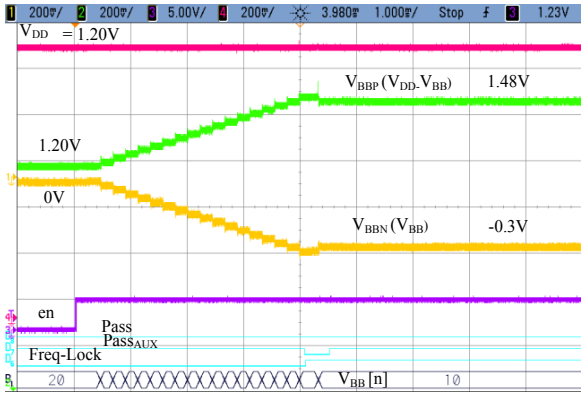

Fig.7: Operation of the ABB loop: Ch-1: V_{BBN}, 0.2V/div. Ch-2: V_{BBP}, 0.2V/div. Ch-3: ABB loop enable, Ch-4: V_{DD}, 0.2V/div. Time Scale: 1ms/div

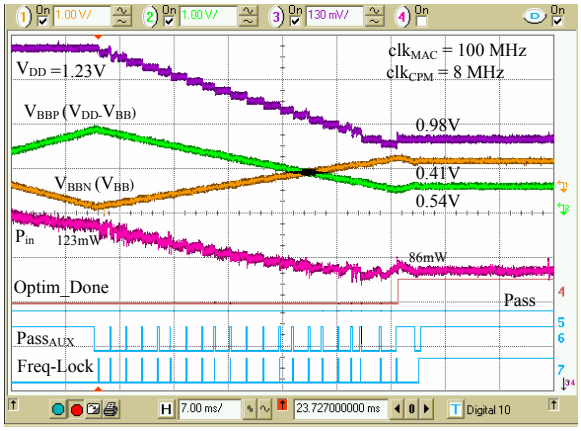

Fig.8: Closed-loop operation of the MiPPT and dc-dc converter: Ch-1: $V_{BBN,}$ 1V/div. Ch-2: $V_{BBP,}$ 1V/div. Ch-3: $V_{DD,}$ 130mV/div, Ch-4: P_{in} 30mW/div. Time Scale: 7ms/div

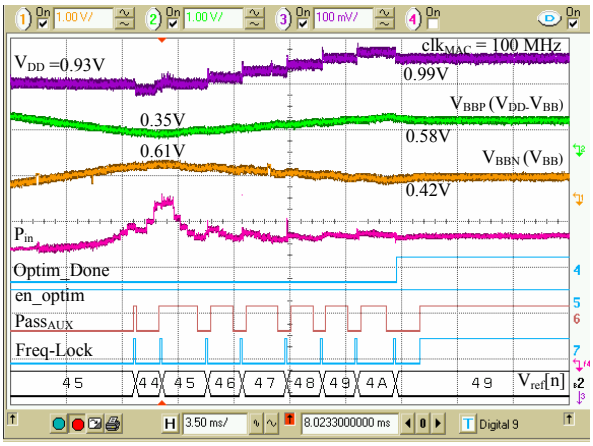

Fig.9: Operation of MiPPT controller when V_{DD} is below the optimum value. Ch-1: V_{BBN}, 1V/div. Ch-2: V_{BBP}, 1V/div. Ch-3: V_{DD}, 100mV/div, Ch-4: P_{in}, 50mW/div. Time Scale: 3.5ms/div

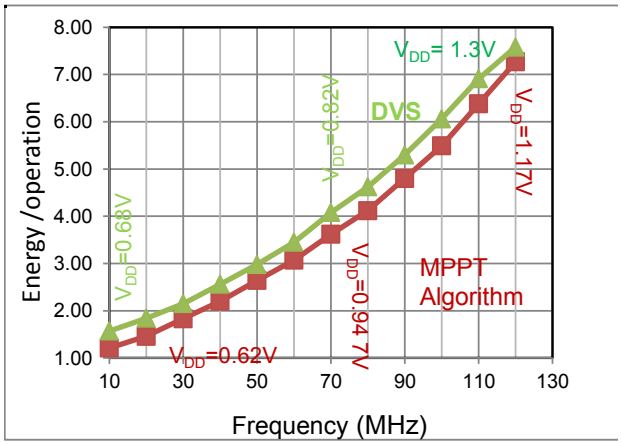

Fig.10: Comparison of DVS with MiPPT controller presented in this work

C. Comparison with DVS

In dynamic voltage scaling (DVS) as the workload conditions change, the supply voltage is scaled such that the system operates only as fast as necessary. As shown in previous works, this, results in significant energy savings compared with fixed-supply voltage operation [30]. However, performing DVS on the digital load will not yield the MiPP since the effect of threshold leakage current is entirely ignored [4]. This has become particularly important in latest nano-scale technology nodes, where the leakage current accounts for a significantly larger portion of total power consumption of the digital circuit. The approach discussed here is more general than the DVS technique. The algorithm, similar to DVS, eventually scales the supply voltage to the optimal value for the target speed. But additionally, it also adjusts the threshold voltage to optimize the ratio of dynamic and leakage power that results in minimum power point consumption. The benefits of the MiPPT algorithm are compared with applying DVS only technique to the MAC IC at different frequencies. As shown in Fig.10 significant additional energy savings are achievable using the techniques discussed in this work.

V. CONCLUSION

A system level solution is presented in this work that tracks the minimum power point of a digital load circuit. The system consists of a dc-dc converter IC that supplies a digital logic load. Based on the information available in the dc-dc converter, the MiPPT controller algorithm sets the load parameters (supply and threshold voltage) to minimize its power consumption at the target frequency. Experimental results of the system verify the operation of the MiPPT controller, which results in 30% reduction in the power consumption from the source.

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