# A LOW-VOLUME POWER MANAGEMENT MODULE FOR PORTABLE APPLICATIONS BASED ON A MULTI-OUTPUT SWITCHED-CAPACITOR CIRCUIT

S M Ahsanuzzaman, Justin Blackman, Timothy McRae, Aleksandar Prodić
Laboratory for Power Management and Integrated SMPS, ECE Department, University of Toronto, CANADA
Email: {ahsansm,prodic}@ele.utoronto.ca

**Abstract— This paper introduces a 2-stage power management architecture for battery powered portable applications. The presented topology combines a fixed ratio multi-output switched capacitor converter stage with two-input buck converters to achieve low volume and high power processing efficiency. Experimental comparisons with a two-cell battery input conventional 5 V bus architecture, providing 15 W of total power in three different voltage outputs, demonstrate up to 50% reduction in the inductances of the downstream converter stages and up to 53% reduction in losses, equivalent to the improvement of the power processing efficiency of 12%.**

## I. INTRODUCTION

The power management module in a typical portable electronic device, such as a cell phone, laptop, or tablet computer, provides multiple regulated dc voltages. These voltages are supplied to various functional blocks, including digital processors, I/O interfaces, and memory devices [1]. A power management module usually consists of multiple dc-dc conversion stages connecting the input voltage source (typically a battery pack) and the functional blocks.

A conventional power management module implementation is shown in Fig.1. It consists of a front-end dc-dc converter, creating a stable intermediate bus voltage, and several downstream switch-mode power supplies (SMPS) and/or low-dropout (LDO) linear regulators providing multiple output voltages meeting specific steady state and dynamic voltage requirements [1]. In order to minimize the power losses of this two-stage conversion process, both stages are required to be very efficient.

One of the main challenges related to the implementation of the traditional power management modules is their weight and size. In numerous portable devices these modules are by far the largest contributors to the overall size and weight [2], taking a significant portion of the overall volume [3]. This is largely due to the bulky and costly reactive components of the SMPS output filters.

This work of Laboratory for Power Management and Integrated SMPS is supported by Qualcomm Inc.

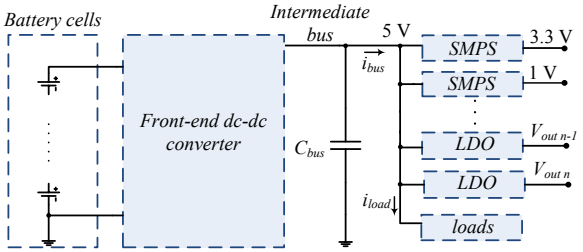


Fig.1 Conventional power management system.

A single-stage solution, based on a triple-output switched-capacitor (SC) architecture, was proposed in [2], to minimize the volume of the power management module. This architecture eliminates the need for bulky filtering inductors, which are typically the largest contributors to the overall filter volume. However, the architecture's fixed input-to-output conversion ratios do not allow its use in battery-powered applications, as the battery voltage varies with its state-of-charge. To provide tight output voltage regulation, in [4], [5] compact and power efficient solutions are presented. In these solutions, a SC fixed-ratio voltage divider is used as a front-stage to provide a bus voltage that is not regulated. This stage is followed by volume-reduced conventional dc-dc converters, providing tightly regulated outputs for the functional blocks.

This paper introduces a novel power management module architecture for battery-powered applications that allows further volume reduction of the reactive

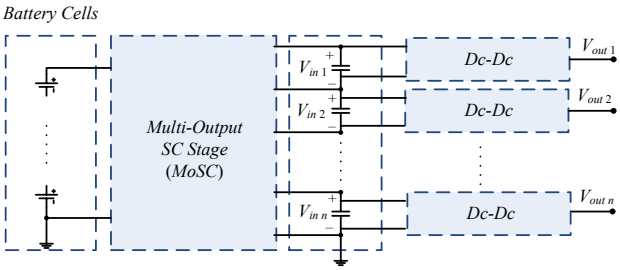


Fig.2 Multi-output SC (MoSC) based power management system.

components. In this architecture, shown in Fig.2, the front-end converter is replaced with a multiple-output SC stage (MoSC) and, instead of operating at the full bus voltage, the downstream converters, providing tightly regulated voltages, are supplied by differential output taps.

The following section shows that, in addition to eliminating the front stage inductor, this arrangement allows reducing the downstream stages' inductors drastically and improving their efficiencies significantly, by minimizing switching losses. These advantages could potentially create an opportunity for an increased level of on-chip integration of the power management modules compared to existing solutions.

The following section explains the principle of operation of the proposed power management architecture. Practical implementation is discussed in Section III, and Section IV presents experimental results verifying the proper system operation.

## II. Principle of Operation

In some low-power applications switched-capacitor (SC) converters are preferred over conventional switch-mode power supplies (SMPS) as they do not require bulky inductors, and hence can easily be implemented on integrated circuits [6]. Such SC networks operate most efficiently (around 95% [7]) at fixed input-to-output voltage ratios. However, they demonstrate significant efficiency degradation when they are required to provide a fixed output voltage as the input voltage varies [8]. The transient response of SC circuits is also inferior compared to conventional SMPS alternatives [9], making them unsuitable for applications where strict voltage regulation and transient response requirements need to be met. On the other hand, SMPS requires bulky inductors, especially in the cases when relatively large conversion ratios are required [10].

The power management architecture introduced in this paper (Fig.2) combines a multi-output switch-capacitor (MoSC) with modified dual-input buck converters [11]. The front-end SC stage operates with a fixed conversion ratio, at the peak efficiency point. The downstream buck converters providing tight regulation are connected across the individual output capacitors of the SC stage, to minimize the voltages across the converters' components, resulting in volume and loss reductions. In the following subsections, more details of the power management module operation are given through a description of the 3-output module shown in Fig.3.

### A. Triple output fixed-ratio switched-capacitor converter

In the system of Fig.3 a MoSC stage provides 2/3 and 1/3 of the battery pack voltage, $V_{batt}$ for the intermediate capacitor network. This stage is a modified version of the well-known single-output switched capacitor voltage

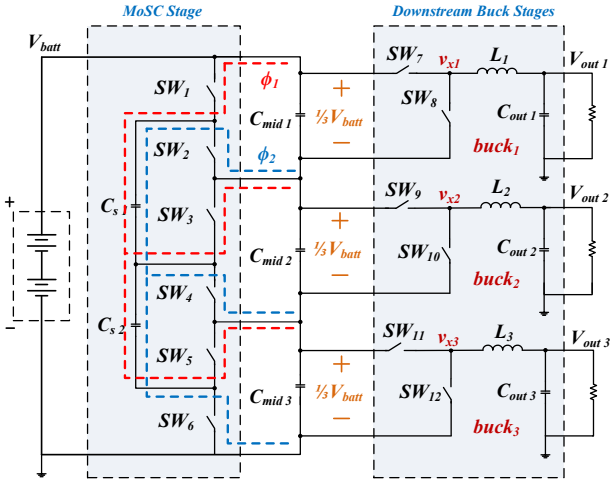


Fig.3 Triple output MoSC-based power management module.

halver [2]. This modification has two additional switches and an extra shuttling capacitor, to accommodate multiple outputs.

To maintain constant $V_{batt}/3$ voltage across all intermediate capacitors, the shuttling capacitors redistribute the charge difference through a two-phase switching sequence. In phase 1, labeled with red dashed lines, $SW_1$, $SW_3$, and $SW_5$ are turned on, to connect shuttling capacitors $C_{s1}$ and $C_{s2}$ across $C_{mid1}$ and $C_{mid2}$, respectively. Similarly in phase 2, marked with blue dashed lines, $C_{s1}$ and $C_{s2}$ are connected across $C_{mid2}$ and $C_{mid3}$ respectively, through $SW_2$, $SW_4$ and $SW_6$.

It is important to note that, compared to conventional topologies, the MoSC stage does not require significantly larger capacitance volume. The total volume of the capacitors $C_{mid1}$ to $C_{mid3}$, which is proportional to the sum of their $CV^2$ values, is approximately the same as that of $C_{bus}$ (Fig.1). The shuttling capacitors, handling just the charge difference between the outputs, have much smaller values and, thus, do not significantly contribute to the overall volume.

### B. Modified downstream buck converters

The front-end MoSC stage of this power management module does not provide regulation of the output tap voltages, in case of input voltage variation. As the battery cell voltages vary, the intermediate voltages also vary, but maintain the desired fixed ratio. In the targeted applications, this change is fairly constrained due to the limited variation exhibited by the battery pack voltage, imposed by inside-the-pack integrated protection systems preventing full discharge [12]. To compensate for the battery's state-of-charge dependent voltage variations, the MoSC stage is connected to a string of modified buck converters providing regulated output voltages, as shown in Fig.3.

Each of the converters is based on the dual-input buck concept [11] that results in a drastic reduction of the

output filter inductance value and minimization of the switching losses. In this case, the concept is extended to multiple outputs. Also, the bulky dual-output flyback converter, earlier used to provide two input voltages, is replaced with the previously described MoSC stage.

The principle of inductor minimization can be described by looking at the current ripple and duty ratio equations for a general single inductor-based converter in continuous conduction mode:

$$\Delta i_L = \frac{V_{L\_on} \cdot D}{2 \cdot L \cdot f_{sw}} = \frac{V_{L\_off} \cdot (1-D)}{2 \cdot L \cdot f_{sw}}, \qquad (1)$$

where $D$ is the duty ratio, $L$ is the inductance value, $f_{sw}$ is the switching frequency, and the values $V_{L\_on}$ and $V_{L\_off}$ the voltages across the inductor during on and off states of the main switch, respectively. In the conventional buck converter case $V_{L\_on} = (V_g - V_{out})$ and $V_{L\_off} = V_{out}$, where $V_g$ and $V_{out}$ are the input and output voltages of the converter, respectively. The most common approach to minimize the inductor value, while maintaining the same current ripple, is to increase the switching frequency [13]. However, this approach results in increased switching losses [14] and therefore, poses a fundamental limit on the inductor size reduction. In the modified buck converters of Fig.3, the inductors are reduced by minimizing $V_{L\_on}$ and $V_{L\_off}$ values. This is achieved by setting the two possible switching node ($v_{x1-3}$ of Fig.3) voltage values, i.e. the outputs of the MoSC stage, to be slightly larger and slightly smaller than the desired converter output voltage. For example, for the buck stage producing $V_{out1}$, the two possible values of $v_{x1}$ are $V_{batt}$ and $2V_{batt}/3$, where $V_{batt} > V_{out1} > 2V_{batt}/3$. This effectively reduces the voltage swings across the inductors, allowing for their minimization. Also, since the converter switches are operating with lower blocking voltages in steady state, the switching losses are reduced as well [15].

## III. Practical Implementation

Fig. 4 demonstrates a practical implementation of the introduced power management module architecture for systems supplied by two series-connected, standard 3.3 V lithium-ion cells (whose voltage typically varies between 2.7 and 3.6 V [16], [17]) and require three different outputs. The output voltages are 1 V for the digital processors, 3.3 V for analog components, and 5 V for USB ports and peripherals. Typical applications for such an architecture include tablet computers and a number of other mobile devices.

### A. Comparison with a conventional topology

The following discussion describes advantages of the introduced power management topology over a conventional system of Fig.1, where a front-end bus converter [18] provides a well-regulated 5 V intermediate bus voltage over the range of battery voltage variation. In

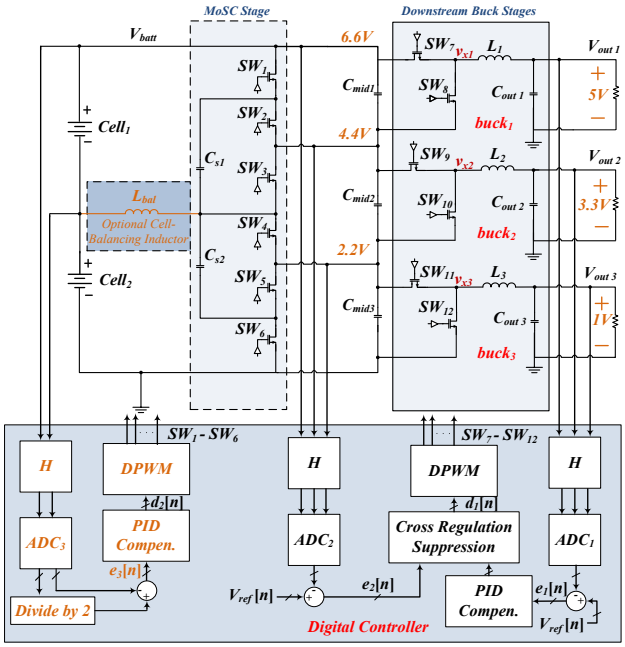


Fig.4 Practical implementation of triple-output MoSC-based power management module and its controller.

the introduced architecture, since the front-end MoSC stage does not provide voltage regulation, $buck_1$ is used to supply 5V loads, as in Fig. 4. As this dual input buck processes less power and operates with a smaller switching node voltage swing, i.e. 1/3 of $V_{batt}$, it requires a much smaller inductor. By taking into account both (1) and the fact that the volume of an inductor is proportional to the energy it stores, i.e. $0.5(LI)^2$, inductor volume reduction in $buck_1$ can be calculated. For a 6.6 V input, this inductor reduction is proportional to approximately $0.36(I_{load}/I_{bus})^2$, where $I_{bus}$ and $I_{load}$ are nominal bus and load currents respectively, for the system of Fig.1. This comparison assumes the same switching frequencies and current ripples. Since the 5 V downstream stage of the MoSC processes less power, it can potentially operate at a higher switching frequency, allowing for an even larger volume reduction [13].

Potential inductor size and switching loss reductions for the downstream stages providing 3.3 V and 1 V are demonstrated in Table I. This table shows normalized values of the switching node ($v_{x1-3}$) voltage swings

Table I: Inductor volume and switching loss reductions

| | $V_{sw\_norm}$ | $L_{\_norm}$ | $P_{sw\_norm}$ | $f_{sw\_norm}$ |
|---|---|---|---|---|
| *Dual-input buck 3.3 V* | 0.44 | 0.49 | 0.44 | 1 |
| *Dual-input buck 1 V* | 0.44 | 0.68 | 0.44 | 1 |
| *Dual-input buck 3.3 V (incr. $f_{sw}$)* | 0.44 | 0.25 | 0.88 | 2 |
| *Dual-input buck 1 V (incr. $f_{sw}$)* | 0.44 | 0.34 | 0.88 | 2 |

$v_{sw\_norm}$, inductances $L_{norm}$, and semiconductors switching losses $P_{sw\_norm}$ for the implemented topology of Fig.4, with respect to their equivalents in a conventional topology (Fig.1). For the conventional topology, the downstream SMPS buck converters operate with a 5 V swing at switching nodes, whereas in the proposed topology, the downstream stages have 2.2 V swings. This is shown in the $V_{sw\_norm}$ column of Table I. Since the currents supplied by the downstream stages in both configurations are the same, the inductor size reduction is only due to the lower voltage swing. It can be seen that significant reductions in inductor size by 51 % and 32 % can be achieved. Table I also demonstrates that this minimization is accompanied with drastic reductions in switching losses, to 44 % of the conventional value [15]. Furthermore, it also shows that, if operating at twice the switching frequencies, the MoSC based architecture can achieve inductor volume reductions that exceed 75 % while maintaining lower switching losses than the conventional counterpart.

### B. *Digital Controller*

A digital controller regulates operation of the MoSC stage and the downstream converters. A three input analog-to-digital converter ($ADC_1$), which can be implemented by three separate conversion channels or single time-shared channel for three inputs [19], is used to acquire digital equivalents of the output voltages. These voltages are then subtracted from their respective references and the corresponding errors, $e_1[n]$ are obtained. A PID regulator creates control signals for a multi-input multi-output digital pulse-width modulator (DPWM) to provide tight-regulation of the output voltages. This architecture is similar to the well-known digital controller architecture discussed in numerous publications [20], [21].

In addition, a *cross regulation suppression* module is incorporated to reduce cross-regulation problems during transients. The cross regulation between different outputs exists due to the stacked-up intermediate capacitor configuration. These intermediate capacitors serve as input filters for the downstream stages and hence, transients at the outputs create charge imbalance in this capacitors. In order to mitigate this problem, a feed-forward based approach [22], [23] is utilized, where $ADC_2$ is used to acquire information regarding the intermediate capacitor voltages during transients. Based on this information, the cross regulation suppression block adjusts the instantaneous duty ratio values such that the cross regulation problem is minimized. The effectiveness of the *cross regulation suppression* module is shown in the experimental results section of this paper.

### C. *Incorporating a cell balancing feature*

The cell balancing feature is incorporated in the topology in a very simple manner, by adding a single inductor, $L_{bal}$ (Fig.4). In normal operation, the right side of the inductor (Fig.4), i.e. its switching node, ideally switches between $2/3V_{batt}$ and $1/3V_{batt}$ with a 50 % phase duration, due to the regular operation of the SC circuit. Therefore, in steady state, the left side of the inductor will be forced to be at $1/2V_{batt}$, which is the average switching node voltage. As a result, in the ideal case, the normal operation of the MoSC stage would force the battery cells to be balanced. However, if a cell imbalance is observed, a slight variation of switch cap phase duration from the regular 50 % value is applied without significantly affecting the intermediate capacitor voltages. This is possible as tight regulation in the intermediate nodes is not required for proper system operation. As shown in Fig.4, $ADC_3$ provides information regarding the battery voltages and this information is used to adjust the duration of the gating signal phases for $sw_{1\text{-}6}$, providing battery cell balancing.

In addition, the cell balancing inductor provides bi-directional energy transfer between the battery cells and intermediate capacitors, through the shuttling capacitors. In the event of unbalanced loads at the outputs, i.e. different load currents taken from different output voltages, the intermediate capacitors and hence, the shuttling capacitors might show charge imbalance. In the presence of $L_{bal}$ this imbalance is minimized as the bidirectional energy transfer allows maintaining equal charge in the shuttling capacitors while balancing battery cells. Furthermore, in the absence of $L_{bal}$, the energy to the output of *buck3* is transferred to $C_{mid3}$ via $C_{s1}$ and $C_{s2}$, whereas $L_{bal}$ creates a direct path from the battery cell to $C_{mid3}$ through $C_{s2}$. As a result, $L_{bal}$, while providing the cell balancing feature, also helps equal charge distribution in the MoSC stage and improves system efficiency.

## IV. Experimental System and Results

Based on the diagram of Fig.4 an experimental system was developed using discrete components and a FPGA-

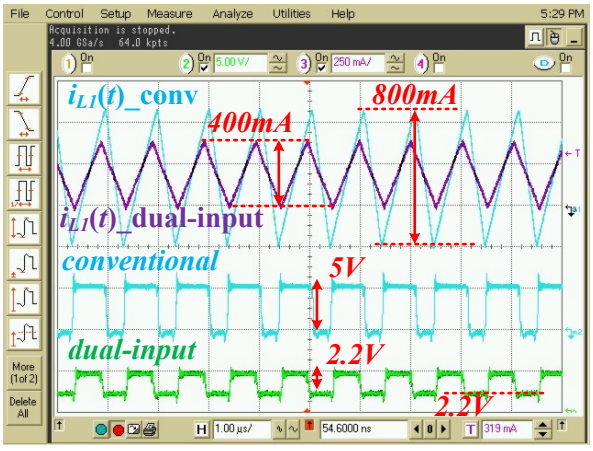


Fig.5 Inductor currents and switching node voltages of the conventional and MoSC-based dual-input downstream stage for 3.3 V output. Ch2: switching node, $v_{x2}$ (5 V/div); Ch3: inductor current (250 mA/div).

based controller implementation. Three stacked buck converters are connected differentially across the intermediate capacitor string. The MoSC stage provides the node voltages of the capacitive string. For two 3.3 V Li-ion battery cells, these voltages are approximately 6.6 V, 4.4 V and 2.2 V. The MoSC stage operates at a fixed frequency of 500 kHz while the downstream stages, providing 5 V/ 3 W, 3.3 V/ 9 W and 1 V/ 3 W, switch at 1 MHz. The characteristics of the MoSC based system functional blocks are compared to those of conventional downstream buck stages operating from a 5 V bus and providing the same outputs.

Figs. 5 and 6 show comparisons of the inductor currents and switching node voltages of the conventional and MoSC-based dual-input downstream stages when providing 3.3 V and 1 V at their outputs, respectively. For demonstration purposes the inductors of both configurations are selected to be the same. The results demonstrate lower switching node voltage swing, and consequently, about 50% lower inductor current ripple for the 3.3 V dual-input buck of the MoSC-based architecture, allowing for the same percentage of inductor volume reduction. For the 1 V output, this reduction is about 30 %.

### *A. System efficiency*

Fig.7 shows measured efficiency comparison of the conventional and dual-input downstream buck converters providing a 1 V output over a 250 mA to 3 A load variation. For the conventional case, the buck converter operates from a 5 V bus voltage, whereas in the proposed topology it operates from the 2.2 V intermediate capacitor voltage. The results confirm up to 53% reduction in total losses, improving the overall efficiency by 12% at light loads, where the switching losses are dominant, as well as a noticeable improvement throughout the entire operating range.

Fig. 8 shows the measured efficiency of the proposed MoSC front-stage, along with combined MoSC and downstream buck efficiency for 1 V output. The MoSC stage in the experimental prototype was developed with discrete components and shows above 90% efficiency for 0.25 A to 3A output current. In the case of an integrated switched-capacitor front-stage this efficiency is expected to be higher. As shown in Fig.8, a relatively flat efficiency curve of the MoSC stage is the key for overall high system efficiency.

### *B. Minimizing cross regulation between outputs*

Fig.9 shows the cross regulation issues discussed in the practical implementation section of this paper. The stacked configuration of the intermediate capacitor network inherently imposes this problem. As shown in Fig.9, due to a transient at any buck converter output (marked with red circles), sub-transient responses at two other outputs can occur.

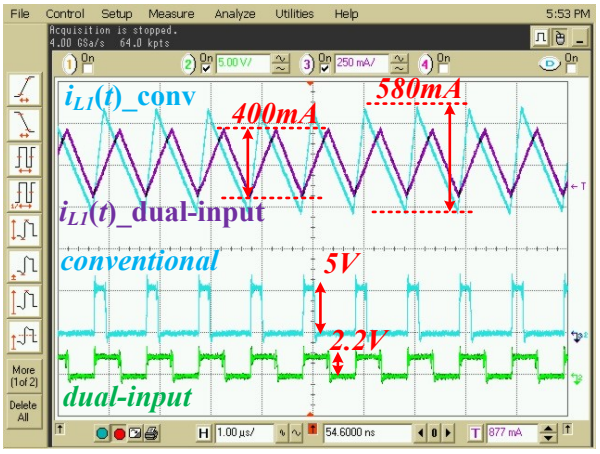


Fig.6 Inductor currents and switching node voltages of the conventional and MoSC-based dual-input downstream stage for 1 V output. Ch2: switching node, $v_{x3}$ (5 V/div); Ch3: inductor current (250 mA/div).

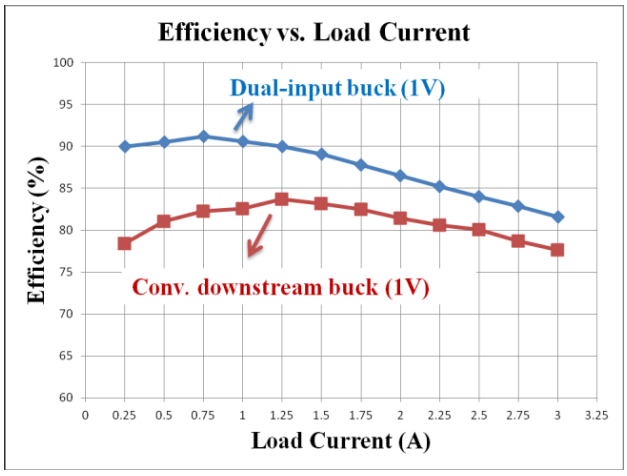


Fig.7 Efficiency comparisons of the MoSC based dual-input buck architecture and the conventional downstream converter.

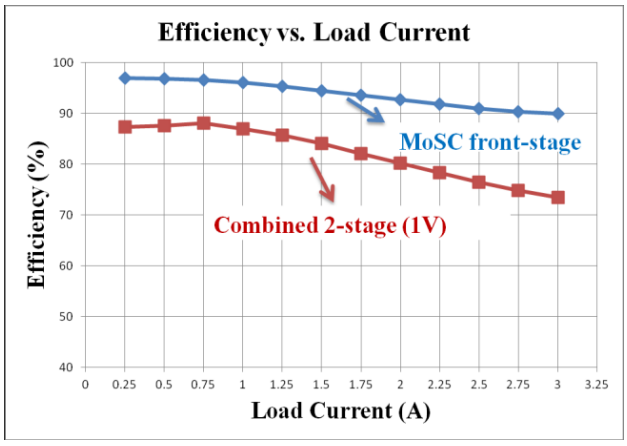


Fig.8 Measured efficiency of MoSC front-stage alone and combined 2-stage, from battery source to 1V output, of the proposed architecture.

The digital controller of Fig.4 reduces the effects of the cross regulation by utilizing a feed-forward architecture. When the centralized controller detects a transient in one of the buck output voltages, it utilizes the feed-forward information to adjust the duty ratios of the other two buck stages, to minimize their sub-transients. The effectiveness of the cross regulation suppression control-action during a light-to-heavy transient at 1V output is shown in Fig.10. The proposed solution allows limiting the sub-transient responses to 20 mV deviation.

### C. *Cell balancing using $L_{bal}$*

Fig.11 demonstrates how battery-cell balancing is performed, while regulating the output voltages, for the case when the top cell has a larger state-of-charge than the bottom one. To show the effect over a relatively short period two 5 F ultra capacitors, having much smaller capacity than conventional battery cells, are used. An initial large mismatch between the capacitors was created to demonstrate the effectiveness of the proposed cell balancing feature. It can be seen that by slightly changing the SC duty ratio from its 50% nominal value, the initial imbalance between $V_{batt1}$ and $V_{batt2}$ is effectively eliminated. Fig.11 also shows how the output voltage is perturbed during this operation. However, it is important to note here that, such a large mismatch (~1V) would not occur during the normal system operation and hence, the balancing would be performed without creating any disturbance at the outputs.

## V. CONCLUSIONS

A low-volume power management architecture for battery powered applications is introduced. To achieve reduced inductor volume and improved efficiency, the front-end buck converter stage existing in conventional systems is replaced with an inductor-less fixed-ratio multi-output switch-capacitor (MoSC) converter. The MoSC stage is followed by a string of modified dual-input downstream buck converters having lower volume and smaller switching losses than their conventional counterparts. The advantages of the new architecture are experimentally verified.

## REFERENCES


[1] P. Henry, "New Advances in Portable Electronics," in *APEC Plenary Session*, March 2009.

[2] P. Kumar, and W. Proefrock, "Novel switched capacitor based Triple Output Fixed Ratio Converter (TOFRC)," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp.2352-2356.

[3] Y. Kaiwei, "High-frequency and high-performance VRM design for the next generations of processors," Ph.D. thesis, Virginia Polytechnic Institute and State University, 2004.

[4] M. Xu, J. Sun, and F.C. Lee, "Voltage divider and its application in the two-stage power architecture," in *Proc. Applied Power Electronics Conference and Exposition(APEC)*, 2006, pp. 7.

[5] J. Sun, M. Xu, Y. Ying, and F.C. Lee, "High Power Density, High Efficiency System Two-stage Power Architecture for Laptop


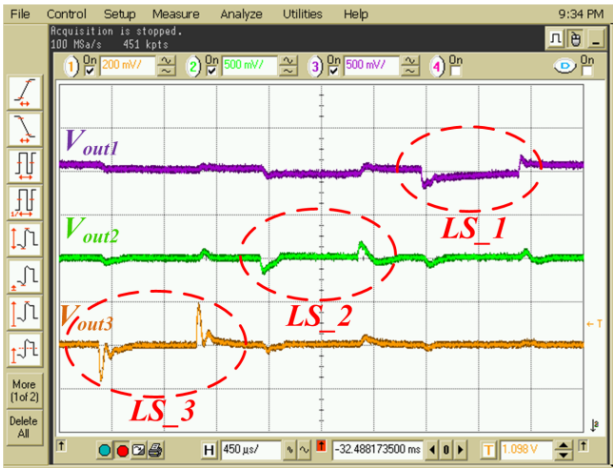


Fig.9 Cross regulation between output voltages. Actual load steps are marked in red dotted circles (*LS_1* to *LS_3*). Ch1: $buck_3$ output voltage, $V_{out\ 3}$ (200 mV/div); Ch2: $buck_2$ output voltage, $V_{out\ 2}$ (500 mV/div); Ch3: $buck_1$ output voltage, $V_{out\ 1}$ (500 mV/div).

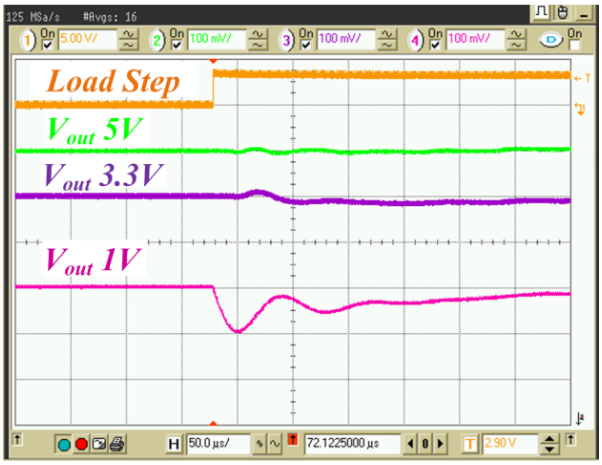


Fig.10 Significant suppression of cross regulation problem. Ch1: load step signal; Ch2: $buck_1$ output voltage, $V_{out\ 1}$ (100 mV/div); Ch3: $buck_2$ output voltage, $V_{out\ 2}$ (100 mV/div); Ch4: $buck_3$ output voltage, $V_{out\ 3}$ (100 mV/div).

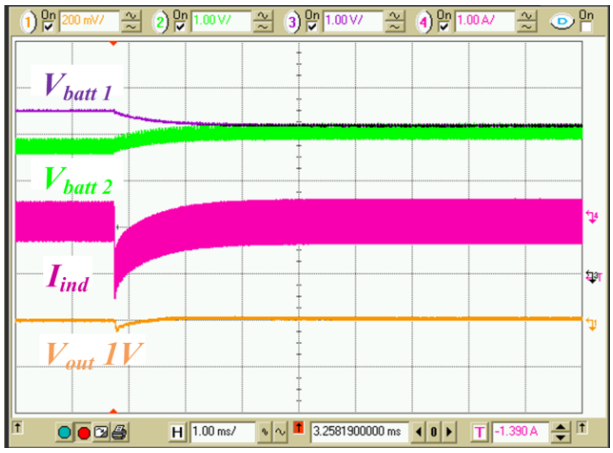


Fig.11 Performing battery cell balancing while regulating the output voltage. Ch1: $buck_3$ output voltage, $V_{out\ 3}$ (200 mV/div); Ch2: bottom battery cell voltage (1 V/div); Ch3: top battery cell voltage (1 V/div); Ch4: current of the cell balancing inductor, $L_{bal}$ (1 A/div).

Computers," in *Proc. Power Electronics Specialists Conference (PESC)*, 2006, pp.1-7.

[6] H.-P. Le, M. Seeman, S.R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," in *Proc. Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2010, pp.210-211.

[7] T. Santa, M. Auer, C. Sandner, and C. Lindholm, "Switched capacitor DC-DC converter in 65nm CMOS technology with a peak efficiency of 97%," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp.1351-1354. [8] S. Ben-Yaakov, and A. Kushnerov, "Algebraic foundation of self adjusting Switched Capacitors Converters," in *Proc. Energy Conversion Congress and Exposition,* 2009, pp.1582-1589.

[8] S. Ben-Yaakov, and A. Kushnerov, "Algebraic foundation of self adjusting Switched Capacitors Converters," in *Proc. Energy Conversion Congress and Exposition,* 2009, pp.1582-1589.

[9] B. Maity, G. Bhagat, and P. Mandal, "Fast transient frequency control voltage regulator using push-pull dynamic leaker circuit," in *Proc. India International Conference on Power Electronics (IICPE)*, 2010, pp.1-6.

[10] B. Mahdavikhah, P. Jain, and A. Prodic, "Digitally controlled multi-phase buck-converter with merged capacitive attenuator," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp.1083-1087.

[11] J. Sebastian, P.J. Villegas, F. Nuno, and M.M. Hernando, "High-efficiency and wide-bandwidth performance obtainable from a two-input buck converter," *IEEE Transaction on Power Electronics*, vol.13, no.4, pp.706-717, Jul 1998.

[12] D. H. Lu, N. Fujishima, A. Sugi, M. Sugimoto, S. Matsunaga, M. Sawada, M. Iwaya, and K. Takagiwa, "Integrated Bi-directional Trench Lateral Power MOSFETs for One Chip Lithium-ion Battery Protection ICs," in *Proc. Power Semiconductor Devices and ICs(ISPSD)*, 2005, pp.355-358.

[13] R. W. Erickson and D. Maksimović, "Fundamentals of Power Electronics", Second Edition, New York: Springer Science+ Business Media, 2001.

[14] S. M. Ahsanuzzaman, A. Radić, and A. Prodić, "Adaptive switching frequency scaling digital controller for improving efficiency of battery powered dc-dc converters," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp.910-915.

[15] J. Klein, "Synchronous buck MOSFET loss calculations with Excel model". Application note AN–6005, Fairchild Semiconductor, version 1.0.1, April 2006.

[16] H.A.-H. Hussein, and I. Batarseh, "State-of-charge estimation for a single Lithium battery cell using Extended Kalman Filter," in *Proc. IEEE Power and Energy Society General Meeting*, 2011, pp.1-5.

[17] C. Kallfab, C. Hoch, A. Hilger, and Manke, I., "Short-circuit and overcharge behaviour of some lithium ion batteries," in *Proc. International Multi-conference on Systems, Signals and Devices (SSD)*, 2012, pp.1-5.

[18] B. Soderberg, and T. Bussarakons, "Compatibility analysis of space qualified intermediate bus converter and point of load regulators for digital loads," in *Proc. 8th European Power Conference*, 14-19 September, 2008.

[19] D. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, 1997.

[20] A. Stupar, Z. Lukić, and A. Prodić, "Digitally-controlled steered-inductor buck converter for improving heavy-to-light load transient response," *in Proc. IEEE PESC conf*, 2008.

[21] Z. Lukic, N. Rahman, and A. Prodic, ―Multibit Σ–Δ PWM Digital Controller IC for DC–DC Converters Operating at Switching Frequencies Beyond 10 MHz,‖ in *IEEE Transaction on Power Electronics*, vol. 22, no.5,pp.1693-1707, 2007.

[22] L. Calderone, L. Pinola, V. Varoli, "Optimal feed-forward compensation for PWM DC/DC converters with 'linear' and 'quadratic' conversion ratio," *IEEE trans*, *Power Electron*., vol.7, No.2, pp.349-355, Apr. 1992.

[23] B. Arbetter and D. Marksimovic, "Feedforward Pulse Width Modulators for Switching Power Converters," *IEEE trans*, *Power Electron*., vol.12, No.2, pp.361-368, Mar. 1997.