# Digitally Controlled Low-Harmonic Rectifier Having Fast Dynamic Responses

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***Abstract*** **– This paper describes a completely digitally controlled low-harmonic rectifier. It is shown that the dynamics of the outer voltage loop can be significantly improved using a digital notch filter. Low input current harmonics and fast voltage response are experimentally verified using a 200W universal-input boost power supply operating at the switching frequency of 200KHz.**

## I. INTRODUCTION

Digital controllers offer advantages over analog controllers such as flexibility, additional processing options, low sensitivity to external influences (aging, temperature variation) and less expensive manufacturing. In the past, digital controllers were considered slower than analog controllers. Also, digital control was restricted to relatively high-power applications owing to high cost of digital signal processors. In recent years use of digital controllers is increasing even in low-to-medium power applications [1-7].

The purpose of this paper is to describe a simple and efficient method for implementation of a digital controller for a PFC (power factor correct) rectifier that exhibits very low harmonic distortion of the input current and extended bandwidth of the outer voltage loop. As a test bed an evaluation board based on Analog Devices processor ADMC401 [8] was used for implementation. This structure shows that a complete controller can be implemented with a fairly simple dedicated hardware structure based on 8-bit digital arithmetic.

A typical power-factor-corrected rectifier based on a boost converter is shown in Fig.1. Current loop is designed so that the converter input current follows the waveform of the input voltage. In the ideal case these two waveforms have the same waveshape and are in phase: thus the rectifier presents a resistive load to the system. The outer loop regulates the voltage across the energy-storage capacitor. This voltage always has ripple at twice the line frequency $2\omega_L$. To maintain low input current harmonics output of the voltage regulator *u(t)* must not have significant line frequency harmonics [9]. Consequently, to avoid distortion of the ac line current through feedback, the capacitor voltage ripple in conventional designs the bandwidth of the voltage loop is limited to frequencies significantly lower than the line frequency (typically 10-20Hz).

In Section II design of a high-performance digitally-controlled PFC rectifier that provides very low distortion of input current is described.

Section III presents a technique that improves transient response of the output voltage. Several approaches to improving the dynamic response of the voltage loop in analog PFC controllers have been proposed [10-13]. The method presented here is based on implementation of a digital notch filter in the feedback loop. Additionally, the problem of the controller design to obtain fast voltage loop is addressed.

Finally, experimental results and conclusions are given.

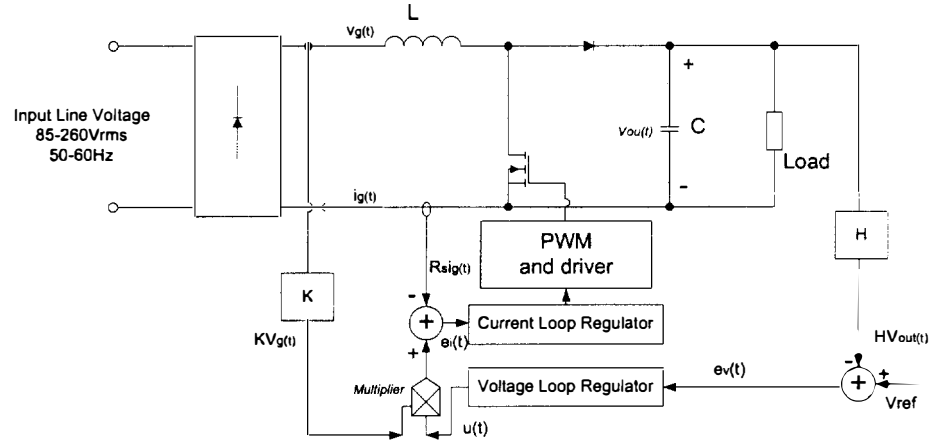


Fig.1. PFC rectifier based on a boost converter

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## II. DIGITAL PFC CONTROLLER

Fig.2 shows the block diagram of a complete digital controller for a 200 W boost-based PFC operating in continuous conduction mode at a switching frequency of $f_s = 1/T_s = 200$ kHz. It is designed for universal input (ac line voltage between 85 and 260 V,rms) and the DC output voltage is regulated at 385 V.

*Selection of switching frequency and resolution of digital pulse width modulator (DPWM)*

In the design of digital controllers for switching converters, a trade off exists between resolution of the digital pulse width modulator (DPWM) and the operating frequency. To obtain smaller components and faster control, it is desired to operate the converter at higher switching frequency. As the switching frequency increases, the resolution of a conventional DPWM whose design is based on a counter decreases [8]. This type of DPWM is often used for digital control of switching converters. Hence, to maintain good resolution of the DPWM, the switching frequency is usually restricted to low values.

In this design we decided to use a DPWM whose resolution is only 6 bits. This choice allows operation at a high switching frequency, with consequent implementation of a high-bandwidth current regulator using a simple computational unit.

In the prototype system, 8-bit arithmetic for the computational unit and analog-to-digital converters is used; this choice contributes to our objective of implementing a high-performance PFC using relatively simple hardware structure.

*Selection of sampling instant*

The input current and input voltage are sampled at the switching frequency. To avoid sampling the noise around the transition, and to obtain values approximately equal to the average of input current during one switching cycle the sampling instants are selected using adjustable delay $t_D$ from the time when the switch is turned on. This delay depends on the current discrete duty cycle value $d[n]$ as follows:

$$t_D = \frac{d[n]}{2} \cdot T_s \quad \text{if } d[n] \geq 0.5 \text{ and} \tag{1}$$

$$t_D = \frac{1-d[n]}{2} \cdot T_s \text{ if } d[n] < 0.5$$

*Current loop regulator design*

To find dependence of the input current on the control variable (duty cycle variation $d(t)$,

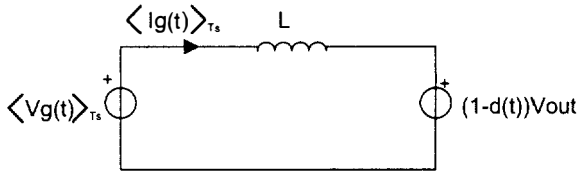


Fig.3 Linearized model describing boost converter input characteristics

the average model of Fig.3 is employed [14]. This model predicts that control-to-input-current transfer function is

$$\frac{\hat{i}_g(s)}{\hat{d}(s)} = \frac{V}{sL} \tag{2}$$

where V is the output capacitor voltage.

The current loop regulator design is based on digital redesign, using the poles-zeroes matched transformation technique [15].

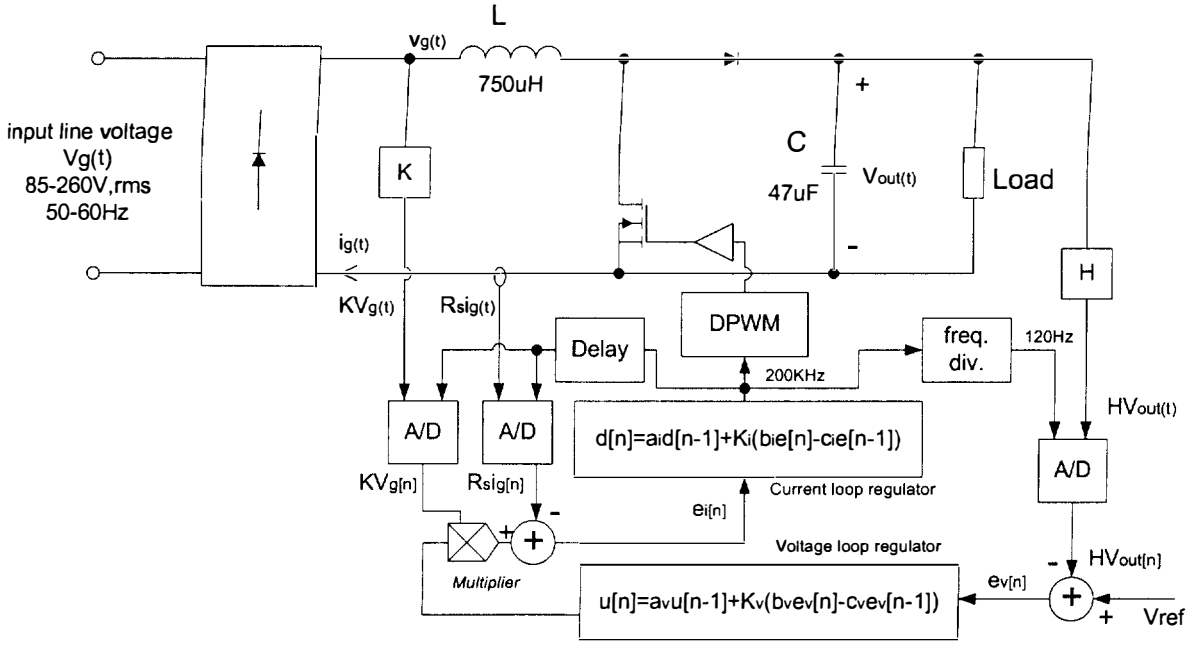


Fig.2. Completely digitally controlled low-harmonic rectifier

It was found that the digital PI regulator can be described with following discrete-time control law:

$$d[n] = d[n-1] + 0.875\left(e_i[n] - 0.85e_i[n-1]\right) \quad (3)$$

Magnitude and phase asymptotes of the system with implemented controller are given in Fig.4.

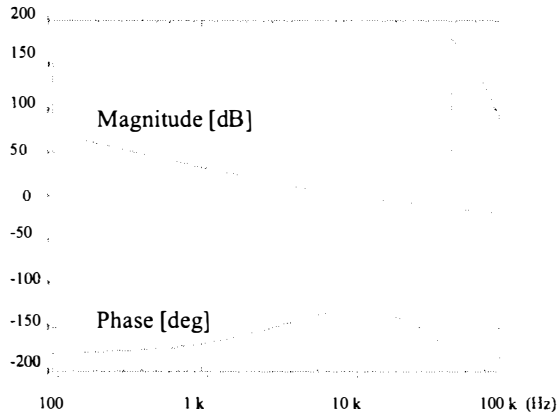


Fig.4 Magnitude and phase asymptotes of the loop gain

It can be seen that applied digital regulator provides sufficient phase margin (about 45°) and a crossover frequency of 12KHz.

*Design of a low-bandwidth voltage loop*

The current loop regulator forces the input current to follow the input voltage waveshape, and as the result the input port of an ideal rectifier behaves as an emulated resistor *Re*. The power apparently "consumed" by this emulated resistor is actually transferred to rectifier DC output. Based on this, the equivalent model of the ideal rectifier is derived [14] and illustrated in Fig.5.

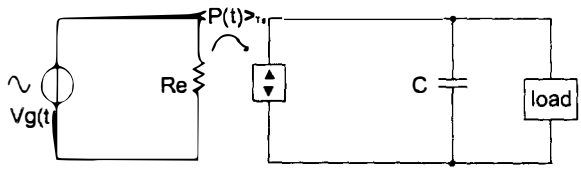


Fig.5 Equivalent circuit of the ideal low-harmonic rectifier

In this model, the output port is represented with a controllable power source. If the input voltage is sinusoidal, the instantaneous power delivered to the power source $p_{ac}(t)$ is

$$p_{ac}(t) = \frac{2V_{g,rms}^2}{R_e}\sin^2(\omega_L t) = \frac{V_{g,rms}^2}{R_e}\left(1 - \cos(2\omega_L t)\right) \quad (4)$$

As the result, the voltage across the output energy-storage capacitor must have ripple at $2f_L$, where $f_L$ is the line frequency.

To regulate the output voltage, additional feedback is needed. This feedback cannot attempt to remove the capacitor voltage ripple at the second harmonic of the line frequency; the capacitor must be allowed to store and release energy as necessary to interface the pulsating power of the single-phase ac input to the constant power drawn by the dc load. Removal of the second-harmonic voltage through feedback would cause constant distortion of the reference for the input current signal, and would consequently create serious distortion of the ac line current.

For the voltage loop digital controller presented in Fig.2, concept described in [9,16] based on sampling at twice the line frequency is used. Sampling at this frequency provides filtering of the second harmonic component. This low sampling frequency also limits the bandwidth of the voltage loop to frequencies lower than the ac line frequency.

To design regulator for the voltage loop of the system shown in Fig.2 low frequency model, based on the averaging over a half of the line period [14] was used. As a result, the following control-to-output transfer function was derived.

$$\frac{\hat{v}(s)}{\hat{u}_c(s)} = \frac{V_{out}}{2 \cdot U \cdot H} \frac{1}{1 + sC\frac{R_{out}}{2}} \quad (5)$$

where $U$ is the steady-state value of the control variable at the output of the voltage regulator.

Using the digital redesign method again, we designed a slow PI regulator that provides 20Hz bandwidth.

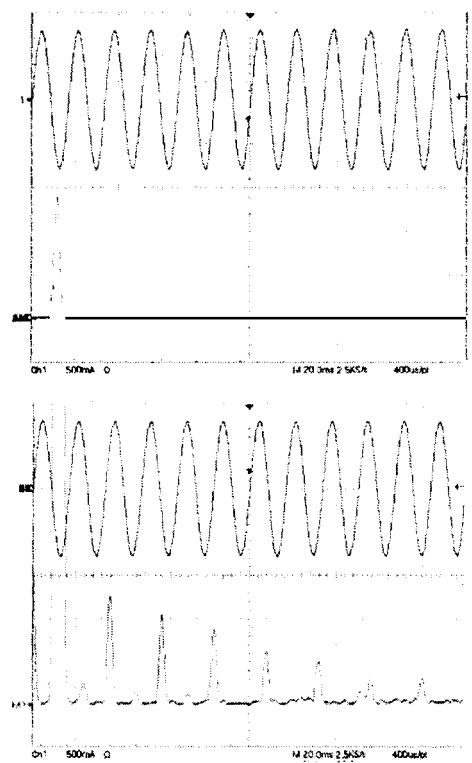

Fig.6 Input current waveform (500 mA/div) and its harmonic content.
Top: Spectrum 200 mA/div.
Bottom: Magnified view of the spectrum, 1 mA/div.

The discrete control law of this regulator is

$$u[n] = u[n-1] + 8(e_i[n] - 0.275e_i[n-1]) \quad (6)$$

In the experimental system based on the diagram in Fig.2: THD of the input current below 3%, and unity power factor over universal input range (85-260$V_{rms}$) were measured. The input current waveform and its harmonic content are shown in Fig.6. From the measurements it can be seen that amplitudes of higher harmonics are negligible in comparison with the fundamental.

## III. DIGITAL CONTROLLER WITH IMPROVED VOLTAGE DYNAMIC RESPONSE

Because of the low bandwidth of the output voltage feedback loop, components within the rectifier and downstream converter must be designed to handle substantial transients in the capacitor voltage induced by low current or ac line voltage transients. Voltage dips can cause loss of regulation in downstream converters or reduced hold up time, while over-voltages require increased voltage rating of energy storage capacitor and other elements. These issues require that conventional designs operate over an increased dynamic range leding to increased cost and reduced efficiency.

A faster voltage loop would provide smaller variations of the output voltage, and consequently greater optimization of the design of the low–harmonic rectifier and following stages. As shown bellow, these benefits can be realized through use of a digital notch filter.

*Digital notch filter*

The characteristics of the ideal notch filter are:

- Infinite attenuation at the center frequency
- Unity gain at all other frequencies
- No influence on phase of the signal
- Insensitive to external influences

Fig.7 shows the equivalent circuit of a low-harmonic rectifier that incorporates the notch filter in the voltage loop. The attenuated output voltage is compared with a reference voltage to generate the following error signal:

$$e(t) = HVout(t) - Vref \quad (7)$$

The output voltage *Vout(t)* can be expressed as the sum of voltage ripple at the second harmonic of the line frequency and the remaining component $V_1(t)$:

$$Vout(t) \approx V_1(t) + \frac{Pload}{2\omega CV_{C,rms}}\sin(2\omega_L t + \varphi) \quad (8)$$

For the case when the center frequency of the notch filter is equal to the second harmonic of the line frequency, the component at the frequency of $2\omega_L$ is eliminated and signal $e_1(t)$ contains only the difference between the reference voltage and $HV_1(t)$

$$e_1(t) = Vref - HV_1(t) \quad (9)$$

Equation (9) shows that the emulated resistance *Re* is not influenced by the second harmonic of the line frequency. Therefore, the bandwidth of thevol tage loop can be expanded to frequencies higher than $2f_L$.

It is difficult to implement an ideal notch filter that satisfies characteristics listed above, using an analog structure [9]. Reasons for this include variations of the component values caused by change of temperature, aging, tolerance of component values, and non-ideal characteristics of physical components.

The discrete transfer function of a digital notch filter [17] is given by:

$$H(z) = b_0 \frac{1 - 2\cdot\cos\omega_0 z^{-1} + z^{-2}}{1 - 2r\cdot\cos\omega_0 z^{-1} + r^2 z^{-2}} \quad (10)$$

Discrete center frequency $\omega_0$ is defined as

$$\omega_0 = 2\pi\frac{f_0}{f_{sv}} \quad (11)$$

where $f_0$ is the filter center frequency $(2f_L)$, $f_{sv}$ is the sampling frequency of the output voltage and parameter $r$ varies in the range $0 < r < 1$.

Magnitude and phase characteristics of the filter for several values of the parameter $r$ are given in Fig.8. It can be seen that for higher values $r$, the characteristics of the filter approach those of an ideal notch filter.

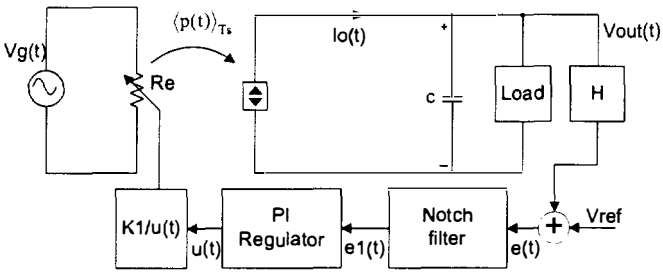


Fig.7. Equivalent circuit of low-harmonic rectifier with notch filter implemented in the voltage loop

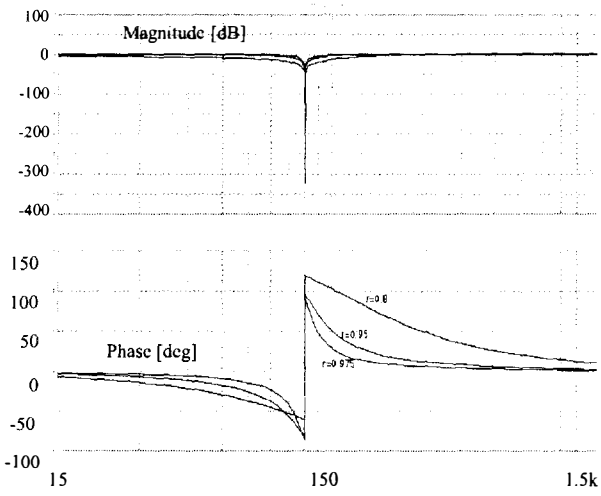


Fig.8 Magnitude (top) and phase characteristic (bottom) of the digital notch filter

*Filter implementation*

To implement the filter of Eq.(10), the output voltage sampling frequency is selected based on two considerations:

- The objective to increase the voltage loop bandwidth,
- Limitation of the achievable values of the filter and controller parameters imposed by the use of the 8-bit fixed-point processing

In the prototype system with the notch filter inserted before the voltage loop regulator (Fig.9), the sampling frequency is 4 kHz, the center frequency 120 Hz and $r = 0.975$. The resulting notch filter transfer function is

$$H(z) = \frac{1 - 1.96z^{-1} + z^{-2}}{1 - 1.91z^{-1} + 0.9502z^{-2}} \qquad (12)$$

*Design of a high-bandwidth voltage loop*

Using Eq. (4), we can see that is possible to separate the power source into two sources as shown in Fig. 9. The instantaneous powers of both of these sources depend on the time-varying value *u(t)*, which controls the emulated resistance *Re*.

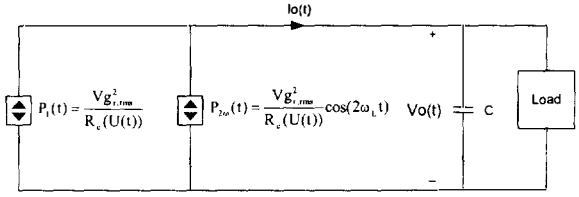


Fig.10 Equivalent circuit of the output port for high-bandwidth voltage loop

Although the component at the second harmonic frequency is eliminated by the filtering of the digital notch filter, we can see that, in a wide-bandwidth voltage loop, components at frequencies higher than $2f_L$ will be created due to fast change of emulated resistance. One consequence of the wide-bandwidth of the control system is that the low frequency models [14], traditionally employed in design of low-frequency voltage loops, cannot be employed here. Moreover, Fig.10 shows that, for the higher bandwidth, this circuit behaves as non-linear, time-varying system and hence the tools of conventional control theory developed for linear time-invariant systems cannot be used.

To implement the regulator with minimal hardware structure we decided to use a single non-adjustable structure that provides fast response on load transient.

The regulator is designed to provide bandwidth between 120Hz and 240Hz for the worst case in the circuit, where the worst case was considered to be the moment when, the instantaneous input power and output load have maximum values. The resulting regulator is described with following discrete control law:

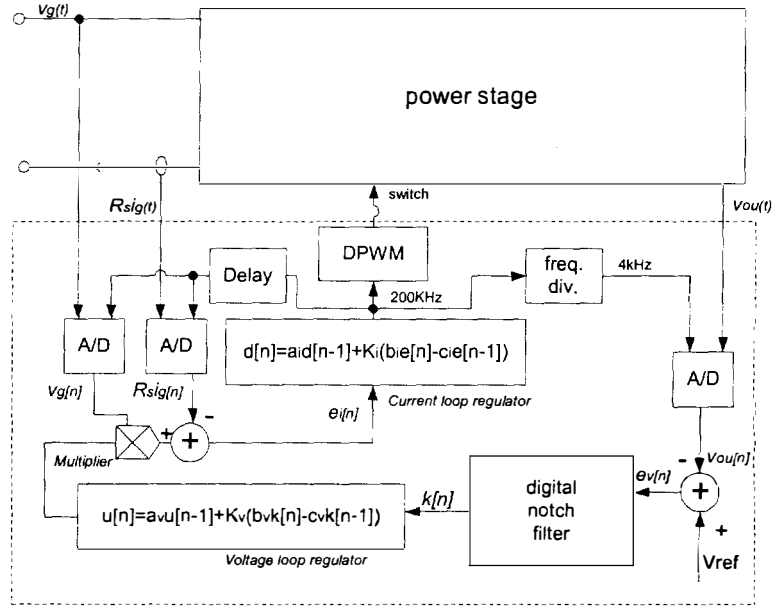


Fig.9. Digital controller with a notch filter and wide-bandwidth voltage regulator

$$u[n] = u[n-1] + 0.875\left(e_i[n] - 0.9685e_i[n-1]\right) \quad (13)$$

In this example, the bandwidth of the voltage loop was limited to 240Hz, due to constant presence of $4^{th}$ and higher harmonics in the reference for input current.

## IV. TEST SYSTEM AND EXPERIMENTAL RESULTS

The experimental system was designed around an ADMC-401 DSP [8], which offers higher performance than needed for controller implementation described in Sections II and III. In the prototype realization, we purposely limited resolution of A/D, DPWM and performed all processing in fixed-point, 8-bit arithmetic to show it would be possible to realize system using even simpler lower cost hardware.

Fig. 11 shows step load (100W to 200W) load transient response measured for two cases: a) with the prototype that has standard, slow voltage loop as described in Section II, and b) with the notch filter and redesigned voltage regulator as described Section III. It can be observed that filter implementation yields significantly improved dynamic response.

Fig.12 compares input current harmonic for the wide-bandwidth voltage loop with and without digital notch filter. Without notch filter wide-bandwidth voltage regulator results in significant input current harmonic distortion (THD of more than 20%), while with the notch filter input current THD is about 4.3%.

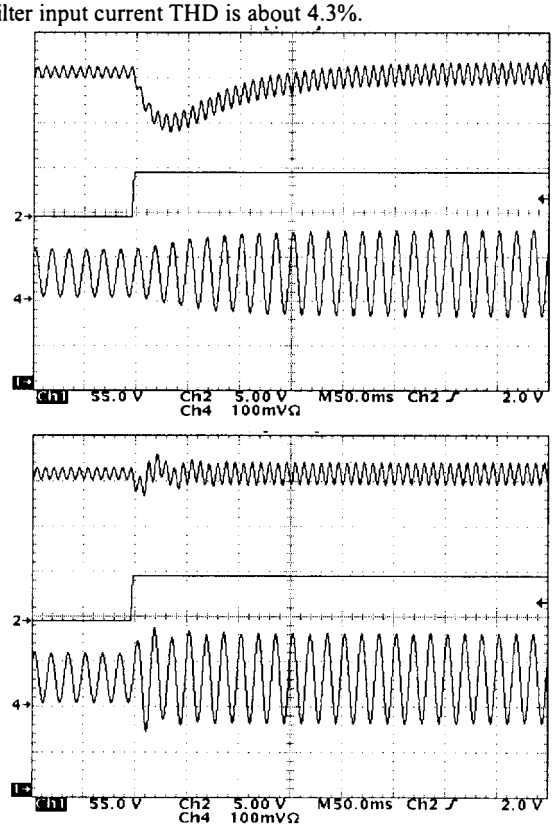


Fig.11. Transient response for the change of load from 100W to 200W, with a standard voltage loop with crossover frequency of 20Hz (top) and for the expanded bandwidth loop with the notch filter (bottom). Ch.1 – output voltage, Ch-2 load transient, Ch-4 input current

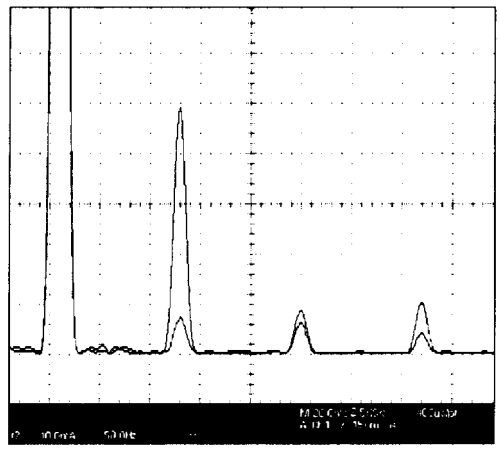

Fig.12.Harmonic content (1st-7th harmonics) of the input current with wide-bandwidth voltage regulator: (1) without the notch filter, THD > 20%, and (2) with the notch filter, THD < 5%.

## V. CONCLUSIONS

This paper describes the practical design of a high-quality low-harmonic rectifier using relatively simple digital control hardware. It is shown how the output voltage dynamic response can be significantly improved by adding a digital notch filter in the feedback loop. Improved voltage loop dynamics potentially enables the use of smaller tank capacitor at the output, operation at a smaller output voltage, and use of smaller, not over-designed components in the following dc/dc converter stage. Low input current harmonics and fast load transient response are experimentally verified on a 200 W boost high power factor rectifier.

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