LOW-VOLUME STACKABLE FLYBACK CONVERTER WITH NEAR MINIMUM DEVIATION CONTROLLER

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***Abstract*— This paper introduces a flyback-based low-volume modular converter and complementary mixed-signal controller that provide input voltage and output current sharing as well as near optimal transient response. This serial-input parallel-output switch-mode power supply (SMPS) is well suited for high-step down ratio applications where, compared to a conventionally used multi-phase buck, it requires a smaller output filter volume, lower MOSFET blocking voltages, and provides better dynamic response. The stackable flyback also has better power processing efficiency and provides inherent passive current sharing. These advantages are achieved by utilizing low-voltage flyback cells and a novel implementation of minimum deviation control method.**

Experiments with a 12-to-1-V, 4-A, 500kHz 2-cell stacked flyback converter prototype show that, compared to an equivalent 12-V 2-phase conventional buck with approximately the same inductor volume, the introduced converter has 14% smaller output capacitor, up to 40% lower power losses, and 33% faster transient response.

I. INTRODUCTION

The miniaturization of switch-mode power supplies (SMPS) is of a key importance for volume and price-sensitive electronic applications. In these applications, to reduce a relatively high internal bus voltage to low voltage levels, required by digital processors, multi-phase buck converters with a limited controller bandwidth [1] are usually used. The multi-phase buck solutions provide effective voltage regulation but, at the same time, their reactive components take a significant amount of the overall device volume and printed circuit board (PCB) area.

To minimize the volume of the reactive components a number of solutions have been proposed [2]-[4] as alternatives to the conventional multi-phase buck. Arguably, among the most interesting are the switched capacitor (SC) [2] and the multi-level buck (MLB) based solutions [3, 4]. Compared to the conventional buck, the SC converters utilize lower-voltage switches, smaller reactive components and provide improved efficiency over a certain conversion range. However, the absence of the inductor that stores energy during voltage and load variations [5] affects power processing efficiency and output voltage regulation. The MLB achieves miniaturization of its output reactive components with the introduction of a voltage attenuating capacitor [3, 4] minimizing inductor voltage swing and components stress. However, those solutions require larger number of switches and high side gate drivers making their integration challenging.

The main goal of this paper is to introduce stacked flyback converter with near minimum deviation controller of Fig. 1 that, compared to the conventional multi-phase buck solutions,

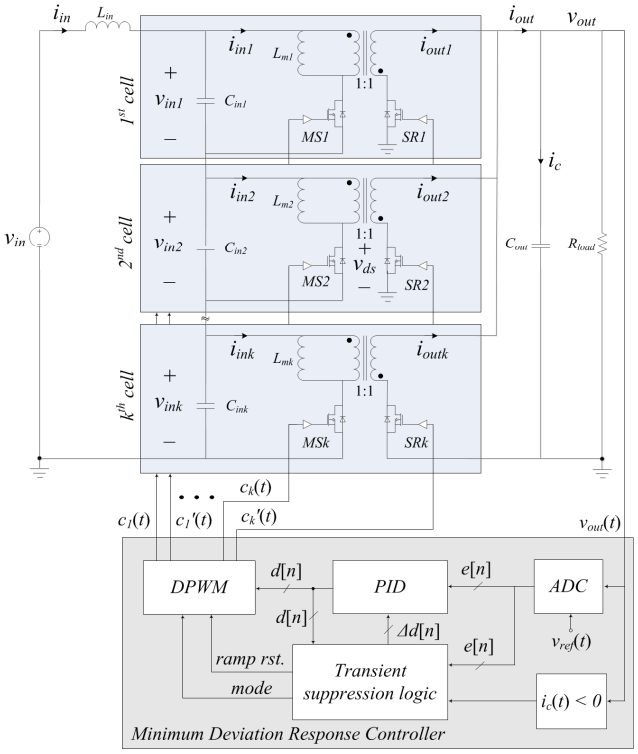

Figure 1. Low voltage stacked flyback converter and complementary minimum deviation controller.

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has smaller output filter volume and achieves better processing efficiency without suffering from the drawbacks existing in SC and MLB solutions. This modular converter structure also provides better transient response and inherent passive current sharing eliminating the need for phase currents measurements and balancing circuits.

II. PRINCIPLE OF OPERATION

In the converter of Fig.1 the input filter capacitor, inevitably existing in the targeted applications, is replaced with a capacitive divider and the inputs of flyback cells are connected to each of the divider taps, such that the voltage between the cells is shared. The outputs of the flyback cells are connected in parallel allowing output current sharing. A two-mode digital controller governs the operation of all modules. During steady state, the system operates as an interleaved voltage mode controlled system where a single multi-phase digital pulse width modulator (DPWM) [6] produces control signals $c_1(t)$ to $c_k(t)$ for the cells. The duty ratios of the signals are identical and determined based on the DPWM input control d[n], which is calculated by the PID once per switching cycle, using the digital output error voltage value, e[n]. During transients the controller enters transient suppression mode to quickly recover from the disturbance.

A. Volume Reduction

The volume reduction advantages of the stacked converter over the multi-phase buck converter can be determined through analysis of the effect of the number of modules on each individual converter. For the multi-phase buck, addition of each module results in lower current stress of the components. On the other hand, for the stacked flyback an increase in the number of modules has a three-fold effect. It reduces both the voltage and current stress of components and, in addition, minimizes the inductor voltage swing, allowing for the use of smaller inductance values [3, 4]. In fact, for a sufficiently large number of modules the flyback converter based topology will be smaller and more efficient than the conventional buck.

Quantitatively, the effect of the inductor voltage swing reduction on the converter volume can be described by analyzing the expression for the flyback magnetizing inductance value [7]:

$$L_m = \frac{1}{1+\frac{k\cdot V_{out}}{V_g}}\cdot\frac{V_{out}}{2\Delta i_{Lm}}\cdot\frac{1}{f_{sw}}, \qquad (1)$$

where V_{out} is the output voltage, f_{sw} is the switching frequency, k is the number of flyback cells, and Δi_{Lm} is the ripple amplitude. It can be seen that as the number of modules increase the inductor value reduces. This reduction in the inductance value, in turn, also allows for the minimization of the output capacitor, whose size in the targeted application depends on the transient performance. This is because, as shown in the following section, the ratio of the maximum voltage deviations of the buck and the stacked flyback under optimal, i.e. fastest possible, control is directly proportional to the ratio of their inductance.

The total reduction in the overall converter volume can be described with the following expressions for total minimum volume of reactive energy storage components and the diagram of Fig.2 showing the volume ratios of an interleaved buck and the stacked flyback modules:

$$V_{fb} \approx \left(\frac{1}{2}\cdot L_m\cdot\left(\frac{i_{load}}{kD'}\right)^2\cdot\rho_L+\frac{1}{2}\cdot C_{out}\cdot v_{out}^2\cdot\rho_C\right), \qquad (2)$$

$$V_{buck} \approx \left(\frac{1}{2}\cdot L\cdot\left(\frac{i_{load}}{k}\right)^2\cdot\rho_L+\frac{1}{2}\cdot C_{out}\cdot v_{out}^2\cdot\rho_C\right), \qquad (3)$$

$$\frac{V_{fb}}{V_{buck}} = \frac{(1+k\cdot\frac{v_{out}}{v_g})^3}{1-\frac{v_{out}}{v_g}}\cdot\frac{1}{k}\approx\frac{1}{k}\quad\left(\frac{v_g}{v_{out}}>>k\right) \qquad (4)$$

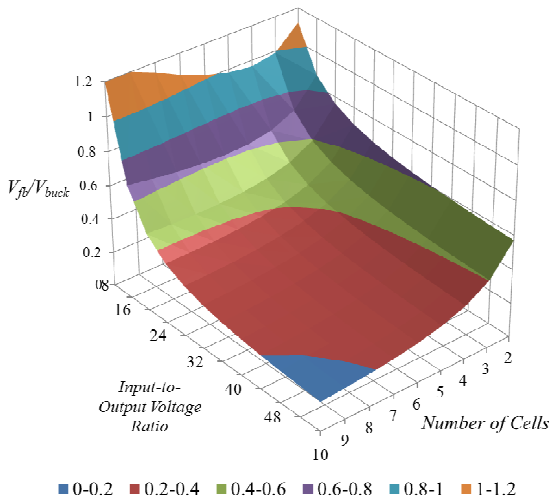

Figure 2. Volume as a function of input-to-output voltage conversion ratio and number of phases.

where, V_{fb} is the volume of a flyback module, V_{buck} is volume of the buck module, while, ρ_L and ρ_C are the inductor and capacitor energy density values, respectively. The results in Fig.2 obtained for typical reactive component energy density values [8], show that for step down ratios larger than eight, the two-module flyback structure already results in a smaller volume than that of the conventional buck.

B. *Inherent Current Sharing and Tap Voltage Sharing*

In conventional multi-phase dc-dc converters current sharing is often required to provide equal current or thermal stress across all phases [9]. The practical implementation of the current sharing systems often requires costly dedicated circuits for sensing or estimation of phase currents and an additional control loop for regulating the process. The stacked flyback provides inherent current sharing eliminating the need for a dedicated circuit.

To explain this feature of the converter, its dc averaged model of Fig.3 can be observed. In this model switching and conduction losses of individual phases are modeled with their secondary side equivalent resistances Req. Analysis of this equivalent circuit reveals two important inherent characteristics of the stacked-flyback: equal current and tight input voltage sharing.

By looking at the model it can be seen that, all the current sources on the primary side are connected in series and, therefore, they must have the same input current independent on the phase variations. Consequently, for the identical duty ratios, the secondary side phase currents, labeled as I_{out1} to I_{outk} are the same. By solving the circuit of Fig.3 for the tap voltages, i.e. voltages across dependent current sources [7], it can be found that V_{inm}, i.e. the voltage across the m^{th} the tap is:

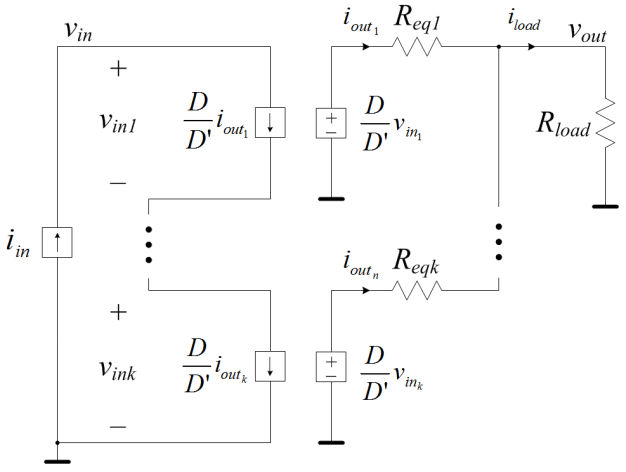

Figure 3. Equivalent dc circuit model of the stacked flyback converter with *k* flyback cells.

$$V_{inm} = \frac{V_g}{k}\left(\frac{1+\dfrac{R_{eqm}}{k \cdot R_{load}}}{1+\dfrac{R_{eq_{av}}}{k \cdot R_{load}}}\right), \tag{5}$$

where R_{eq_av} is the average lumped-sum equivalent resistance, and R_{load} is the output load resistance. This expression shows that, for a properly designed converter, where $R_{load} >> R_{eq}$ equal voltage sharing among the capacitor taps is practically achieved

III. NEAR OPTIMUM DEVIATION CONTROLLER

One of the main drawbacks of conventionally controlled flyback converters is relatively slow transient response, mostly caused by the conventional compensator design and the presence of the right half plane zero. To eliminate this problem and allow the stackable flyback to be used in the targeted applications, where the transient response of the controller is of a key importance, a near-minimum deviation controller is developed. This controller utilizes a modification of the minimum deviation control method, presented in [10, 11] where, for a given converter topology, the controller suppresses load transients with minimum possible output voltage deviation using very simple hardware and requiring no knowledge of converter parameters. In this two-step method, as soon as a disturbance is detected, the controller enters the transient suppression mode. During this mode the new steady state values of the inductor current and its ripple are reconstructed over one switching cycle. As a result the effect of the transient on the output voltage is reversed and the deviation limited to its minimum possible value. After the current reconstruction is completed the control task is passed to a conventional PID regulator recovering voltage to its reference value. In this case, to simplify the controller implementation and allow only secondary side control, the optimum deviation method is modified and the current reconstruction is performed over several cycles, by monitoring polarity of the output capacitor current. Still, as it will be shown later, the transient performance of this system are better than that of the optimum-deviation controlled buck.

A. *Light-to-Heavy Transient*

During light-to-heavy transients the recovery is performed through a simple repetitive charge and check based procedure. This procedure can be explained with the help of diagrams shown in Figs. 4 and 5. For simplicity, the diagrams are shown

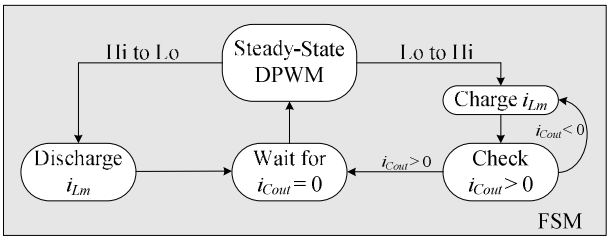

Figure 4. Finite state machine for light-to-heavy and heavy-to-light transients.

for a 2-module case. As soon as the transient is detected, at $t = t_0$, the main switches of the flyback cells are turned on over $t_{on}=DT_{sw}$ period (labelled *c* in Fig. 5) and the inductor current is ramped up. At the end of the charging period, the MS transistors are turned off (SRs turned on) and the coupled inductors are discharged into the output node (labelled *d* in Fig. 5). During the discharging phase the polarity of the capacitor current is monitored by the controller. If a negative current is detected within a time period equal to t_{min}, the inductor charging mode (*c*) is reactivated. The charging and discharging procedure is repeated until a positive capacitive current value is detected. This only occurs when the inductor current is larger than that of the load, i.e. sufficiently high to reverse capacitor discharge and start the voltage recovery process. At that point the PID compensator is reactivated and the voltage is recovered to its reference value in a monotonic fashion.

B. Heavy-to-Light Transient

During heavy-to-light transients the transient suppression logic operates as a non-modified minimum deviation controller [10]. After a transient is detected, at $t=t_1$, the SRs are turned on and the coupled inductors discharged into the output capacitor until the zero capacitor current crossing is detected. At that point initial values of the duty ratios are reset, as described in [9], and the PID is reactivated.

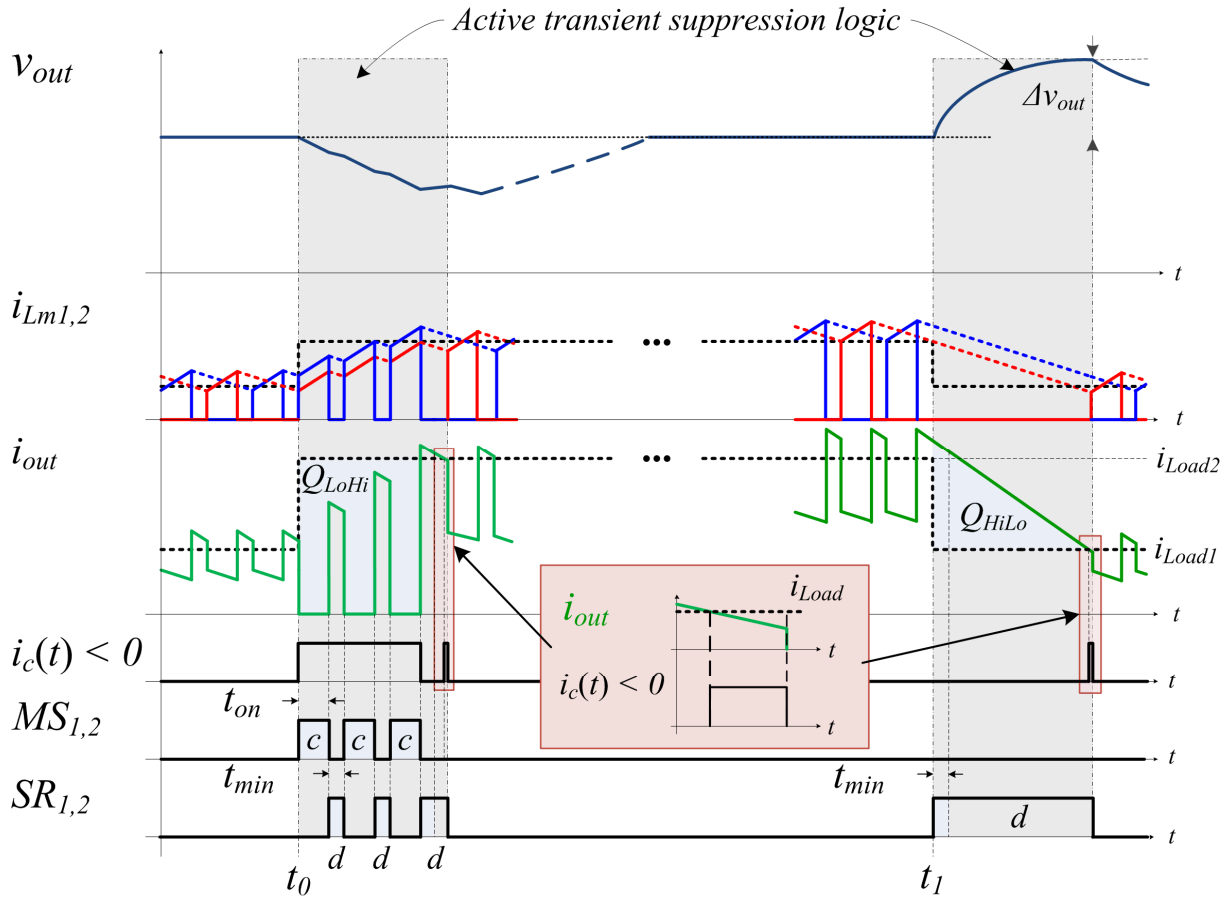

Figure 5. Main current and voltage waveforms during light-to-heavy and heavy-to-light transients.

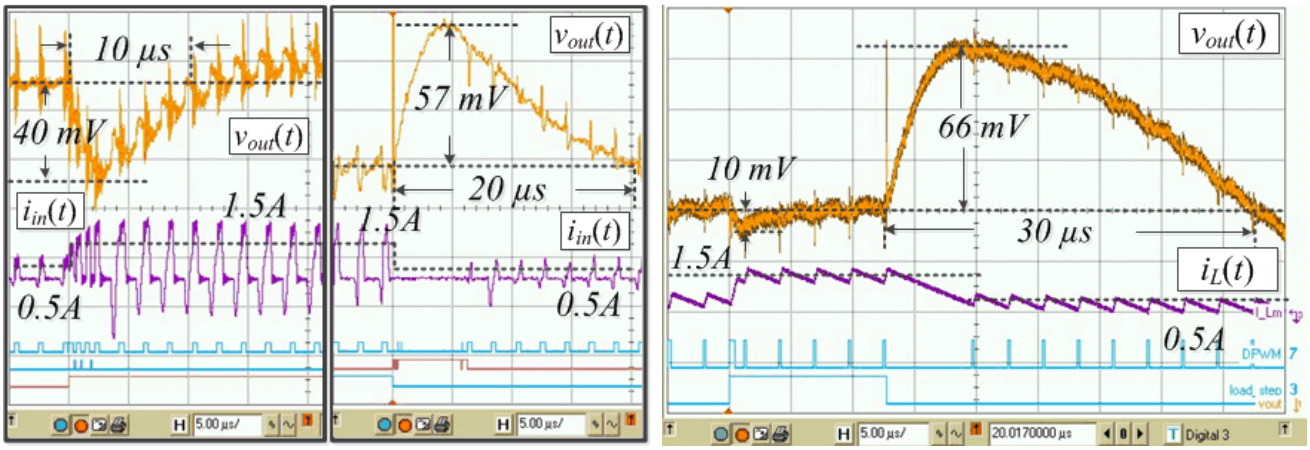

Figure 6. Response to a 0.5-A→1.5-A→0.5-A load step of the stacked flyback cell (left) and buck converter phase (right). Ch.1: Output voltage $v_{out}(t)$, 20mV/div; Ch. 2: Inductor current $i_L(t)$, 2A/div; The time scale is 5µs/div for both waveforms.

IV. Experimental Results

To verify the converter and controller an experimental prototype of a stackable flyback is created based on Figs. 1, 4 and 5. The performances of this converter are compared to that of a conventional buck. The prototype is designed to operate with 2 or 3 cells. Each cell was designed for 2A maximum output load current, 6V input voltage, 1-1.5V output voltage and 500 kHz switching frequency. The power stages are formed of discrete components, while the controller is based on a field-programmable gate array system (FPGA) and discrete components. The zero current detection circuit has self-tuning capability and utilizes simple design shown in [12]. The power stages also include active snubber circuits [13]. The flyback inductors with 1:1 turns ratio have magnetizing inductances of 3.3 µH [14]. The output capacitor value of 40 µF is selected, ensuring less than 100 mV voltage deviation during the worst case load transient. Using the principles outlined in subsection II.A, the buck converter reactive components are selected such that the volume of the reactive components, related to the Li^2 and Cv^2 products, and inductor current ripple are the same for both converters. The inductor size for such an optimization is 4.7 µH, assuming k = 2, the output capacitor 40 µF and the switching frequency 390 kHz.

In Fig. 6, the responses to a 0.5-A→1.5-A→0.5-A load step (per cell) for a 12-V-to-1-V two-cell stacked flyback experimental prototype and two-phase buck converter are compared. From Fig. 6 it can be seen that a 14% smaller voltage deviation and 33% shorter settling can be achieved with the stacked flyback, while utilizing a similar volume inductors. The improved output voltage deviation enables a similar reduction of the output capacitor size.

Figure 7 plots the power processing efficiency (left) of the

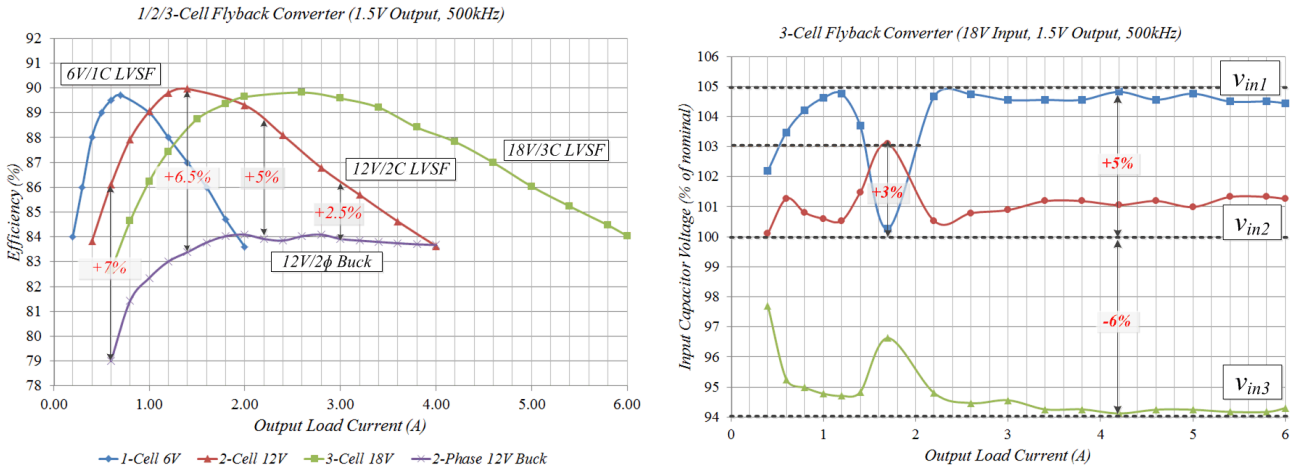

Figure 7. Power processing efficiency (left) the 1/2/3 Cell stacked flyback and 2-phase buck converter prototypes and input capacitor voltages (right) of the stacked flyback converter with respect to the output load current.

stacked flyback and buck converter experimental prototypes and the input capacitor voltage sharing (right) of the stacked flyback converter. Compared to the 2-phase buck converter, the 2-cell stacked flyback delivers up to 6.5% better power processing efficiency, i.e. 40% lower power losses. These results can allow for a further increase in switching frequency and thus an additional reduction of the inductor volume for the stacked flyback. Furthermore, tight passive input voltage sharing is maintained across the entire range of output load levels, within 6% of the nominal values. Also, near-linear efficiency scaling is observed with respect to the number of cells.

V. CONCLUSIONS

The paper introduced a modular solution for high step down conversion ratio applications that combines a stacked flyback converter and novel near optimal deviation controller. For high step down ratios and relatively small number of modules this topology requires smaller volume of reactive components than an equivalent multi-phase buck and results in better power processing efficiency. This is due to three-fold effect of modularization that at the same time causes current sharing, voltage stress reduction, and inductor value minimization. The near optimum deviation controller eliminates slow dynamic response problem characteristic for conventional flyback solutions and provides smaller voltage deviation than that of an optimally controlled buck.

REFERENCES

[1] Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines, Intel Corporation, Santa Clara, CA, Sept 2009.

[2] V. W. Ng, M. D. Seeman, and S. R. Sanders, "Minimum PCB footprint point-of-load DC–DC converter realized with switched-capacitor architecture," *in Proc. IEEE Energy Convers. Congr. Expo*., pp. 1575–1581, Feb. 2009.

[3] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched capacitor energy transfer," *in Proc. IEEE Power Electron. Spec. Conf*., pp. 4008–4015, Jun. 2008.

[4] T.A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *Industrial Electronics, IEEE Transactions on* , vol.49, no.5, pp. 955- 964, Oct 2002.

[5] M. Shoyama, T. Naka, and T. Ninomiya, "Resonant switched capacitor converter with high efficiency," *in Proc. IEEE Power Electron. Spec. Conf*., pp. 3780–3786, Jun. 2004.

[6] A.V. Peterchev, Jinwen Xiao, and S.R. Sanders, "Architecture and IC Implementation of a Digital VRM Controller", *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pt. 2, pp. 356-364, Jan, 2003.

[7] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics. New York, NY:Springer Sience+Business Media Inc., 2001.

[8] M.D. Seeman, V.W. Ng, Le Hanh-Phuc, M. John, E. Alon, and S.R. Sanders, "A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies," *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on* , vol., no., pp.1-7, 28-30 June 2010.

[9] Z. Lukić, "Design and Practical Implementation of Advanced Reconfigurable Digital Controllers for Low-Power Multi-Phase DC-DC Converters." PhD thesis, University of Toronto, Canada, 2011.

[10] A. Radić, Z. Lukić, A. Prodić, and R. de Nie, "Minimum Deviation Digital Controller IC for DC-DC Switch-Mode Power Supplies," *Power Electronics, IEEE Transactions on* , vol.28, no.9, pp.4281-4298, Sept 2013.

[11] M.M. Peretz, "Hybrid Control Method for Optimal Transient Response and Output Filter Minimization for Buck-Boost type Converters" , *PCIM-2013 Nuremberg*, pp. 1428-1435, May 2013.

[12] A. Radić, D. Baik, A. Straka, A. Prodić, and R. de Nie, "Noninvasive self-tuning output capacitor time constant estimator for low power digitally controlled dc-dc converters," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Fifth Annual IEEE*, pp. 559-562, 17-21 Mar. 2013.

[13] R. Watson, F.C. Lee, and G.-C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *Power Electronics, IEEE Transactions on* , vol.11, no.1, pp.162-169, Jan 1996

[14] LPD5030-332MEB 3.3 µH Coupled Inductor Datasheet, Coilcraft Inc., Cary, IL, 06/2013.