Design of a Digital PID Regulator Based on Look-Up Tables for Control of High-Frequency DC-DC Converters

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Abstract – **This paper describes design of a digital PID regulator based on look-up tables for high frequency dc-dc switching converters. The use of the look-up tables instead of multipliers enables a small, low-power implementation and operation at high switching frequencies. Design guidelines are given for the resolution and size of entries in the look-up tables. A design example and experimental results are presented for a digital controller IC used to control a 1 MHz, 2.7 V, 3 W buck converter.**

I. INTRODUCTION

Digital controllers can offer a number of advantages over analog controllers, including flexibility, lower sensitivity, and programmability without external components [1-6].

Figure 1 shows a digitally controlled switching converter. It consists of an analog-to-digital converter, a processing unit (regulator) that implements a control law, and a digital pulse width modulator (DPWM). In order to achieve dynamic characteristics comparable with analog PWM controllers, fast implementation of a discrete-time control law is required. For cost-driven low-power, high-frequency applications, simplicity, small size and low power consumption are important. In order to implement a digital controller for these applications, hardware optimization is needed. The hardware requirements that DPWM and analog-to-digital converter have to satisfy are defined in [7, 8]. In this paper, we focus on minimum hardware requirements for the computational unit that implements a discrete-time PID control law.

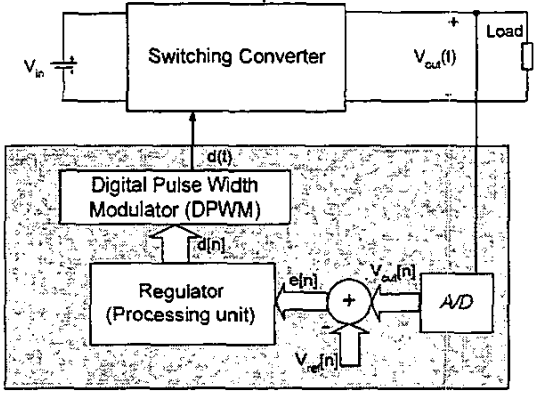

Figure 1. Block diagram of a digitally controlled dc-dc switching converter.

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In Section II, the regulator structure is given and problems of conventional implementation based on multipliers are addressed. Design guidelines for selection of the resolution of the computational unit are given in Section III. Section IV shows experimental results obtained with an on-chip implemented, look-up table based regulator for a buck converter operating at 1 MHz switching frequency.

II. REGULATOR STRUCTURE

In the controller of Figure 1, the sampled output voltage is compared to a reference and their difference forms an error signal. A regulator that implements a control law processes the error signal. The control law can be represented in the following form:

$$d[n] = \alpha_1 d[n-1] + \alpha_2 d[n-2] + .. + \beta_0 e[n] + \\ + \beta_1 e[n-1] + \beta_2 e[n-2] + ... \qquad (1)$$

where $d[n]$ and $e[n]$ are the current values of the duty ratio and the error signal, while $d[n-i]$ and $e[n-i]$ are the values of the duty ratio and the error signal i cycles before the current cycle. The coefficients α_i and β_i determine the regulator characteristics.

It can be seen that implementation of the discrete-time control law (1) requires several multiplications and additions. Digital multipliers are relatively large or slow components.

For a properly operating feedback system, the difference between the measured output voltage and the reference is relatively small. This opens the possibility of implementing the regulator using relatively small look-up tables instead of multipliers [3].

A block diagram of the look-up table based structure is shown in Figure 2. The regulator performs the following discrete-time PID control law [9]:

$$d[n] = d[n-1] + a \cdot e[n] + b \cdot e[n-1] + c \cdot e[n-2] \qquad (2)$$

Outputs of the look-up tables are pre-stored values of their inputs multiplied by the controller coefficients. The current and previous values of the error signal are used as address generators for the tables. New value of the duty ratio is formed as a sum of its previous value and the values at the look up tables' outputs.
The PID control law given by Equation (2) results in zero steady-state error. Furthermore, there is no further processing of the previous value of the duty ratio. This is important because the duty ratio has large variations and the result of multiplication by a controller coefficient cannot be stored in a small look-up table.

III. CONTROLLER DESIGN

The size of the look-up tables and the number of bits needed for representation of the previous value of the duty ratio are discussed in this section in relation to the desired dynamic and static characteristics, resolution of the DPWM, analog-to-digital converter, and the converter configuration.

Principles of controller design are illustrated using the buck converter example of Figure 3. An objective is to find the minimal structure that can satisfy desired dynamic and static voltage regulation characteristics. Necessary conditions for the resolution of the A/D converter and the DPWM to avoid undesired limit-cycle oscillations are analysed in [7]. The minimum DPWM resolution for the buck converter is

$$n_{pwm} \geq \text{int}\left[\log_2\left(\frac{V_{ref}}{V_Q \cdot D}\right)\right] \qquad (3)$$

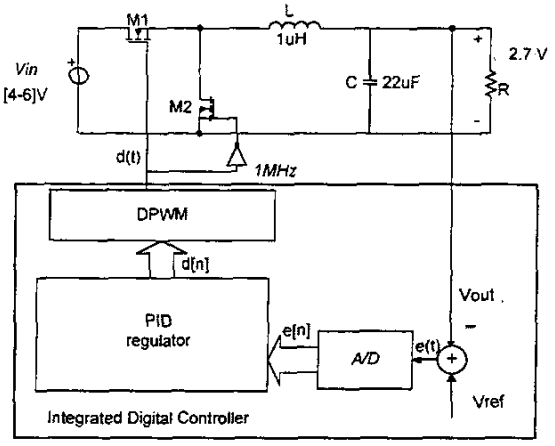

Figure 3. Experimental system: buck converter controlled by a digital controller integrated circuit with PID regulator based on look-up tables.

where: n_{pwm} is the number of bits of DPWM, V_Q is the A/D quantization level, V_{ref} is the reference voltage, and D is the minimum steady-state value of the duty ratio, which corresponds to the maximum input voltage. The value given by Equation (3) is also the minimum number of bits required at the regulator output. For example, starting from the requirement for 1.5% voltage regulation at the nominal output voltage of 2.7 V, an analog-to-digital converter with the quantization level V_Q of 40mV and an 8-bit DPWM are needed.

A. PID Regulator design

The block diagram of Figure 4 shows the system model.

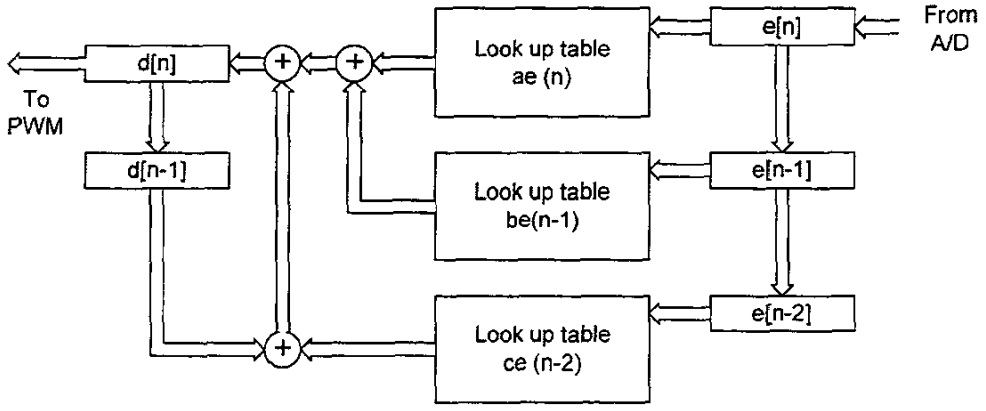

Figure 2. PID regulator based on look-up tables.

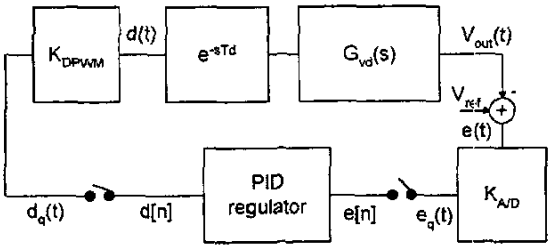

Figure 4. Block diagram of the sampled-data system consisting of a PWM switching converter and a discrete-time digital controller.

The system is divided into two parts: continuous-time and discrete-time. The continuous-time transfer function $G_c(s)$ from d_q to e_q can be found as:

$$G_c(s) = K_{A/D} K_{DPWM} G_{vd}(s) \exp(-sT_D) \tag{4}$$

where: $K_{A/D}$ is the gain of the A/D converter, K_{DPWM} is the gain of the DPWM, $G_{vd}(s)$ is the control-to-output transfer function of the averaged model of the converter [10], and T_D is a processing delay. For the considered experimental example, these values are $K_{A/D} = 1/V_q = 25$, $K_{DPWM} = 1/255$ and the delay is $T_D = 1/f_s$, where f_s = 1MHz is the switching frequency. The buck converter operates in continuous conduction mode. The transfer fuction $G_{vd}(s)$ has a pair of poles with the center frequency equal to 35 kHz.

The discrete-time part of the system is the digital PID regulator. The controller parameters are found using a digital redesign based on the pole-zero matching transformation method [9].

The number of words in look-up tables is defined by a maximum allowed output voltage variation. In the experimental case, for the maximum allowed voltage variation of 5% around the nominal output voltage, the A/D converter must operate only over a small range (+/- 160mV). Given V_q = 40mV, we need only nine quantization levels, and therefore only nine words in each of the look-up tables.

The control law determines the number of bits needed for the representation of the look-up table words. The control law defined by Equation (2) forms a PID regulator with a pole at 0 Hz and two zeroes. A larger number of bits is needed to represent zeros at lower frequencies. This is because a low-frequency zero in continuous-time domain is transferred close to the unit circle in the z-plane.

In order to reduce the size of the look up tables, the controller zeroes f_z are placed at higher frequencies, close to the center frequency of the converter control-to-output transfer function. This selection also results in a lower sensitivity to round off effects in comparison with a configuration that would have zeroes at lower frequencies.

The desired loop gain characteristics are shown in Figure 5. Bandwidth of the closed loop system is limited by additional phase shift caused by the processing delay.

In order to keep the phase margin higher than 45 degrees, the cross-over frequency is limited to the range between 50 kHz and 100 kHz.

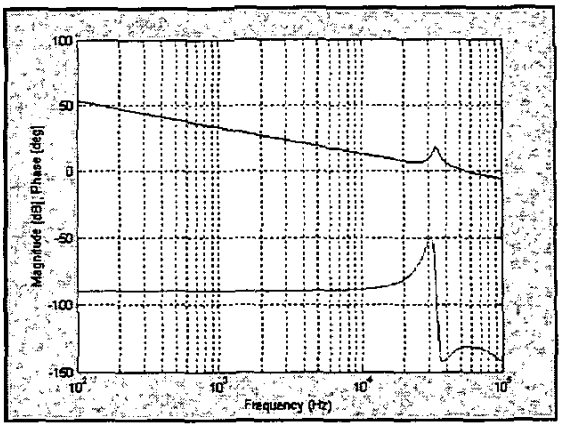

Figure 5. Desired loop gain characteristics.

The PID regulator is designed starting from a continuous-time equivalent:

$$C(s) = K_{IA} \frac{1 + \frac{s}{Q\omega_z} + \frac{s^2}{\omega_z^2}}{s} \tag{5}$$

which leads to the following discrete-time control law obtained using the pole-zero matching transformation method:

$$d[n] = d[n-1] + K_I (e[n] - 2r\cos(2\pi \frac{f_z}{f_s}) e[n-1] + r^2 e[n-2]) \tag{6}$$

In Equation (6): K_I is the gain of the digital regulator, f_z is the center frequency of the pair of zeros, and f_s is the sampling frequency, which in this case is the same as the switching frequency of the converter. The relation between the factors r and Q is given by

$$r = \exp\left(-\frac{\pi f_z}{Q f_s}\right) \tag{7}$$

which can also be derived using the same transformation method. The factor r is found for the maximum value of the Q factor of the pair of poles in the control-to-output transfer function of the converter, which corresponds to the light load condition.

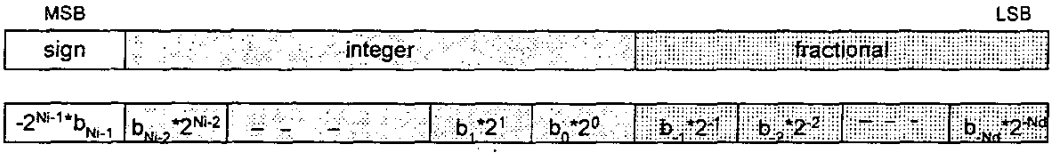

Figure 6. Digital numbers representation used in the regulator design.

To find the minimum number of bits for the implementation of this PID regulator, let us use the representation for digital numbers shown in Figure 6.

A number x is formed as:

$$x = -(2^{Ni-1} \cdot b_{Ni-1}) + \sum_{i=-N_d}^{N_i-2} b_i 2^i \qquad (8)$$

where the coefficients b_i can have value 0 or 1. To enable effect on the output variable even when the values of the resolution must be high enough to store that minimum increment/decrement. Therefore, the minimum number of bits needed for the representation of the fractional parts of $d[n-1]$ and the entries in the look-up tables is:

$$N_d = \text{int}\left[\log_2\left(\frac{1}{K_I(1-2r\cos(2\pi f_z / f_s)+r^2)}\right)\right] \qquad (9)$$

where: int[] – denotes the upper rounded integer value.

The control law and the maximum value of the error signal define the number of bits needed to represent the integer part of the numbers stored in the three look-up tables:

$$\begin{aligned} N_{IC1} &= \text{int}\left[\log_2(1+2K_I \cdot |e[n]_{max}|\right] \\ N_{IC2} &= \text{int}\left[\log_2(1+4K_I r \cdot \cos(2\pi f_z / f_s) \cdot |e[n]_{max}|)\right] \\ N_{IC3} &= \text{int}\left[\log_2(1+2K_I r^2 \cdot |e[n]_{max}|\right] \end{aligned} \qquad (10)$$

Given the error range ($-e[n]_{max}$ to $e[n]_{max}$), the selected number of bits for the representation of the integer part of numbers provides for the sign and the integer value.

Equations (9) and (10) show that we can use smaller-size words for systems with a stronger gain and with a higher ratio of the corner frequency and the switching frequency. The maximum gain is limited by the phase-margin constraints and by the other requirements to avoid limit-cycle oscillations [8]. In the design example, the selected gain is $K_I = 12.5$, and the discrete-time control law is given by:

$$d[n] = d[n-1] + 12.5(e[n] - 1.88e[n-1] + 0.92e[n-2]) \qquad (11)$$

For the selected gain, the crossover frequency of 50 kHz is obtained for the light load condition.

From Equation (9), it follows that in this case one bit is needed to represent the fractional part of the numbers. Based on Equations (3) and (10), eight bits are needed to represent $d[n]$, $ae[n]$ and $ce[n-2]$, while nine bits are needed to represent $be[n-1]$ and $d[n-1]$. Table I gives the total size of the regulator blocks for the experimental structure.

Table I – Resources needed for look-up table based regulator implementation

	Number of words	Word length
Table ae[n]	9	8-bit
Table be[n-1]	9	9-bit
Table ce[n-2]	9	8-bit
d[n-1]	1	10-bit

A total of 225 bits of storage is needed for the look-up tables in this example. In the experimental system, additions are performed using one adder and an accumulator [11]. The system clock frequency is 8 MHz.

IV. EXPERIMENTAL RESULTS

A. Load transient

Load transient experimental results for the output current change from 0.3 A to 1 A are shown in Figures 7.a. and 7.b.

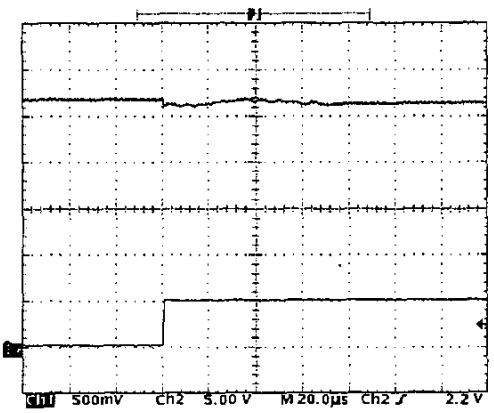

Figure 7.a. Load transient response, Ch-2 load change from 0.3 – 1 A; Ch1-Output voltage top (500mV/div).

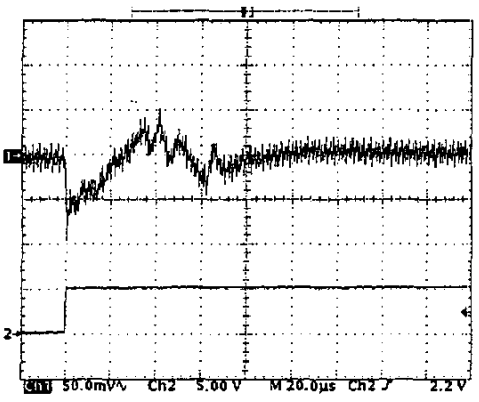

Figure 7.b. Zoomed ac component of the output voltage Ch-1 (50mV/div); Ch2-Load current

From Figures 7.a. and 7.b. it can be observed that the output voltage variations during transients are smaller than 5% and that the output voltage settles inside the +/-40 mV range in less than 50µs.

B. Soft start

The presented controller configuration has an additional advantage that it provides a built-in soft start. During start-up transient, the error signal is limited to its maximum value and the duty ratio slowly increases from zero toward the steady-state value. Figure 8 shows the output voltage during a start-up transient when the converter is supplied from an input voltage of 6 V.

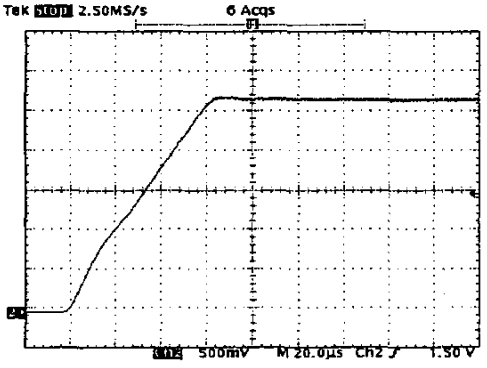

Figure 8. Output voltage during start-up transient.

V. CONCLUSIONS

In this paper we describe design and implementation of a digital PID regulator in a controller based on look-up tables, which results in fast and simple hardware realization. Guidelines for selection of the size of the hardware structure are given and demonstrated on an example of a digitally controlled buck converter operating at 1 MHz switching frequency.

VI. REFERENCES

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