Self-Tuning Digital Comb Filter for PFC Applications

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Abstract – Design and implementation of a self-tuning digital comb filter for power factor correction (PFC) rectifier applications are described. The comb filter enables fast response to load transients in universal input rectifiers and consequently more optimal design of the PFC power stage and a downstream dc/dc converter. The design is based on a modification of a conventional comb filter and implementation of frequency selector logic. The filter is used to eliminate the second and higher harmonic components from the voltage loop, while the frequency selector logic provides automatic adjustments of the filter characteristics and correct operation for different input line frequencies. Experimental results obtained on a 200 W universal-input boost PFC prototype are demonstrated.

I. INTRODUCTION

In conventional design of the outer voltage loop for PFC applications the bandwidth of the loop is limited to a frequency significantly lower than the input voltage line frequency [1,2]. This limitation is imposed by the output capacitor ripple at the twice the line frequency, which cannot be removed without causing significant input current distortion. A low-bandwidth voltage loop eliminates the ripple from the feedback but causes poor dynamic response. Large overshoots and dips during load transients require over-design of the PFC power stage and downstream dc/dc converters.

Several approaches to improving dynamic response of the voltage loop in PFC rectifiers have been proposed [3-10]. A method based on elimination of the second harmonic from the voltage loop with an analog notch filter in the feedback loop was proposed in [5,6], but the implementation with standard analog components is not considered practical. Implementation of a digital notch filter has been presented in [9]. This implementation is limited to a single input line frequency and the case when the input voltage waveform is not distorted. To address these limitations, the method presented in [10] is based on elimination of second and higher harmonics from the voltage loop using a self-tuning digital comb filter (STCF). This paper is focused on details of the self-tuning comb filter design and implementation. It is shown how this implementation provides fast dynamic response for different input voltage frequencies even in the case when the input voltage is distorted.

This paper is organized as follows: the influence of the filter on the voltage loop is analyzed in Section II. The modified comb filter is described in Section III. Section IV gives design guidelines for implementation of the modified comb filter, together with experimental results illustrating improved dynamic responses. The method for the input line frequency detection and adjustment of the filter characteristics is presented in Section V.

II. FILTER IN THE VOLTAGE LOOP

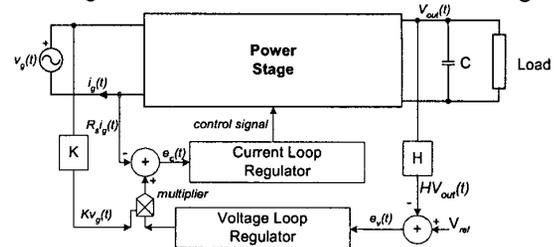Block diagram of a PFC rectifier circuit is shown in Fig.1.

Figure1: Block diagram of a PFC rectifier.

Control is typically performed with two feedback loops: a current loop, and a voltage loop. The fast current loop forces the input current $i_g(t)$ to follows the shape of the input voltage $v_g(t)$, according to

$$i_g(t) = \frac{v_g(t)}{R_e} \qquad (1)$$

The value of the emulated resistance R_e is controlled by the slow voltage loop. The voltage loop controls the power flow and regulates the output voltage $V_{out}(t)$ around a reference value.

In the ideal rectifier model, the input port is represented with a "loss-less" resistor R_e, while the output port is represented by a controlled power source [2]. The instantaneous power of this source is

$$\left\langle p_{ac}(t) \right\rangle_{T_s} = \frac{v_g(t)^2}{R_e} \qquad (2)$$

where, in general, the periodic input line voltage can be expressed as a sum of the fundamental and higher harmonics:

$$v_g(t) = V_1 \sin(\omega_L t) + \sum_{n=2}^{\infty} V_n \sin(n\omega_L t + \varphi_n) \qquad (3)$$

In the ideal case, the higher harmonics do not exist. In practice, the input voltage waveform can have significant amount of higher, usually odd harmonics.

From (2) and (3), it follows that the instantaneous power transferred from the input to the output of the rectifier can be written as sum of a dc power component P_0 and components at the multiples of twice the line frequency

$$\langle p_{ac}(t) \rangle = P_0 + \sum_{n=1}^{\infty} P_n \cos\left(2n\omega_L t + \varphi_n\right) \qquad (4)$$

Consequently, the output voltage besides the dc component contains components at twice the line frequency and possibly components at multiples of that frequency. In a conventional design, the voltage loop is closed at a frequency (typically 10 to 20 Hz) significantly lower than the second line harmonic.

In order to improve dynamics of the voltage loop, a digital comb filter that eliminates the second harmonic and its multiples from the voltage feedback has been proposed in [10].

III. MODIFIED COMB FILTER

The purpose of the comb filter is to eliminate the second harmonic and its multiples from the voltage feedback loop, while having minimum impact on the magnitude and phase responses at other frequencies.

A suitable filter transfer function, obtained by modifying a conventional comb filter [11] is given by [10]:

$$H_{mc}(z) = \frac{1 - z^{-(M+1)}}{1 - z^{-1}} \cdot \frac{1 - (rz)^{-1}}{1 - (rz)^{-(M+1)}} \qquad (5)$$

To examine the frequency response of this filter, we can write the complex variable z in polar form,

$$z = |z| e^{j\omega}, \omega = 2\pi \frac{f}{f_s} \qquad (6)$$

and observe the magnitude and the phase characteristic of (5) for the case when $|z| = 1$, while the input signal frequency f changes between 0 and f_s. The resulting frequency response can be written as:

$$H_{mc}(j\omega) = \frac{\left(e^{j\omega} - z_1\right)\left(e^{j\omega} - z_2\right)..\left(e^{j\omega} - z_k\right)}{\left(e^{j\omega} - p_1\right)\left(e^{j\omega} - p_2\right)..\left(e^{j\omega} - p_k\right)} \qquad (7)$$

Fig.2.a and 2.b show a Z-plane graphical representation of this equation for two different input signal frequencies.

In Fig.2.a we can see that the zeroes of the filter are placed at the unit circle:

$$z_k = e^{j2\pi \frac{k}{f_s(M+1)}}, k = 1,2,..,M \qquad (8)$$

while the poles are placed at:

$$p_k = r \cdot e^{j2\pi \frac{k}{f_s(M+1)}}, k = 1,2,...,M \qquad (9)$$

where, $r \in [0 \div 1)$.

The discrete transfer function now can be described as the ratio of products of vectors

$$H_{mc}(z) = \frac{R_{Z1} \cdot R_{Z2}...R_{zk}}{R_{P1} \cdot R_{P2}...R_{Pk}} \qquad (10)$$

where R_{Zi} and R_{Pi} are the vectors of differences between z_i, p_i and $e^{j\omega}$ respectively.

For the case when the factor r is close to one, and frequency of the input signal is far from one of the pole-zero frequencies (Fig.2.a), the vectors R_{zi} and R_{pi} have approximately the same magnitude and phase. Consequently, the amplitude and phase of the input signal remain almost unchanged.
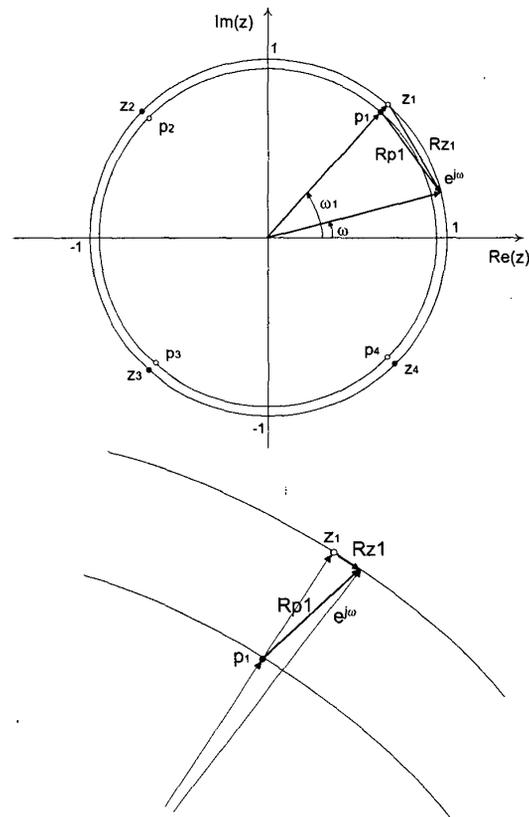

Figure 2: Z-plane, pole - zero pattern of the modified comb filter. a)(top) position of the vectors for the case when the input signal frequency ω is far from a pole/zero frequency b) (bottom) a magnified section of the unit circle around the pole/zero p_1/z_1 for the case when $\omega \approx \omega_1$.

Fig.2.b shows the case when the input signal frequency is in the vicinity of a pole/zero. The dominant factor in the frequency response becomes the ratio of the vectors R_{Zi} and R_{Pi}. Finally, when the frequency of the input signal is equal to one of the pole/zero frequencies the input signal is completely attenuated.

Fig.3 shows the magnitude and the phase response of the modified comb filter for two different values of the factor r. It can be seen that for higher values of the factor r the filter characteristic becomes closer to the ideal for the intended application.

IV. FILTER IMPLEMENTATION

Based on (5), the difference equation of the modified comb filter is

$$e_{vf}[n] = e_{vf}[n-1] + r^M e_{vf}[n-M] - r^M e_{vf}[n-M-1] + \\ + e_v x[n] - re_v[n-1] - e_v[n-M] + re_v[n-M-1] \quad (11)$$

where, $e_v[n]$, $e_v[n-i]$ are sampled values of the input signal, in this case the voltage error (Fig.1) at time instances nT_s and $(n-i)T_s$, respectively, and T_s is the sampling period. The discrete value of the filter output at the time instance nT_s is $e_{vf}[n]$. This is the filtered value of the voltage error signal.

A diagram of the structure that implements (11) is shown in Fig.4. The computation is initialized with the sampling of $e_v[n]$. The following operations are then performed: 1) $e_v[n]$ is stored into the input circular buffer at the first address location labelled as <address:n_{x0}>; 2) Each of the previously sampled values is moved to a new, one bit higher address; 3) The oldest sampled value is overwritten; 4) A new output value is calculated and stored into the
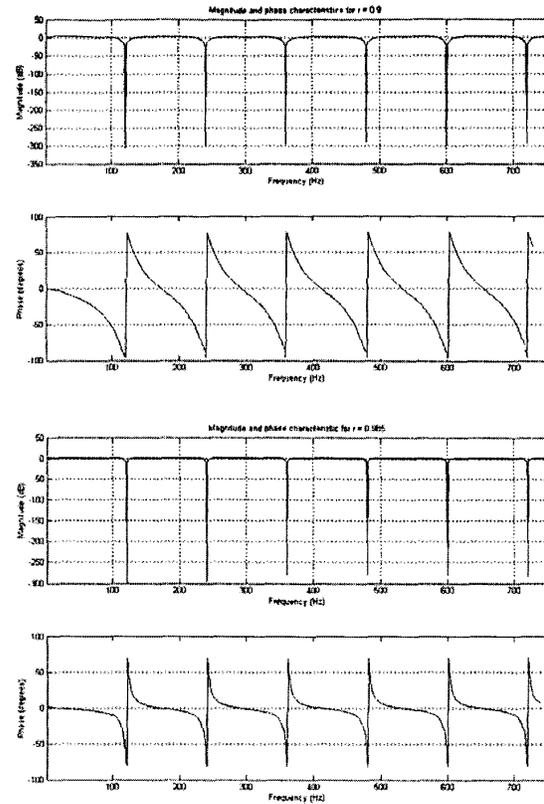

Figure 3: Magnitude and phase characteristics of the modified comb filter for (a) $r = 0.9$ (top), and for (b) $r = 0.985$ (bottom).

output circular buffer at the first address location labelled as <address:n0>; 5) The previous output values are moved to higher addresses.
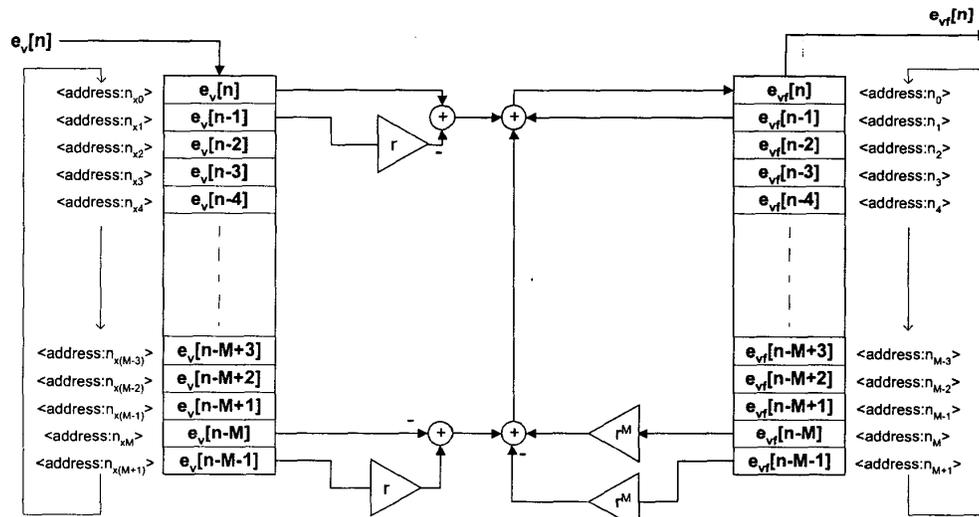

Figure 4: Implementation of the modified comb filter.

From Fig.4 it can be seen that the use of the circular buffers for software implementation of this comb filter presents a simple and flexible solution. In order to calculate the output value, only six stored values are used: the values stored one cycle before, and the two oldest values.

With the use of the circular buffers, the two oldest values of the input sampled signal $e_v[n-M]$ and $e_v[n-M-1]$ can be called using the addresses <address:n_{x0}-1> and <address:n_{x0}-2>. When a circular buffer is used, those addresses will be understood as the oldest addresses. Similarly, the two oldest output values can be addressed as <address:n_0-1> and <address:n_0-2>. Therefore, to implement the filter, a simple computation is performed as follows:

$$e_{vf}[n] = e_{vf}\langle address:n_1\rangle + r^M e_{vf}\langle addrss:n_0-2\rangle +$$
$$+ r^M e_{vf}\langle address:n_0-1\rangle + e_v[n] - re_v\langle address:n_{x1}\rangle - \quad (12)$$
$$- e_v\langle address:n_{x0}-2\rangle + re_v\langle address:n_{x0}-1\rangle$$

This equation does not depend on the filter order M. It has the same form for different lengths of the circular buffers and different sampling frequencies. This means that in order to change characteristics of the filter we can just change the sampling frequency and the sizes of the circular buffers. The number of words needed for each circular buffer depends on the filter order and equals M+2.

I. Hardware constraints

To implement the filter in an experimental system shown in Fig.5 we decided to use the sampling frequency 40 times higher than the second harmonic frequency of the ac line, and 8-bit, fixed-point arithmetic.

Selection of the sampling frequency is influenced by the desire to provide the wider bandwidth of the voltage loop and by the hardware constrains: available memory for the filter implementation, and the resolution of the processing unit.

From (8) and (9) it can be seen that in order to keep the center frequency and its multiples unchanged as the sampling frequency changes, the ratio of the sampling frequency f_s and the order M of the filter has to remain constant. Consequently, the higher sampling frequency provides wider bandwidth of the voltage loop but also requires the larger memory for the filter implementation.

Figure 3 shows that the filter characteristics improve as the value of the factor r approaches one. Its maximum value r_{max} is

$$r_{max} = 1 - 2^{-(N-1)} \quad (13)$$

where N-is the number of bits of the fixed-point arithmetic unit. In the experimental system it was found that factor r of 0.985, which can be implemented with 8-bit arithmetic gives good characteristics shown in Fig.3.b.

The transfer function of the implemented filter is given by:

$$H(z) = \frac{1 - 0.985\cdot z^{-1} - z^{-40} + 0.985\cdot z^{-41}}{1 - z^{-1} - 0.546\cdot z^{-40} + 0.546\cdot z^{-41}} \cdot \quad (14)$$

II Experimental Results

The comb filter given by (14) is tested in the voltage loop of a completely digitally controlled boost PFC rectifier operating at 200 kHz switching frequency [9]. The rectifier is shown in Fig.5. Using the "frozen coefficients" method [12], we designed a voltage loop with a bandwidth higher than 120 Hz for the worst operation case (the largest instantaneous power and the largest load). Measured transient responses for a load change from 30% to 60% of 200 W are compared in Fig.6 for the case when a conventional, slow voltage loop is used, and the case when the comb filter and the wide-bandwidth voltage loop are implemented. The experimental results show significant improvement of the response with the comb filter implemented inside the voltage loop. The response has smaller dips and overshoots, and enables more optimal design of the PFC power stage and the downstream dc/dc converter. The harmonic distortion of the input current is very low (less than 5 %). Without the comb filter (or some other method of eliminating the harmonics of twice the line
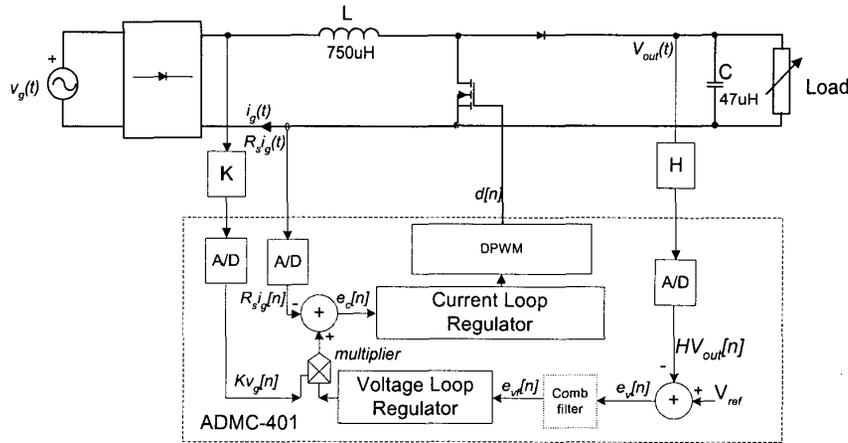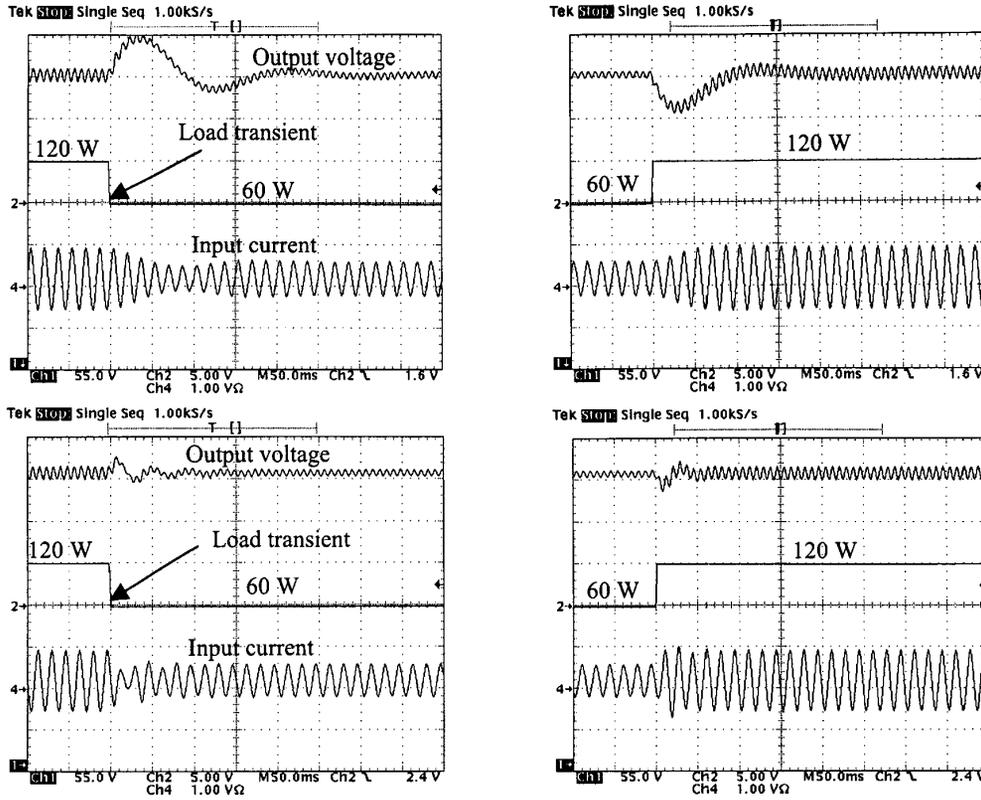

Figure 5: Experimental system

Figure 6: Transient response for the change of load between 60 and 120 W, a) (top two) slow voltage loop without the comb filter and b) (bottom two) with the fast voltage loop and the digital comb filter.

frequency), extending the voltage loop bandwidth results in significant current distortion [1,2,9].

V. FREQUENCY DETECTOR AND SELF-TUNING COMB FILTER

In order to facilitate universal-input operation, it is desirable to automatically "recognize" the line frequency and adjust the filter characteristic accordingly.

Figure 7 shows block diagram of a self-tuning digital comb filter (STCF). The filter tuning is based on the fact that the center frequency of the comb is directly proportional to the sampling frequency (6,8,9).

In order to explain operation of the frequency detector, let us assume that the sampling frequency is not properly selected. In this case second harmonic component will appear at the output of the filter and will cause a high value at the output of the block that performs rectification and averaging, according to

$$y[n] = \frac{1}{N}\sum_{n=1}^{N}e_{vf}[n] \approx \frac{1}{KT_s}\int_0^{KT_s}|e_{vf}(t)|\,dt \qquad (14)$$

where N is the number of samples taken in averaging (or the number of periods K).

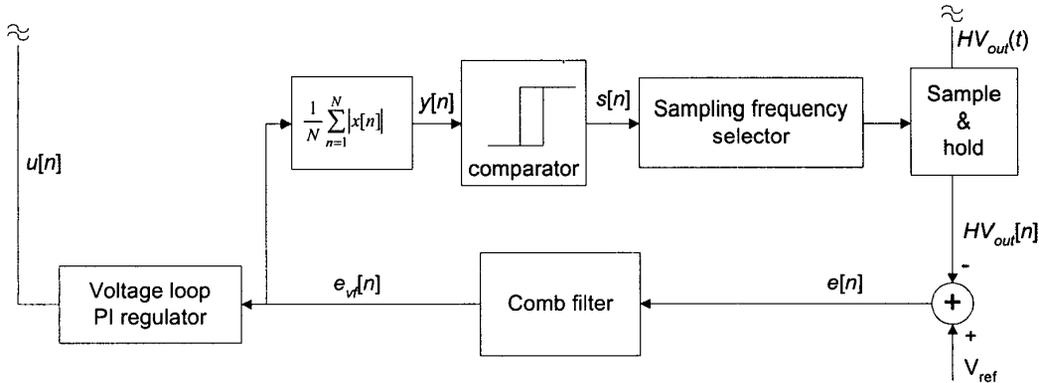The number of samples is selected to ensure that fast

Figure 7: Self-tuning digital comb filter (STCF).

transients of the control signal do not cause changes at the block's output. The high value at the output of the rectifier/averaging block triggers the comparator and gives a signal *sel(t)* to the sampling frequency selector to change the sampling frequency. When the sampling frequency is properly selected, the second harmonic component of the line frequency is eliminated at the output of the comb filter. As a result, the outputs of the rectifier/averaging and the comparator blocks are low, and the frequency selector is locked to the proper sampling frequency.

It is important to note that this self-tuning filter requires a PI regulator in the voltage loop that eliminates the dc component of the voltage error. Presence of a dc component in the error signal could cause triggering of the frequency selector and erroneous operation of the self-tuning structure.

Experimental results in Fig.8 show the error signal at the output of the self-tuning comb filter for a change of the line frequency from 50 Hz to 60 Hz. After the frequency change occurs, second harmonic component can be observed at the output of the filter. The condition characterized with the presence of the second harmonic continues for several line cycles, until the self-tuning structure "recognizes" the new state, asserts the high level of the signal at the output of the rectifying/averaging block, triggers the comparator signal *s(t)*, and adjusts the filter coefficients by adjusting the sampling frequency. Once when the proper sampling frequency is selected, the second harmonic from the filtered error signal is eliminated, causing the low value of *s(t)* and constant sampling frequency as long as the line frequency is stable.
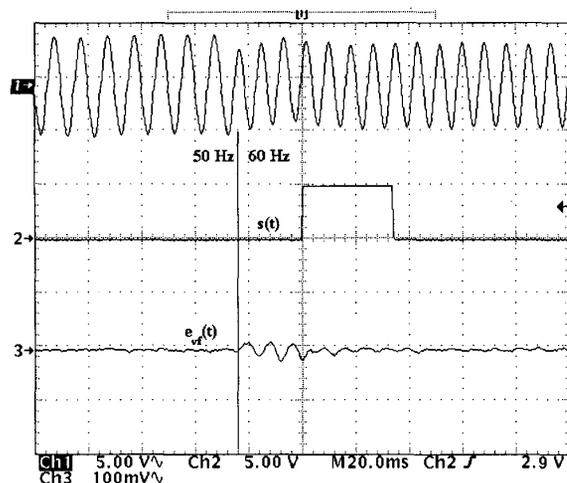

Figure 8: Response of the self-tuning comb filter for the 50 Hz to 60 Hz line frequency change: Ch.1 - output capacitor ripple; Ch.2 – output of the comparator $s(t)$; Ch.3 - filtered voltage error signal $e_{vf}(t)$.

VI. CONCLUSIONS

The self-tuning, digital comb filter (STCF) described in this paper provides expansion of the voltage loop bandwidth in universal-input, low harmonic rectifiers and less conservative design of the power stage and a downstream dc/dc converter. Other advantages are that the structure does not require output current measurement or knowledge of the output capacitance value. The input port of the rectifier behaves as a resistor even when the input voltage is distorted. Operation, design, and implementation of the STCF are described.

Experimental results obtained with a 200 W, boost PFC rectifier confirm improvement of the voltage loop dynamics, and ability of the STCF to operate in the universal supplies.

VII. REFERENCES

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