

# Multimode Digital SMPS Controller IC for Low-Power Management

Nabeel Rahman, Amir Parayandeh, Kun Wang, and Aleksandar Prodić  
 Laboratory for Low Power Management and Integrated Switch-Mode Power Supplies  
 Department of Electrical and Computer Engineering, University of Toronto  
 Toronto, ON, CANADA  
 prodic@power.ele.utoronto.ca

**Abstract**— This paper introduces a novel low-power digital controller for high frequency dc-dc switch-mode power supplies (SMPS) that is well-suited for integration in power management systems of small handheld devices. The controller operates at programmable constant switching frequencies up to 20 MHz and can change mode of operation to improve the overall SMPS efficiency. The key elements of the controller are a high frequency digital pulse-width modulator (DPWM), based on a segmented ring oscillator, and a signal-race based digital pulse-frequency modulator (DPFM). The controller is implemented in a standard CMOS 0.18  $\mu\text{m}$  process and its operation verified both through simulations and experiments.

## I. INTRODUCTION

In existing miniature handheld devices such as cell phones, PDAs, and MP3 players dedicated analog ICs are almost exclusively used to control SMPS. The ICs consume very low power and, usually, operate as constant frequency pulse-width modulator (PWM) controllers that are, because of less wide-bandwidth noise, preferred to variable-frequency solutions. The analog controllers require relatively long design process and need to be almost completely redesigned each time implementation technology changes. As such, they are not suitable for monolithic integration with fast changing digital hardware, on which the majority of portable devices are based. Moreover, in the latest CMOS processes not all functional blocks of analog controllers can be implemented due to very limited supply voltages.

Digital control of low-power SMPS allows easier system integration and, supported by automated design tools, fast transition of designs from one implementation technology to another. Furthermore, the digital control can simplify realization of advanced power management techniques [1,2].

Although the potentials of digital controllers are known, in low-power SMPS they are sporadically used. Compared to analog solutions, they have higher power consumption and lower switching frequency that result in poor efficiency and a larger power stage that negate all digital advantages.

Recent solutions [3-5] demonstrating low-power constant-frequency digital SMPS controllers are still not suitable for monolithic integration with power management systems of handheld devices. They operate at frequencies between 400 kHz and 1 MHz, much lower than commercially available analog controllers that can operate at 5 MHz [6], and, in near

future, are expected to run at frequencies beyond 10 MHz. In addition, the demonstrated systems do not offer a digital solution for pulse-frequency modulation (PFM), which at light loads largely improves SMPS efficiency [3].

In this paper we present a new low-power architecture that allows integration of digitally controlled SMPS in the existing and upcoming handheld devices. The controller, shown in Fig.1, operates at programmable switching frequencies up to 20 MHz and can switch between PWM and PFM voltage regulation modes.

## II. OVERALL SYSTEM DESCRIPTION

The operation of buck converter regulated by the new digital controller, depicted in Fig.1 depends on the value of the *mode* signal. In PWM, *mode* signal is low and the transistor  $Q_2$  functions as a synchronous rectifier reducing conduction losses [7]. At light loads the synchronous rectifier is disabled, (*mode* signal is high) allowing discontinuous inductor current and, consequently, operation in PFM. Most of the controller functional blocks are utilized in both modes of operation. The output voltage reference is set by a low-power low-frequency sigma-delta digital-to-analog converter ( $\Sigma$ - $\Delta$ DAC) [8] and compared to the buck converter output voltage  $v_{\text{out}}(t)$  using a windowed analog-to-digital converter (ADC) [4]. The

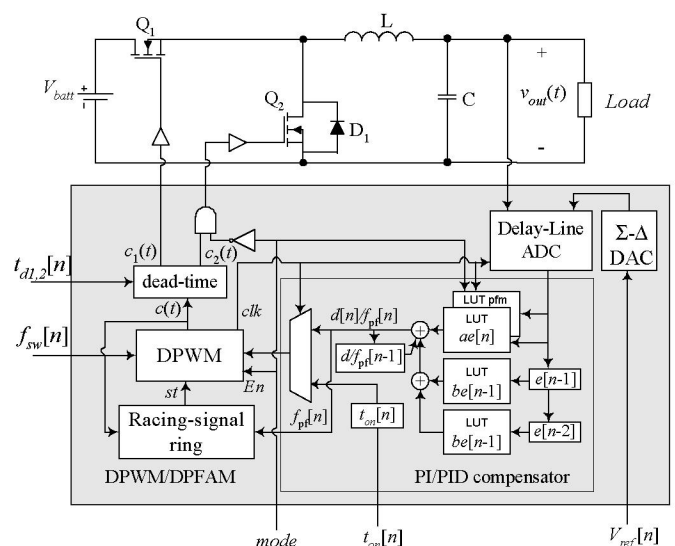


Figure 1. Buck converter regulated by multimode digital controller.

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resulting error  $e[n]$  is then processed by a look-up table (LUT) based PI/PID compensator [4,9] that, using dual set of tables, either creates  $d[n]$  control input for DPWM, or  $f_{pf}[n]$ , frequency control signal of the DPFM. In DPWM, three LUTs are used to implement the following discrete time PID control law

$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2], \quad (1)$$

where pre-stored table entries  $ae[n]$ ,  $be[n-1]$ , and  $ce[n-2]$  depend on the current error value  $e[n]$ , and on the values of error, one and two switching cycles before,  $e[n-1]$  and  $e[n-2]$ , respectively. The discrete-time control law, i.e. LUT entries, is selected in accordance with the procedure described in [9]. When operating in PFM (i.e.  $mode=1$ ) the switching converter behaves as a first-order system and is regulated by changing the switching frequency with a slow PI compensator

$$f_{pf}[n] = f_{pf}[n-1] + a_{pf}e[n]. \quad (2)$$

that employs only one look-up table, LUT\_pfm, containing pre-stored values  $a_{pf}e[n]$ .

The advantage of PI compensator over conventional PFM controllers operating at random switching frequencies is elimination of noise interference. Combined with a programmable block that sets transistor  $t_{on}$  time the PI allows control over the range of switching frequencies and minimizes undesirable noise components that influence portable devices.

To reduce power consumption in both modes the ADC and compensator are clocked at the switching frequency, with  $f_{clk}$  signal produced by the DPWM/DPFM modulator.

In PWM the resulting signal  $c(t)$  is passed to programmable dead-time circuit that prevents simultaneous conduction of transistors  $Q_1$  and  $Q_2$ . In PFM the circuit is disabled.

### III. ARCHITECTURES OF BASIC FUNCTIONAL BLOCKS

All functional blocks of the controller are either fully digital or consist of digital logic and current-starved delay cells, the only analog elements used in the controller implementation. The current-starved cells are selected because of simple structure implantable in latest IC technologies, low-power consumption, and ability to operate at low voltages.

#### A. Segmented-Ring Based Digital PWM

The 8-bit DPWM shown in Fig.2 is based on combination of segmented DPWM and ring oscillator based architectures [5]. However, unlike the segmented DPWM it does not require an external clock and can be implemented on less than 1/8 of the

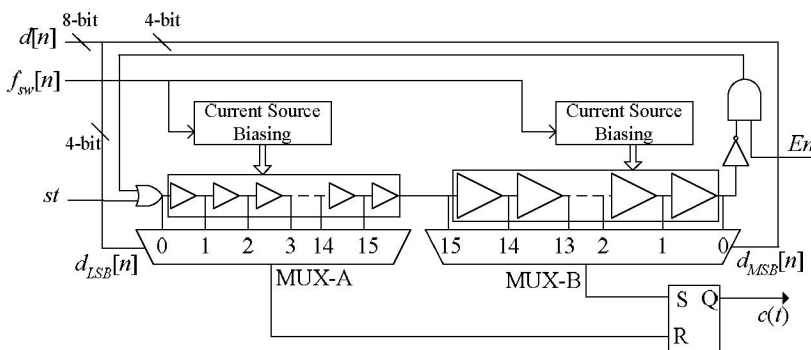


Figure 2. Ring-based segmented DPWM.

area needed for the conventional ring implementation. The size of the DPWM is reduced by replacing a large 256:1 multiplexer (MUX) with two 16:1 MUXs and by weighing the delay cells in a logarithmic fashion.

The two “back-to-back” connected MUXs and delay lines function as a ring oscillator, and the MUXs’ outputs are connected to an SR latch. The first delay line consists of 16 identical fast delay cells. The second line comprises 16 slow cells, where each of them is 16 times slower than those of the first line. The intermediate nodes (taps) of the first line are passed onto MUX-A, and the taps of the slower line are connected to MUX-B.

The 8-bit input  $d[n]$  is divided into two parts. The 4 most significant bits (MSBs) are inputs for MUX-B. They define the rising edge of the pulse-width modulated signal  $c(t)$  and coarsely adjust its duty ratio value. The four least significant bits (LSBs) of  $d[n]$ , inputs of MUX-A, define the falling edge of  $c(t)$  and perform fine adjustment of the duty ratio.

The operation of the segmented-ring DPWM can be described by observing its behavior for a high and low input control duty ratio values. Let us assume that there is a pulse propagating through the ring oscillator and first consider the case when  $d[n]$  is a randomly selected binary number 1110 1000, corresponding to a duty ratio of 0.9065. As the pulse is passing through the ring oscillator, the output of the SR latch will be set to high when it reaches the tap 14 of MUX-B corresponding to 4MSBs of the binary input  $d[n]$ . The pulse now travels through 14 slow cells, then passes through 8 fast delay cells before it reaches tap 8 of MUX-A (value corresponding to 4LSBs of  $d[n]$ ) and resets the SR latch. As a result  $c(t)$  is set to low. The new switching cycles start as soon as the pulse reaches tap 14 of the multiplexer MUX-B. When the input is small, for example  $d[n] = 0001\ 0001$ , the pulse sets the SR latch at the tap 1 of MUX-B, traverses through only one slow and one fast delay cell and, then, resets the output at the tap 1 of MUX-A. This results in low value of duty ratio.

#### 1) Programmable Current-Starved Delay Cell

Figure 3 shows a digitally programmable current starved delay cell and corresponding current biasing circuit.

The delay of this cell depends on the equivalent capacitance seen at the node A and on the current mirrored by the programmable biasing circuit. The current can be programmed in the binary fashion by changing the number of differently sized ( $W/L$ ,  $W/L$ ,  $2W/L$ ,  $4W/L$ , and  $8W/L$ ) transistors conducting at the same time.

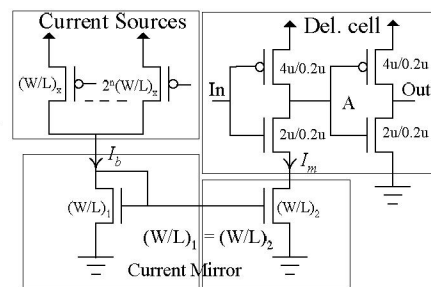


Figure 3. Programmable Current Starved Delay Cell.

### B. Digital Pulse Frequency Modulator (DPFM)

To reduce switching losses, in PFM, the switching converter usually operates at a switching frequency lower than in the PWM mode, and the effective value of “duty ratio” is also significantly smaller.

In handheld applications, the PFM frequency could range from several tens of kHz up to several hundreds of kHz and the period during which transistor  $Q_1$  (see Fig.1) is in on state is measured in fractions of a microsecond. In these applications the power consumption of the controller is limited to several  $\mu\text{W}$  to allow extended battery life when the handheld device is not fully active and behaves as a light load.

In the design of a digital pulse-frequency modulators one of the main challenges is to create long intervals using very fast digital logic. Direct implementation of DPWM based architectures for this application is impractical. Counter based DPFM designs proposed in [10] consume significant amount of power. While the delay-line based implementations do not provide low effective duty ratio and long switching periods without sacrificing large on-chip area.

The novel signal-race DPFM architecture is shown in Fig.4. It allows creation of very long-time intervals using fast digital logic, and can be implemented with low-power hardware. In addition, it allows active control of on-transistor time and consequently operation in combined pulse-frequency / pulse-amplitude regulation mode. The intervals are created with two pulses racing each other around a ring-oscillator. The first pulse is given a head start, while the second pulse propagates slightly faster. The time it takes the second pulse to catch the first pulse, determines off-time interval of PFM signal, while the period between the two starts defines its on-time  $T_{on}$ .

The DPFM has three major blocks. The DPWM described in the previous section, an end of race detector (EoR), and a ring oscillator comprised of SR-latches, current-starved delay cells and inverters.

In DPFM mode the ring oscillator of DPWM is disabled by  $En$  signal (Figs.1 and 2) and the DPWM operates as a delay line. This delay line is triggered by signal  $st$  and creates transistor control signal  $c(t)$  which duration  $T_{on}$  depends on the input value  $t_{on}[n]$ . This signal initiates propagation of two pulses through SR-latch-based ring oscillator. The rising edge of the DPWM-produced signal initiates the first racing pulse and its falling edge starts the second pulse. The initial output state of all SR-latches in the ring is zero. As the first pulse propagates through the ring it triggers sets inputs of the SR-latches. The other pulse, which is delayed by  $T_{on}$ , propagates through inverters and on its way resets the RS-latches. Compared to current-starved cells the inverters have smaller transition time resulting in faster propagation of the delayed pulse. As both pulses propagate through the ring the time distance between them decreases, until they finally meet and all SR-latch outputs are zero. This condition is detected by *end of race* block EoR that also sends  $st$  signal to the DPWM to initiate another pulse, i.e. start new switching cycle.

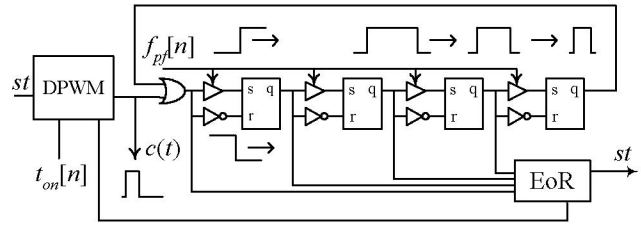


Figure 4. Signal-race based DPFM.

The frequency regulation is performed through the variation of the propagation time of current-starved cells that are implemented as shown in the previous section.

### C. Self-Strobed Delay-Line Analog-to-Digital Converter

The windowed ADC shown in Fig.5 is a modification of the architectures presented in [4,11]. The design is adapted to have faster conversion time and operate over a wide range of input voltages utilizing a small number of delay cells.

To measure the difference between the buck converter output  $v_{out}(t)$  and the reference  $V_{ref}$  created by sigma-delta DAC (See Fig.1) in the range of  $-4 \leq e[n] \leq 4$  the ADC employs two delay-lines. A reference delay-line consisting of a slow cell and  $N_f$  fast delay cells and input voltage line having a slow and  $N_f+4$  fast cells. A digital block consisting of a latch and encoder is connected to the taps of last nine fast delay cells of the input delay-line.

At the beginning of each conversion period  $clk$  signal simultaneously initiates two pulses propagating through the both delay-lines. When the pulse of the reference delay-line reaches its end, it takes a snapshot of the input delay-line and, based on the latched value, encoder determines the error. If pulses propagate through the same number of cells the encoder output  $e[n]=0$ . When the output-line pulse propagates through a larger number of cells the input voltage is larger than reference. Similarly, propagation through a smaller number of cells indicates a lower voltage.

The slow delay cells are used to obtain high ADC resolution without utilization of a large number of fast cells or voltage control oscillators [3,11] that increase hardware complexity and power consumption.

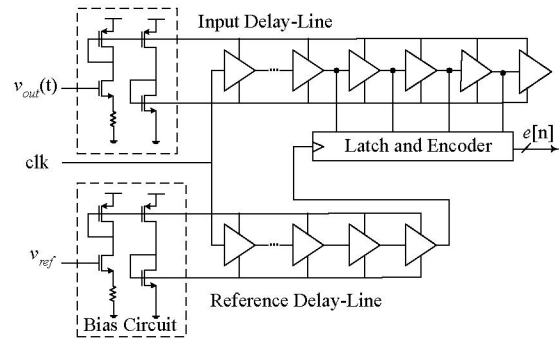


Figure 5. Self-strobed delay-line ADC.

#### IV. SIMULATIONS AND EXPERIMENTAL VERIFICATION

The controller of Fig.1 is implemented in a standard 0.18  $\mu\text{m}$  process and tested with an experimental 3W, 3.3 V buck switching converter. Chip parameters listed in Tables I and II are obtained both through HSPICE simulations.

TABLE I- PARAMETERS OF ON-CHIP IMPLEMENTED DPWM AND DPFM

	Area	Frequency range	Current cons.
DPFM	0.01936 $\text{mm}^2$	20 kHz to 250 kHz	3 $\mu\text{A}$
DPWM	0.008361 $\text{mm}^2$	1 MHz to 20 MHz	4.5 $\mu\text{A}/\text{MHz}$

TABLE II- PARAMETERS OF ON-CHIP IMPLEMENTED ADC

	Area	Current consumption	Conversion time
ADC	0.0275 $\text{mm}^2$	28 $\mu\text{A}/\text{MHz}$	30 ns

The ADC provides quantization steps  $\Delta V_q$  smaller than 1% of  $V_{ref}$  over the full range of operation from 1 V to 2.5V.

Fig. 6 shows experimental waveforms of the DPFM as the frequency control input  $f_{pf}[n]$  changes. They verify operation over a wide range of frequencies needed for a good voltage regulation over wide range of output loads.

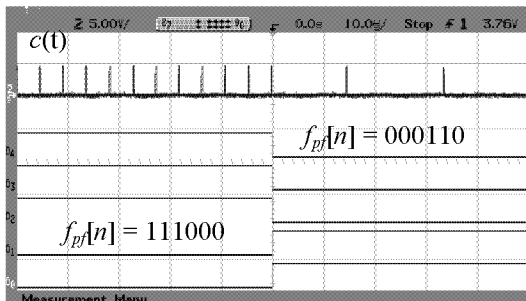


Figure 6. DPFM operation for a sudden change of control input  $f_{pf}[n]$ ; D0 to D4 - five MSB-s of  $f_{pf}[n]$ ; Ch2- PFM output  $c(t)$ .

Figs. 7 and 8 show closed loop operation in DPWM and DPFM mode, obtained with an experimental buck converter operating at 6 MHz. The switching frequency of the controller is intentionally reduced due to the frequency limits of existing power stage components. The experimental results verify tight regulation of the output voltage in both regulation modes.

#### V. CONCLUSIONS

A digital SMPS IC controller suitable for monolithic integration with power management systems of handheld devices is presented. The IC utilizes novel architectures of basic functional blocks DPWM, DPFM, and ADC, to achieve high switching frequency, low power consumption, and operation in different voltage regulation modes that improve overall efficiency. Results obtained with an experimental chip implemented in 0.18 $\mu\text{m}$  process show operation at 20 MHz and very low power consumption, comparable to that of the state of the art analog realizations.

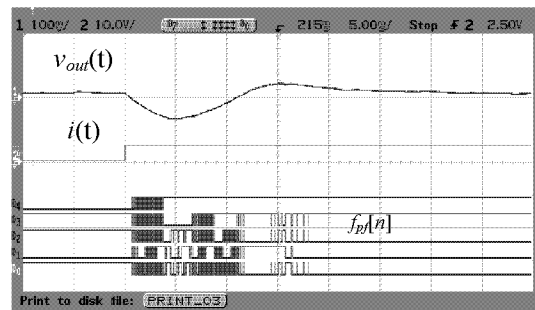


Figure 7. Closed loop operation in PFM voltage regulation mode for the output load change from 1 mA to 2 mA. Ch1:  $v_{out}(t)$ ; Ch2: load current  $i(t)$ ; D0-D4: five MSBs of  $f_{pf}[n]$ .

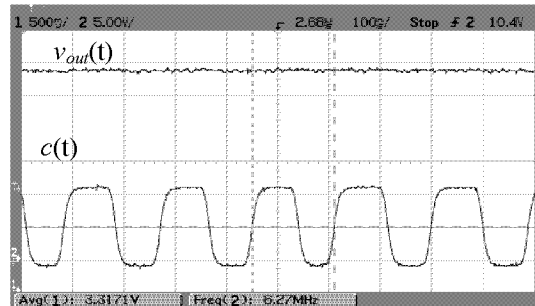


Figure 8. Closed loop operation in DPWM voltage regulation mode at 6 MHz. Ch1:  $v_{out}(t)$ ; Ch2: PWM signal  $c(t)$ .

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