Digital Controller for High-Frequency Rectifiers with Power Factor Correction Suitable for On-Chip Implementation

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Abstract-- ***This paper describes a digital controller for high-frequency single-phase power factor correction rectifiers (PFC) that is suitable for on-chip implementation. To achieve high switching frequency, fast dynamic response, and implementation with a small number of logic gates, the designs of basic functional blocks are optimized. In the outer voltage loop a windowed based analog-to-digital converter (ADC) with adjustable quantization steps is used, to achieve fast dynamic response. The complexity of the current loop realization is significantly reduced through the utilization of a floating reference created by a Σ-Δ modulator and another windowed based ADC. In addition, a segmented ring-oscillator based digital pulse-width modulator (DPWM) is used to eliminate the need for a high frequency external clock and reduce the overall size of the system. The effectiveness of this digital architecture is demonstrated on a 200 kHz, 300 W boost-based PFC experimental prototype.***

***Index Terms*—PFC, digital control, IC implementation.**

I. Introduction

Digital control of switch-mode power supplies (SMPS) offers attractive features, such as superior flexibility, implementation of advanced control and power management techniques, simple transfer of designs from one implementation technology to another (design portability), and realization with a small number of external passive components [1]. Even though these advantages are generally recognized, application specific analog controller integrated circuits (IC) are still predominant in single-phase rectifiers with power factor correction (PFC). This is mostly due to the high complexity of general-purpose functional blocks that have been used in prototypes presented in recent research literature [1]-[6].

A block diagram of a digitally controlled PFC is shown in Fig.1. It consists of a power stage controlled by two feedback loops. The inner, current loop, forces the input current $i_g(t)$ to follow the wave shape of the input voltage. The task of the outer loop is to regulate the output voltage by changing emulated resistance R_e, which is the ratio of the input voltage and current $V_g(t)/i_g(t)$.

It can be seen that a general implementation of this controller requires three ADCs, a processing unit for control laws implementation, and a digital-pulse width modulator (DPWM). An attempt to integrate this architecture using conventional general-purpose components would result in an overly complex IC, whose

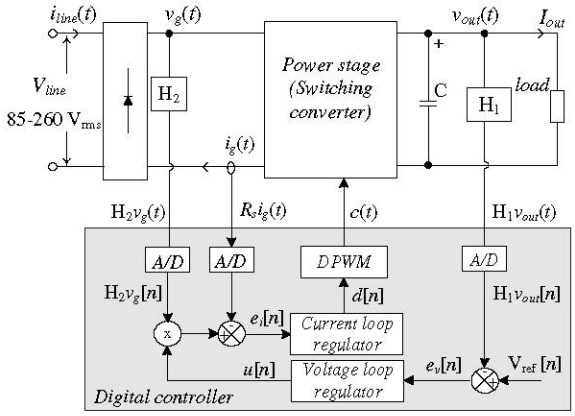

Fig.1. Digitally controlled PFC.

silicon area would be significantly larger than that of less-expensive integrated analog controllers [7] are still preferred choice in PFC applications.

For example, to regulate a PFC at switching frequencies beyond 200 kHz, the ADC for input current measurement is required to sample the current during each switching cycle [5],[6] and produce a digital equivalent of its analog input in several microseconds or less. A general purpose ADC with such characteristics is usually more complex than a complete analog controller consisting of a few operational amplifiers, a pulse generator, and a multiplier]. The ADCs for the output and input voltage measurements are usually over-designed as well. Information about slow-varying input voltage can be acquired less frequently than that about the input current and a full range ADC for the output voltage measurements is usually not necessary. For a properly designed voltage loop, most of the time, the output voltage is around a desired reference and the ADC operates in a very narrow range. Additional problem is the limited frequency of counter-based DPWM [9] that are commonly used in such systems. The DPWM resolution decreases with frequency, and often does not provide satisfactory voltage regulation [10].

The main goal of this paper is to introduce a new digital controller that has optimized architectures of ADCs and DPWM that allow efficient on-chip implementation. To achieve these results basic functional blocks of digital controllers developed for low-power high frequency dc-dc converters are modified [11]-[13]. Namely, windowed-based ADC for output voltage measurements,

floating reference ADC for input current error measurements, a low range compensator and a segmented ring-oscillator based DPWM are combined.
In the following section an explanation of the controller operation is given. Section III gives a description of basic functional blocks. Experimental results verifying proper operation of this system are given in Section IV.

II. Controller Operation

The controller of Fig.2 operates in a similar way as the conventional average-current controller of Fig.1. The ADC of the outer loop creates a digital equivalent of the voltage error $e_v[n]$ that is passed to the voltage loop compensator. The compensator, then, produces a control signal $u\,[n]$ that effectively changes emulated resistance. It is multiplied by the value proportional to the instantaneous rectified line voltage $v_g(t)$, to create the reference for the input current. The difference between this product and a scaled input current, i.e. current error $e_i[n]$, is processed by the current loop compensator. It creates a command $d[n]$ for the DPWM.
However, the main difference between architectures shown in Figs. 1 and 2 is that the two ADCs for input current and voltage measurements and the multiplier of the conventional architecture are replaced with a much simpler structure. In addition, the conventional full-range ADC for output voltage measurement is replaced with another windowed-based ADC with non-uniform and programmable quantization steps. Finally, a segmented ring high-resolution DPWM [12], which unlike conventional counter-based structures does not require a high frequency external clock is used. This DPWM can operate at programmable switching frequencies exceeding 10 MHz and requires very simple hardware for implementation.

III. Architectures of Basic Functional Blocks

This section gives a description of the architectures of the key functional blocks that make this controller structure suitable for on-chip implementation.

A. Voltage loop and the ADC with non-uniform and programmable quantization steps

The voltage loop is designed having two main goals on the mind, simple implementation and fast response to the output load transients.
It consists of look-up table based PI compensator and a windowed based ADC whose input-to-output characteristic around the reference V_{ref} is shown in Fig.3. Its quantization step around reference $\Delta Vq_{|e=0}$, i.e. zero error bin, is larger than the other bins. This non-uniform structure allows direct implementation of a regulation band, i.e. dead-zone, voltage loop controller [14] – [17] that results in very good dynamic response. In this method, the zero error bin of the ADC is set to be larger than the output capacitor ripple at the twice line frequency. In this way, the ripple, which limits the maximum bandwidth of the conventional voltage loop [18] is eliminated, allowing for much faster control. In addition, to eliminate output voltage oscillations at light loads, characteristic for dead-zone controllers [17], the size of the quantization step is made adjustable in accordance with the output load. At light loads it is reduced to accommodate smaller ripple amplitude and prevent low-frequency oscillations inside the zero error bin.
The block diagram of Fig.4.a shows the architecture of the programmable non-uniform ADC.The ADC of is based on the architecture presented in [13]. It consists of two delay lines, a snapshot register, and an error decoder.

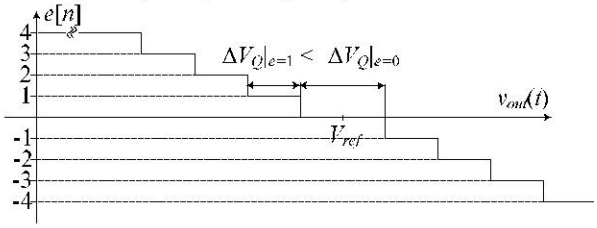

Fig.3. Input-output characteristic of a windowed-based ADC with non-uniform quantization steps.

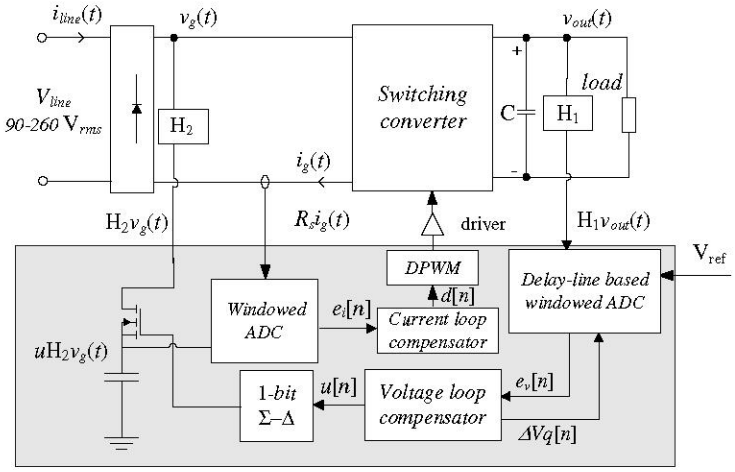

Fig.2. Hardware-efficient digitally controlled PFC.ring architecture

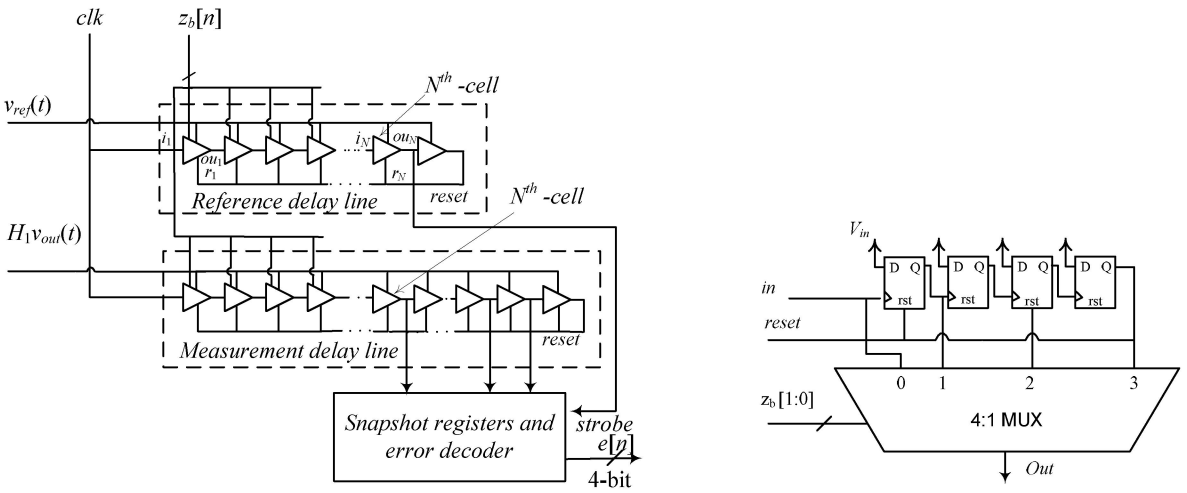

Fig.4. a: (left) Winowed ADC with non-uniform and programmable quantization steps; b: (right) digitally programmable delay cell.

The propagation times of the delay cells, formed of logic gates (D flip-flops), is controlled through the change of their supply voltage. The first line, has N+1 cells whose propagation time is controlled by the reference voltage v_{ref}(t). The other one comprises of $N + M$ cells and its propagation time is inversely proportional to the attenuated output voltage of the PFC (Fig.2). The first N-1 cells of both delay lines are constructed as shown in Fig.4.b, they consist of 4 D flip-flops and a 4-to-1 multiplexer. The number of D flip-flops signal goes through, and hence, the propagation time of this delay cell depends on control signal z_b[n] which regulates the size of the zero error bin.

The conversion process is initiated by the clock signal *clk,* whose frequency is a 1/10 of the switching frequency. This signal triggers both lines and sends two pulses through them. When the pulse propagating through the reference line reaches the N^{th} cell, a strobe signal is created and the state of the measurement line is captured by the *snapshot register*. Based on the number of cells the signal has propagated through, the output voltage error is determined. If the number of cells the signal has propagated is smaller than N the output voltage is lower than v_{ref}(t) and positive error $e[n]$, proportional to the difference in the number of cells is created by the *error decoder*. Similarly, the propagation through a larger number of cells indicates higher output voltage resulting in a negative error. The $(N+1)^{th}$ cell of the reference line is used to reset all the cells before the next *clk* pulse arrives.

It can be shown that for this structure the size of error bin is:

$$\frac{1}{z_b[n](N-1)} Vref = \Delta V_{q|e=0} \qquad (1)$$

Hence by changing $z_b[n]$ the zero error bin can be change as well.

The voltage loop compensator implements the following PI control low:

$$u[n] = u[n-1] + ae_v[n] \qquad (2)$$

where the coefficient a is selected in accordance with the guidelines for fast voltage loop design, given in [19].

B. Current Loop

To allow the use of the obtain the reference value for the simple windowed ADC of Fig.2 for the input current measurements its structure is slightly modified and a floating reference is provided. In this case, the ADC is clocked at the switching frequency and all the delay cells of the same type are used. The floating reference is formed with a single-bit Σ-Δ modulator a transistor and a filtering capacitor. This simple structure eliminates the need for the ADC for input voltage measurement and digital multiplier, which are significantly more complex devices. It should be noted that, since the filtering capacitor is supplied from the input line, its voltage is proportional to uV_g(t), where $u(t)$ is the control value from the voltage loop.

Since this structure operates in closed loop it behaves similar to a successive approximation ADC. The current loop forces the voltage across the filtering capacitor to be close to the value proportional to the input current and the need for a full range fast ADC for input current measurement is eliminated as well.

Furthermore, since the range of the current error signals $e_i[n]$ is limited, the use of small look-up table based PID compensator [15] is enabled. Consequently, the need for a high-speed processor for digital control law implementation is also eliminated.

C. Segmented-Ring Digital Pulse Width Modulator

To implement an 8-bit digital-pulse width modulator the a segmented-ring architecture [12] is used. It is a modification of the conventional based ring-oscillator-based structure presented in [9]. Compared to the original architecture, the segmented ring requires much smaller multiplexer, which results in order of magnitude smaller silicon area.

The DPWM is used both to create control waveforms for the power stage and to provide the clock signal for the entire system.

IV. Experimental Results

Based on the block diagram shown in Fig.2 a digital controller combining an FPGA system and custom-made integrated circuits was designed and tested with a 300 W boost-based PFC. To accommodate limitations of the existing switching components the switching frequency was limited to 200 kHz, even though the controller can support operation at frequencies exceeding 2 MHz.

A. Steady-state operation

Fig.5 shows steady-state operation of the experimental system. It can be seen that the input current accurately follows the input voltage waveform. Results of measurement of the power factor measurements showed that a power factor above 0.98 can be achieved for the output loads ranging from 20 % to 100% of the rated power. The results also showed a very small total harmonic distortion of less than 5% over the above mentioned range.

B. Load-transient performance

Experimental results demonstrating load transient response are shown in Fig.6. It can be seen that this controller has very fast dynamic response. Compared to conventional solutions, having slow output voltage loop, this implementation has several very important advantages. It allows for a significant reduction of the size of the output filter capacitor of the power stage. In addition it minimizes the current and voltage stress on the power stage components as well as on a downstream dc-dc converter, which is the most common PFC's loads.

V. Conclusions

A digital controller for high-frequency PFCs is introduced. It is shown that by utilizing a floating reference ADC for input current measurement and windowed ADC with non-uniform quantization steps for output voltage measurement overall structure of the controller can be significantly simplified. An effective operation of this digital controller is verified through experiments.

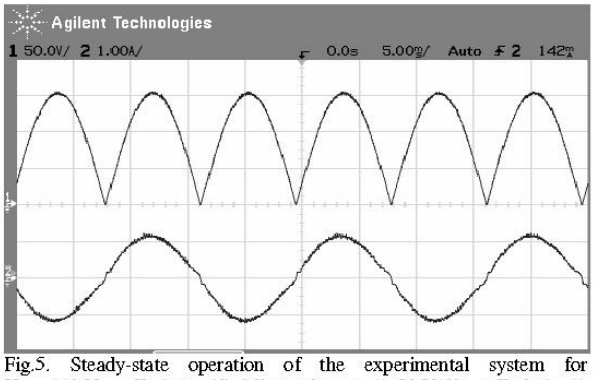

Fig.5. Steady-state operation of the experimental system for V_{line}=110 V_{rms}, Ch-1: rectified line voltage $v_g(t)$ 50 V/div ; Ch-2: $i_{line}(t)$ 0.5 A/div

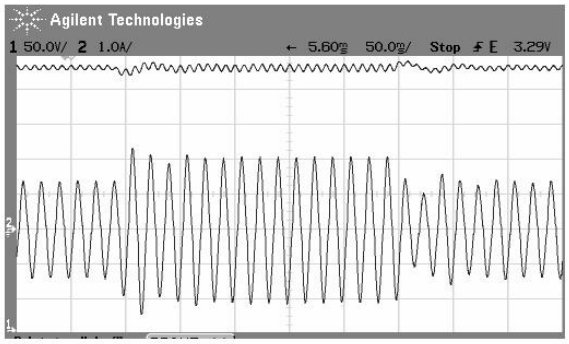

Fig.6. Load transient response of the fast dead-zone controller for load change between 100 W and 175 W. The input line voltage is: (a) V_{line} =110 V_{rms}, Ch-1: $v_{out}(t)$ 10 V/div – ac ; Ch-2: $i_{line}(t)$ 1 A/div

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