High-Power Density Hybrid Converter Topologies for Low-Power Dc-Dc SMPS

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***Abstract*-This paper gives a review of several emerging dc-dc converter topologies that combine capacitor-based and inductive converters in single hybrid converter structures. It is shown that, compared to the conventional topologies, the hybrid buck converters allow for a drastic reduction of the inductive components while minimizing switching losses and improving the overall power processing efficiency. Therefore, the hybrid converters result in a higher power density. As examples, buck with merged capacitive divider, a two-phase interleaved buck, and a differential buck-based multi-output power module for mobile applications are shown. The presented converters have up to four times smaller inductor volume and, at the same time, about 12% lower losses.**

I. INTRODUCTION

Power management systems of modern portable devices, computers, and numerous other applications incorporate a large number of low-power switch-mode power supplies, processing power from a fraction of watt to several hundreds of watts. The reactive components of these SMPS, especially inductors, take a significant portion of the overall device weight and volume. In numerous applications, they occupy much more than 25% of the overall device volume [1], and, as such, are a large obstacle to further system minimization. Also, the power processing efficiency of these SMPS is usually significantly smaller than that of the converters processing more power, increasing cooling requirements and, in battery-powered application, affecting operating time.

A number of different methods for minimizing the volume of the reactive components [2]-[9], have been proposed in the past. Generally, those can be divided in the frequency based and topological solutions. The frequency based methods [2] increase effective switching frequency of the converter to minimize the filter requirements at the expense of larger switching losses.

On the topological side, arguably, among the most interesting are switched-capacitor (SC) converters [3]-[7], that eliminate the inductive components. The SC converters show advantages in terms of power density and power processing efficiency for certain fixed voltage conversion ratios. However, the absence of the inductor in those structures causes voltage regulation problems and negatively affects power processing efficiency (or the system volume) in applications where the conversion ratio is not fixed [4]. Therefore, the use of SC in typical applications of interest, where the load changes frequently and input voltage is not constant, is fairly limited. To eliminate the previously mentioned problems, cascade connections of a SC and a conventional buck (Fig.1) have been proposed in [7]-[9]. The cascaded topologies eliminate the voltage regulation problem and have much smaller inductor than the conventional buck. However, these solutions often increase the resistance of in the conduction path and, consequently, suffer from increased conduction losses. The conventional cascaded solutions also require a relatively bulky intermediate capacitor (C_{sc} of Fig.1) for energy transfer and balancing of the capacitor cells.

The main goal of this paper is to review several recently emerged hybrid converter topologies [10]-[13] that eliminate the drawbacks of the previous two-stage solution. As, shown in Fig.1, *the hybrid converters merge the capacitive and inductive converter in a single structure such that components are shared between them and/or the need for a bulky intermediate capacitor is eliminated.*

In the following sections, the principle of operations of three types of topologies that perform commonly required functions in power management system of interest are reviewed. Namely, a buck converter with a merged

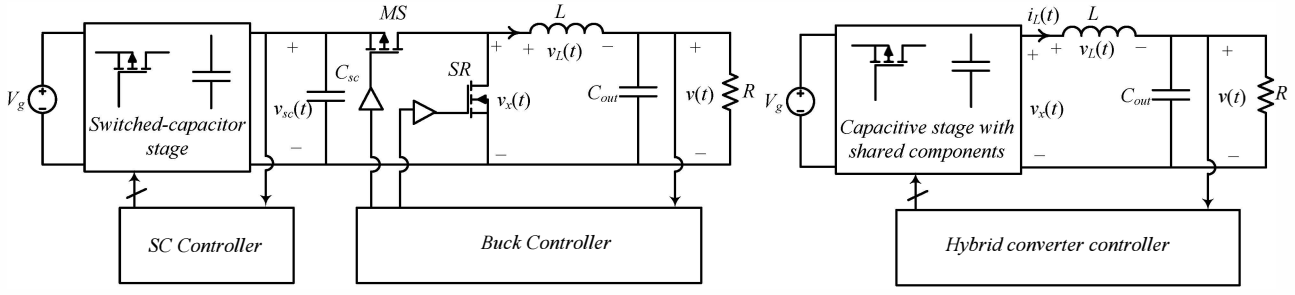

Fig.1. Cascaded switched-capacitor (SC) and buck converter topology (left) and hybrid converter (right).

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capacitive divider [10], a two-phase interleaved buck [11], and a multi-output power management module utilizing differential buck connection [12] are shown. In comparison with the conventional buck based solutions the hybrid converters reviewed here require much smaller inductor and have better power processing efficiency. Both of these result in a significant increase in the power density of the hybrid structures. To achieve these advantages, all of the presented hybrid converters utilize the principle of reduced inductor volt-second product, which is reviewed in the following section.

As demonstrated in the other related work [14],[15], the hybrid conversion principles reviewed in this paper apply not only for buck-based converter topologies but also for boost-based and other indirect energy transfer converters, used in applications such as rectifiers [14] and inverters [15].

II. Minimizing the Inductor and Switching Losses Through Voltage Swing Reduction

To analyze the fundamental principle of hybrid converters operation, we can start from the expression for the steady-state inductor current ripple [2]. For a general inductive converter operating at a constant switching frequency f_{sw}, with a duty ratio D the inductor ripple can be expressed as

$$\Delta I_{ripple} = \frac{|V_{L\_on}|}{2L}\frac{D}{f_{sw}}, \quad (1)$$

or

$$\Delta I_{ripple} = \frac{|V_{L\_off}|}{2L}\frac{1-D}{f_{sw}}, \quad (2)$$

where, V_{L_low} and V_{L_high} are the voltages applied across the inductor during the on and off state of the main converter switch, respectively, and L is the inductance value. For a conventional buck the two values are:

$$V_{L\_on} = V_g - V \quad \text{and} \quad V_{L\_off} = -V, \quad (3)$$

where V_g and V are the converter input and output voltage values, respectively.

To minimize the ripple amplitude and, therefore, reduce the inductor, most commonly the switching frequency is increased. The main drawback of this solution is that, at the same time, switching losses and the inductor core losses are increased negatively affecting the overall power processing efficiency.

In hybrid and cascaded topologies of Fig.1, the inductor is reduced by minimizing V_{L_on} or/and V_{L_off}, resulting in consequent reduction of the inductor volt-second product. In the following section it will be shown that the reduction of the V_{L_low} or/and V_{L_high} values can be achieved without the use of bulky intermediate capacitors existing in the straightforward cascaded solutions [7]-[9]. It will also be demonstrated that the hybrid architectures not only allows for a significant minimization of the inductors but also reduce the voltage stress across the switches, minimizing the switching losses and, at the same time, allowing for minimization of the conduction losses.

III. Buck Converter with Merged Active Capacitive Divider

The buck converter with merged capacitive divider [10],[11] is shown in Fig.2, together with equivalent circuits describing its operation. This converter can also be viewed as a topology obtained through a source-load inversion [2] of a three level boost converter [15]. The converter consists of the active capacitive divider, four

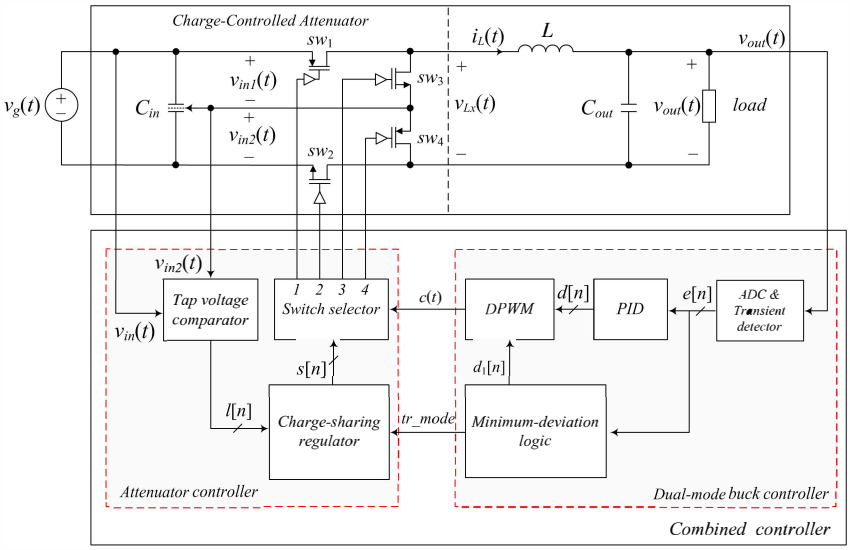

Fig.2. Buck converter with merged capacitive divider [10].

switches, and the downstream buck stage. Here, as shown in Fig. 2, the downstream portion of the converter and the active capacitive divider C_{in} share the same switches. To eliminate the need for a balancing and intermediate capacitors existing in conventional SC converters, in this topology, the buck inductor is used for the balancing of the capacitor cells.

The operation of the converter can be understood by looking at the equivalent circuits of Fig.3. When the divider capacitors are balanced, i.e. voltage $V_g/2$ is across both of them. The switching sequence is performed over two switching periods, where $T_s=1/f_{sw}$ is the switching period. The converter passes through the following modes $a - b/d - c - b/d$, such that, as described in [10], the mode a starts at the beginning of the switching period, mode c starts at T_s, and both of these modes last for DT_s time. Ideally, for perfectly matched components and the duty ratio value, this operation results in the same amount of charge taken from both capacitors and equal voltage sharing. In the case of a mismatch causing unbalanced voltages, the sequence is altered such that more current is taken from the capacitor with higher voltage, until the balance is regained.

It can be seen that in this converter $V_{L\_on} = (V_g/2 - V)$ is lower than that of the conventional buck, resulting in a reduction of volt-second product and a consequent reduction of the inductor value.

By looking at Fig.2 it can also be seen that the blocking voltage of all is $V_g/2$, i.e. half of the value of the conventional buck. This reduction of the voltage stress allows for a significant reduction of switching losses and for the use of a transistors with lower voltage rating that for the same amount of silicon used have about four times smaller on resistance [16]. As a result, a drastic reduction of both switching and conduction losses with this topology is possible.

A. Extension to the two–phase topology

Fig.4 shows extension of the buck with merged capacitive divider to a two phase case [12], where, again, the

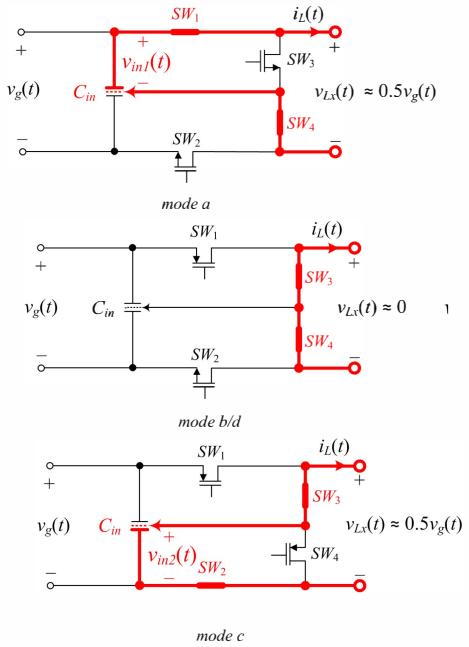

Fig.3. Modes of operation of the buck converter with a merged capacitive divider.

inductors of the downstream portion of the converter are balancing the capacitor divider taps. Operating modes of the converter are shown in Fig.5. In this case, the charging of the capacitive divider is performed through the input filter and Q_1, during the period when the SR switch of the upper phase (transistor Q_9) is turned on. The discharging, and balancing of the capacitors is performed with the inductors of the corresponding buck phases. In this case again, V_{L_on} in both converter phases is reduced to $V_g/2 - V$ and the blocking voltages of all components are reduced to a half of those needed in conventional topologies. This topology also provides inherent equal current sharing between two phases [7] eliminating the need for current balancing circuits.

In the implementation shown in Fig.4 the charging of

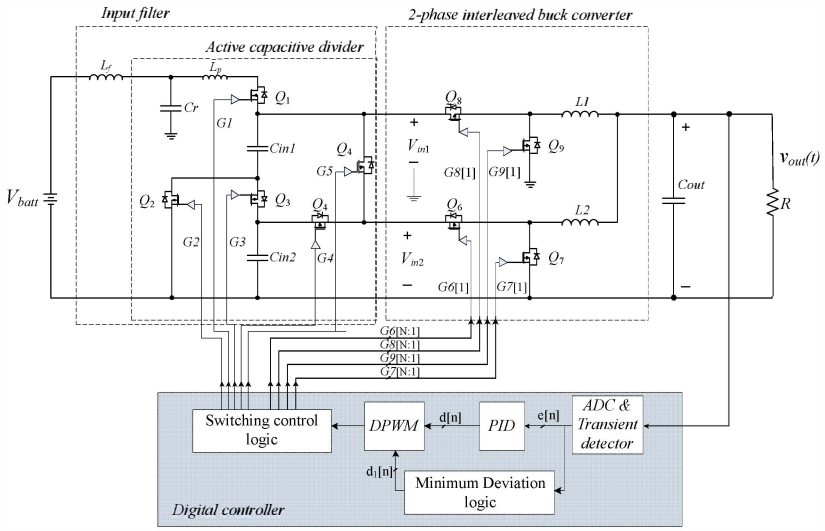

Fig.4. Two phase buck converter with merged capacitive attenuator [12].

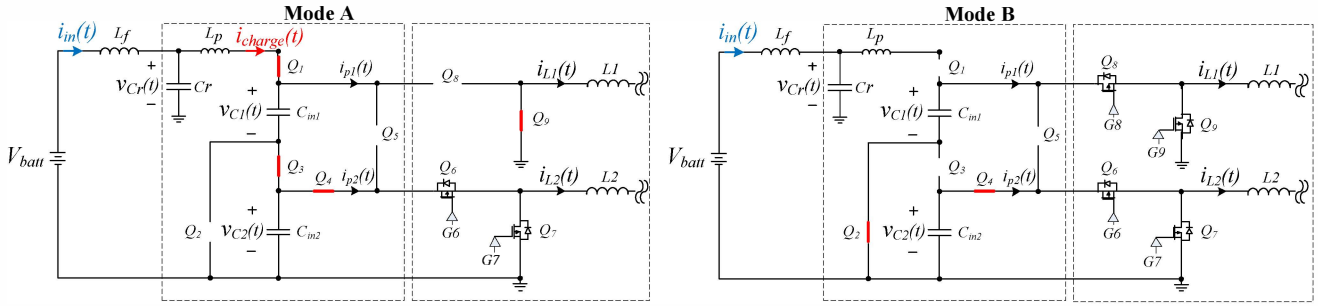

Fig. 5. Operating modes of a two phase buck with merged capacitive divider: adiabatic charging of the capacitors (left) discharging and balancing (right).

both capacitors is performed through Q_1 and the resonant tank L_r-Cr, which provides adiabatic capacitor charging and, therefore, minimizes the losses of Q_1.
It should be noted that even though both of the presented topologies require a larger number of switches than the conventional ones, the total conduction losses are not increased, due lower voltage rating of the switches and, consequently, smaller on resistance values.

IV. Multi Output Hybrid Power Management Block Based on Differential Buck Connections

Hybrid converter topologies can also be utilized at the system level, to increase the power density of power management systems in portable applications.

A typical architecture of a power management system for a battery powered applications is shown in Fig.6. The system of consists of a multiple buck converters, supplied by a bus voltage. The buck converters provide well-regulated voltages for the dedicated functional blocks, such as various data processors and memory. In these applications the reactive components take a significant portion of the overall device volume that depending on the application can vary between 12% and 80% of the overall device volume [1], [11].

Fig.7 shows a hybrid power management structure. In this architecture the sharing of the components is performed such that the capacitive string of the front-end multi-output switched-capacitor converter (MoSC) also acts as the input filter capacitor [2] of the downstream buck converter, i.e. replaces C_{bus} of Fig.6. The downstream buck converters are connected differentially to the output taps of front-end stage. The tap voltages are set such that at the terminals of the buck converters the voltages are slightly higher and slightly lower than the desired output voltage, rather than changing the switching node voltage between the full bus value and the ground. As a result a large reduction in V_{L_on} and $V_{L\text{-}off}$ values (volt-second products) is obtained and, at the same time, the blocking voltages of the switches are reduced.
A practical implementation of this topology for a typical battery-powered application is shown in Fig.8, and the inductor value reductions in comparison with a conventional architecture (Fig.6) operating with the same

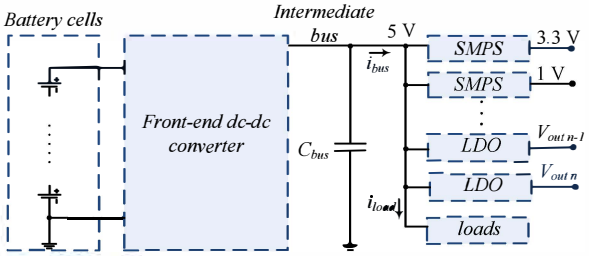

Fig.6. Conventional power management system of a battery-powered device.

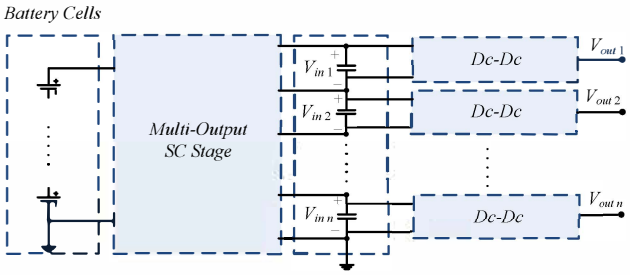

Fig.7. Multi-output switched capacitor (MoSC) based hybrid converter (power management block) based on differential buck converter stages.

input and output voltages are shown in Table 1. The table compares efficiencies and the volumes of the components for two cases, when the buck converters of the hybrid architecture operate at the same frequencies as those of the conventional system and when those converters operate at two times larger frequencies.
It can be seen that for the operation of both system at the same switching frequency the inductance values are reduced up to 50% and the reduction in switching losses of up to 56% is achieved. The table also shows that for the case when a portion of the savings on the switching losses is traded for operation at the higher frequency the inductor can be reduced by up to four times while maintaining significantly smaller switching losses.
Results of efficiency comparison measurements for a 1 V output obtained from a 2-cell Li-ion battery-powered system are shown in Fig.9. The results confirm that with the MoSC hybrid topology significant efficiency improvements are obtained throughout the whole

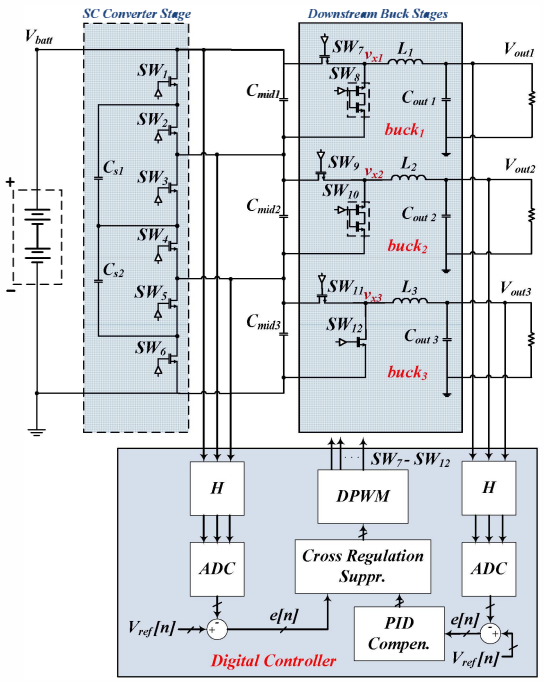

Fig.8. Multi-output hybrid converter based on differential buck converter stages [13].

operating range confirming that both volume reduction and efficiency improvements are obtained with the hybrid architecture.

TABLE I
INDUCTOR VOLUME AND SWITCHING LOSS REDUCTION

	$V_{s\ norm}$	$L_{\ norm}$	$P_{sw\ norm}$	$f_{sw\ norm}$
Dual-input buck 3.3 V	0.44	0.49	0.44	1
Dual-input buck 1 V	0.44	0.68	0.44	1
Dual-input buck 3.3 V (incr. f_{sw})	0.44	0.25	0.88	2
Dual-input buck 1 V (incr. f_{sw})	0.44	0.34	0.88	2

V. CONCLUSIONS

A review of three hybrid topologies combining a switched-capacitor (SC) and buck converter in single structures is given. It is shown that by sharing components and utilizing the SC to reduce inductor volt-second product drastic reduction of inductive components can be achieved and, at the same time, significant power processing efficiency improvements obtained.

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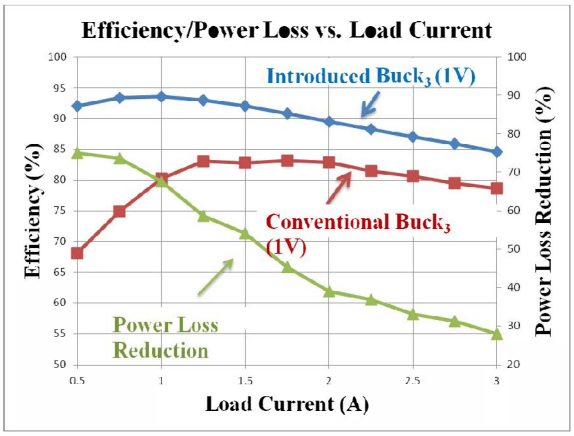

Fig.9. Efficiency comparisons of the dual-input buck of the MoSC based architecture and the conventional downstream converter.

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