# Limit-Cycle Oscillations Based Auto-Tuning System for Digitally Controlled DC–DC Power Supplies

Zhenyu Zhao, *Student Member, IEEE*, and Aleksandar Prodić, *Member, IEEE*

***Abstract*—This paper introduces a new method and system for parameter extraction and automated controller adjustment, suitable for low power digitally controlled dc–dc switch-mode power supplies (SMPS). The system allows closed-loop calibration throughout regular converter operation. During a short-lasting test phase, SMPS parameters, such as output capacitance and load, are estimated by examining the amplitude and frequency of intentionally introduced limit cycle oscillations in duty ratio control variable as well as from its steady state value. Accordingly, a digital compensator is automatically constructed to provide fast dynamic response and good output voltage regulation. In addition, the load estimation data are used for improving efficiency of a converter having segmented transistors. It is performed through a selection of driving sequence resulting in minimized sum of switching and conduction losses. The effectiveness of the system is demonstrated on an experimental 400 kHz, 9 V-to-3.3 V, 10 W, digitally controlled synchronous buck converter.**

***Index Terms*—Auto-tuning, digital control, limit-cycle oscillations (LCOs), low-power dc–dc converters.**

## I. Introduction

DIGITAL control offers features that can improve characteristics of low-power high-frequency switch-mode power supplies (SMPS) for battery-powered handheld devices, consumer electronics and other similar applications. These include flexibility, realization with a small number of passive components [1]–[5], low sensitivity to external influences [6], [7] and availability of automated design tools.

On the other hand, in low-power SMPS, some of the most attractive advantages of digital control have not been fully utilized. In particular, auto-tuning controllers [8]–[12] that significantly improve dynamic response, efficiency, and reliability are rarely used. Those controllers usually perform a two-step procedure. During the first, system identification (SI) phase, the controller actively monitors system behavior and "learns" about its properties through parameters extraction from the feedback loop. Then, in the second phase, the controller accordingly adjusts its own operation, i.e., performs auto-tuning, to accommodate any system changes (uncertainties) and improve the system's characteristics. The auto-tuning controllers are widely employed in large-scale systems, such as power or chemical plants. They compensate for various uncertainties, including temperature and load variations, aging, changes in the number of system elements, and partial failures [8].

The main reason for the absence of auto-tuning controllers in low-power converters is their complexity. Conventional systems usually use hardware whose complexity and power consumption exceed that of a complete low-power dc–dc converter. This is mostly due to high computational demands of commonly used auto-tuning techniques [8]–[12].

Recent publications [13]–[16] show simplified auto-tuning controllers for SMPS. In [13] and [14] a system utilizing pseudo-random binary sequence (PRBS) is presented. The main disadvantage of that implementation is that, during SI phase, the SMPS operates without output voltage regulation. A significantly simpler system, based on an adaptive linear prediction error filter (PEF), is proposed in [15]. That system utilizes a self-learning concept. Upon disturbances occur, the voltage loop compensator gradually adjusts its coefficients until the optimal control law is achieved. There, it is assumed that a repetitive disturbance of the same type always occurs and that in each step the controller "learns" more about it. However, the proposed solution uses a PD compensator that does not provide good steady-state regulation. The authors also do not address problems of nonrepetitive disturbances and of those causing possible system instability. An effective relay-based auto-tuning system is presented in [16]. In that solution, during the SMPS start-up a relay causing oscillations at the system resonant frequency is introduced. Then, through several iterative steps a PID compensator auto-tuning is performed by examining the frequency of the introduced oscillations. The performance of that auto-tuner has not been verified for the regular system operation (upon the start-up). This is mostly due to the potential voltage regulation problems, caused by the use of analog-to-digital converter for the output voltage measurement during SI phase.

The main goal of this paper is to present a new hardware efficient parameter extraction and auto-tuning system for digital pulse-width modulation controlled SMPS shown in Fig. 1. The system utilizes information from intentionally introduced limit-cycle oscillations (LCO) of digital pulse-width modulator (DPWM) control variable $d_c[n]$, as well as the variable's steady-state value, to achieve the following features:

- closed loop calibration during regular converter operation with significantly improved voltage regulation compared to the previous solutions;
- fast compensator adjustment through a single process containing both SI and auto-tuning;
- estimation of the output load and capacitance values, allowing power supply "health monitoring" and dynamic mode changes, to improve efficiency over the full range of operation.

Manuscript received August 12, 2006; revised March 14, 2007. Recommended for publication by Associate Editor K. Smedley.

The authors are with the Electrical and Computer Engineering Department, University of Toronto, Toronto, ON M5S 3G4 Canada (e-mail: zhenyu@power.ele.utoronto.ca; prodic@power.ele.utoronto.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2007.909307

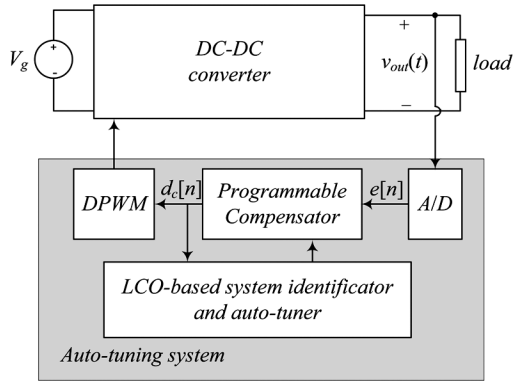



Fig. 1. SMPS with an LCO-based auto-tuning system.

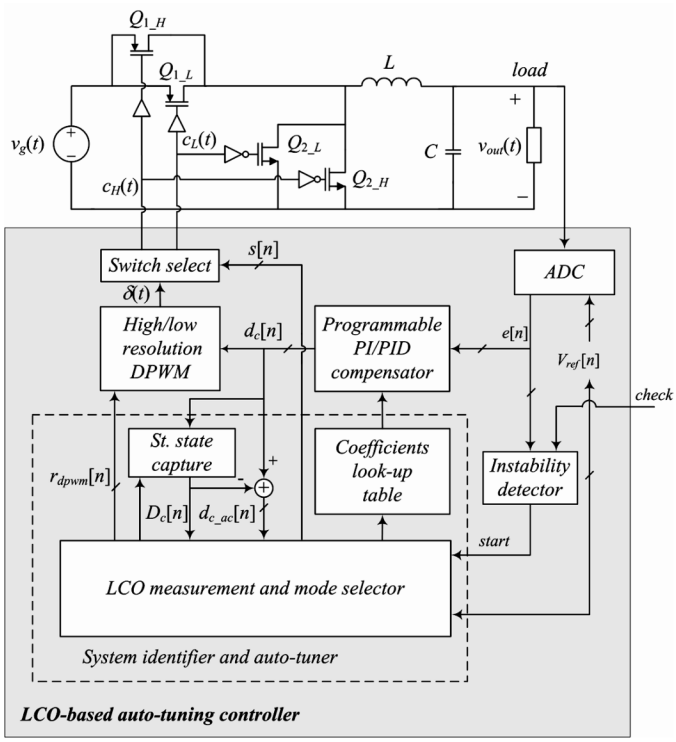



Fig. 2. LCO-based auto-tuning controller regulating operation of a buck converter.

This system can also be used to minimize stability problems in distributed power architectures (DPA) [17]–[19] and parallel converters [20]. Furthermore, in future, it could serve as a basis for the development of universal digital controllers. They will be able to operate with various power stages without any need for a prior compensator design. Ideally, once connected to a power stage, the universal controller will be able to extract system parameters and adjust mode of operation to result in a fast dynamic response and high efficiency in all operating conditions.

In the following section we describe the system operation. Section III briefly describes limit-cycle oscillations (LCO) phenomena and explains how they are used for SMPS parameters extraction. The relations between LCO features and system parameters for buck and boost converters are also derived. In that section, we also address influence of a nonnegligible inductor resistance on parameter estimation and related stability problems. In Section IV we describe the architecture of a programmable compensator and power estimator block for improving converter efficiency. Section V shows experimental results obtained with a prototype utilizing this auto-tuning concept.

## II. System Operation

The operation of the LCO-based auto-tuning controller is demonstrated on the SMPS of Fig. 2, showing the controller regulating a synchronous buck converter with segmented switches. In this implementation, both the main switch and synchronous rectifier are replaced with two differently sized parallel transistors. Transistors $Q_{1\_L}$ and $Q_{2\_L}$ have larger turn-on resistances but smaller gate capacitance, i.e., lower switching losses, compared to those of $Q_{1\_H}$ and $Q_{2\_H}$.

The process starts when a disturbance causing potential instability occurs. Such event is identified by *instability detector* [14] and the auto-tuning begins. The auto-tuning can also be initiated with an external *check* signal, and performed on a regular basis.

The auto-tuning controller operates on a similar principle as the relay system presented in [16]. However, in this case, instead of a relay digital-pulse width modulator (DPWM) is used. To intentionally introduce small limit cycle oscillations (LCO) in $d_c[n]$, the controller temporary reduces the resolution of the DPWM. During this short-lasting phase power stage corner frequency, output capacitance and load are estimated from the amplitude and frequency of the ac component of the signal $d_{c\_ac}[n]$ as well as from its steady state value, $D_c$ [n] and the known digital voltage reference $V_{ref}[n]$. The $D_c[n]$ is obtained with *steady-state capture* block. It captures the control value during the regular converter operation immediately preceding auto-tuning process. In this way the need for a low-pass filter is eliminated and a fast extraction of the steady state obtained with a very simple hardware.

Based on collected information, appropriate coefficients for PID compensator are selected from a set of pre-stored look-up table values. In addition, to improve the overall efficiency, the output load is estimated and transistors driving sequence selected accordingly. The selection is performed by the signal $s[n]$ controlling *switch enable* block. The larger transistors $Q_{1\_H}$ and $Q_{2\_H}$ are disabled when the light loads are estimated, while at heavier loads all four transistors are enabled. Once all adjustments are completed, the controller restores high DPWM resolution reestablishing regular system operation.

As it will be described in more details in the following sections, the use of the DPWM instead of a relay results in much better voltage regulation during auto-tuning process, and consequently allows closed-loop system calibration. This is because the *system identification is based on the observation of the changes in the duty ratio control value $d_c[n]$ which do not cause significant output voltage variations*. As a result this system provides not only better voltage regulation but also eliminates possible stability problems existing in systems having only initial auto-tuning.

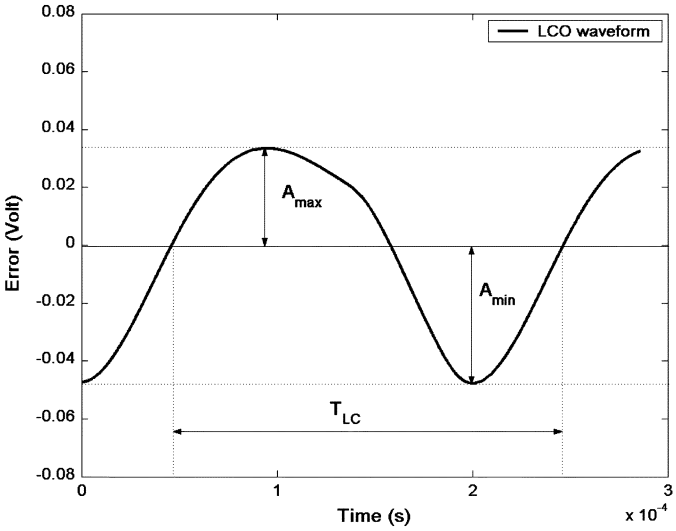



Fig. 3. Typical waveform of limit-cycle oscillations.

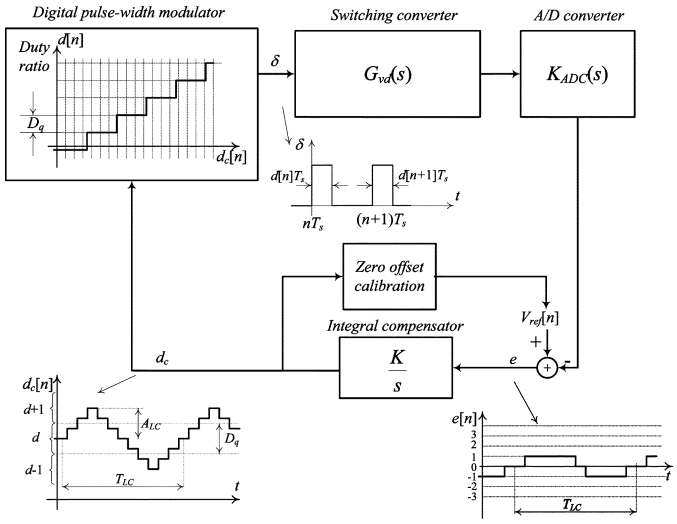



Fig. 4. Model of the LCO-based auto-tuning system during system identification.

## III. Parameter Estimation From Limit-Cycle Oscillations

A specific property of digitally controlled SMPS, as the one of Fig. 1, is that small self-oscillations of the output voltage around the reference could occur in steady state. These oscillations are caused by nonlinear quantization effects in the analog-to-digital converter (ADC) and the digital pulse-width modulator (DPWM). The DPWM produces a discrete set of duty ratio values, meaning that only a finite number of steady-state voltages can be obtained. When the resolution of the DPWM is low, compared to that of the ADC, for some operating conditions quantized DPWM outputs cannot result in steady-state zero error, i.e., $e[n] = 0$. Then, the voltage loop compensator containing an integrator changes the duty ratio control signal $d_c[n]$ between two or more adjacent discrete duty ratio values and the oscillations known as limit cycling (LCO) occur. The problem of LCO in digitally controlled dc–dc SMPS and the conditions for their elimination are extensively analyzed in [21], [22].

Although undesirable in steady state, limit cycle waveforms contain useful information about the controlled system. Fig. 3 shows a typical LCO waveform.

It is a nonsymmetric signal characterized by its maximum and minimum amplitudes $(A_{\max}, A_{\min})$ and period, $T_{\rm LC}$. In a digitally controlled SMPS these three distinctive features depend on the values of power stage inductance, output capacitance and load. They also depend on $V_g$, the input voltage of the power stage and compensator parameters. Since in digital controllers the compensator coefficients are usually known, LCO features $A_{\max}, A_{\min}$ and $f_{\rm LC} = 1/T_{\rm LC}$ can be used for the estimation of any other three system parameters. However, the extraction of parameters from nonsymmetric LCO usually requires complex mathematical tools, such as $A$ -functions [10], which give little insight in the system's physical behavior. For that reason, we use symmetric LCO and analyze their amplitude and frequency only. To compensate for the lost data, we combine these two LCO features with other readily available information from the digital control loop. Namely, the dc value of $d_c[n]$ and the output voltage reference $V_{\rm ref}[n]$.

### A. Introduction of LCO and System Identification

Fig. 4 shows a model of the auto-tuning controller during system identification (SI). In a general system like this, the SI can be performed by placing a relay in the loop and measuring the frequency and amplitude of the oscillations at the input of the relay [10]. In [16] the authors introduced a relay after the subtractor and the variations of the output voltage error signal $e[n]$ are utilized for compensator auto-tuning only. The main problem of this approach is the relay placement that limits possibility for system identification and causes voltage regulation problems. To obtain valuable information about the LCO amplitude at the relay input significant variations of $e[n]$ need to be produced. As a result the output voltage regulation can be impaired. In that solution, a minimization of the output voltage oscillations could be achieved with an ADC having very small quantization steps. However, this would require an expensive high-resolution ADC, which in targeted cost-sensitive application is not a preferable solution. Hence, the authors limited the application of the method to start-up phase only.

In the system we present here no additional relay is needed. To improve voltage regulation and allow dynamic adjustments during converter regular operation, the DPWM as a natural quantizer is used. As shown in Fig. 4, during the auto-tuning, the resolution of the *DPWM is reduced while it is still fed with a high resolution control variable*, so that multiple values of $d_c[n]$ correspond to a single duty ratio value $d$. In addition, the PID compensator used for regular converter operation is replaced with an integral compensator, $K/s$. This integrator has a dual role. It amplifies small LCO of the output voltage resulting in much larger variations of control variable $d_c[n]$, which can be easily measured without significantly affecting voltage regulation. The other role of the compensator is simplification of the system identification procedure.

The amplitude and frequency of produced oscillations, $A_{\rm LC}$ and $f_{\rm LC} = 1/T_{\rm LC}$, respectively, can be found form the following condition for their existence [22]–[24]

$$-1 = 1\angle 180^\circ = N_{\rm DPWM}(A_{\rm LC},\varepsilon)G_{\rm vd}(j\omega_{\rm LC}) \times K_{\rm ADC}(j\omega_{\rm LC})\frac{K}{j\omega_{\rm LC}} \quad (1)$$

where $N_{\rm DPWM}(A,\varepsilon)$ describes the gain of the DPWM, $G_{\rm vd}(j\omega)$ is control-to-output transfer function of the switching converter, and $K_{\rm ADC}(j\omega)$ input-to-output transfer function of the analog-to-digital converter. In this case, to obtain the gain of DPWM we use describing functions [23], [24]. Also, to simplify the analysis we assume that the frequency of LCO is much smaller than the switching frequency and that, at $f_{\rm LC}$, the delays of ADC and DPWM have negligible effects.

In [22] it was shown that the nonlinear gain of DPWM depends not only on the input signal amplitude, but also on the signal's offset, $\varepsilon$. Hence, direct parameter extraction cannot be performed unless the offset is taken into account or its influence eliminated.

To eliminate the offset, we introduce a *zero-offset calibration* block, shown in Fig. 4. Before the resolution of the DPWM is reduced, the block calculates the offset of $d_c[n]$ and accordingly changes the digital voltage reference $V_{\rm ref}[n]$ to result in zero dc bias. For example, if the resolution of the DPWM is to be reduced from 10 to 7 b and if the three least significant bits (3 LSBs) of the 10-b $d_c[n]$ value are 001, the offset calibration block changes the reference to have the 3 LSBs of $d_c[n]$ equal 100. It is performed by adding 011 to $V_{\rm ref}[n]$ (see Fig. 2). This value is the midpoint between two successive 7-b values and has zero offset. As a result a symmetric LCO can be easily created and analyzed using describing functions (DF) with zero dc bias [23]. That analysis shows that the gain of the DPWM is

$$N_{\rm DPWM}(A) = \frac{4D_q}{\pi A_{\rm LC}} \quad (2)$$

where $D_q$ is a quantization step of DPWM when operating with crude resolution (see Fig. 4). It should be noted that offset calibration block always insures the existence of limit-cycle oscillations during auto-tuning. For some operating points, even a very low-resolution DPWM can result in operation without LCO. It happens when one of the coarse quantization steps causes the output voltage to fit inside the zero-error bin. By introducing zero offset this situation is eliminated and the average value of $d[n]$ always lies between two discrete values. It is also worthy to mention that this change of reference does not have a significant effect on the output voltage regulation. For the example discussed above, the temporary output voltage change of less than 2% can be expected.

The flowchart of Fig. 5 summarizes the complete SI and auto-tuning process. After the SI is initiated the controller checks system stability. If an instability is detected the controller moves to regain stability mode. In that mode, the output voltage is regulated with a conventional PID compensator that would be used for a system without auto-tuning. After the steady state is regained the auto-tuning system performs parameter extraction and controller adjustments in accordance with the earlier described procedure.

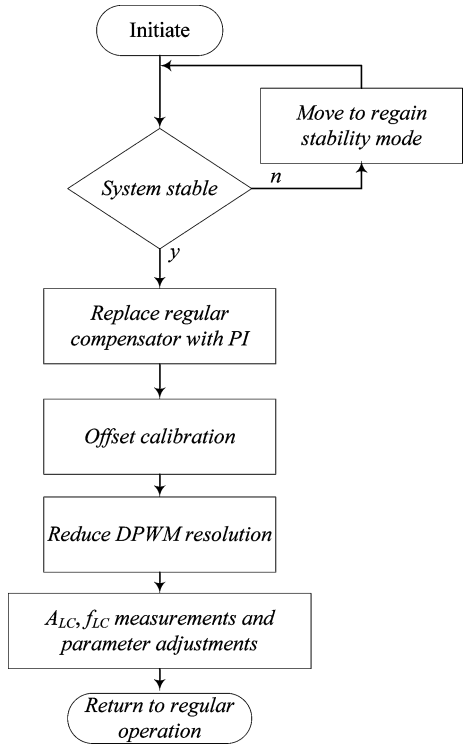



Fig. 5. Flowchart of the limit-cycle initiation and system identification process.

### B. Measurements of LCO Features

In this subsection we give a more detailed description of the blocks for LCO amplitude and frequency measurements.

*1) Peak-to-Peak Amplitude Measurements:* To improve accuracy by minimizing quantization effects, peak-to-peak amplitude of the LCO, $A_{\rm PP}$ is measured. The evaluation is performed through a simple detection of sign change in the difference of the control signal $d_c[n]$

$$\Delta d_c[n] = d_c[n] - d_c[n-1]. \quad (3)$$

This signal is sampled at the switching rate, which is much higher than the LCO frequency. The value $d_c[n-1]$ immediately preceding the sign change from positive to negative is considered to be the maximum amplitude of LCOs, $A_{\rm max}$, while the $d_c[n-1]$ preceding the opposite sign change is equal to the minimum, $A_{\rm min}$. Peak-to-peak amplitude $A_{\rm pp}$ in one LCO period is calculated by taking the difference between $A_{\rm max}$ and $A_{\rm min}$ values.

### C. LCO Frequency/Period Estimator

Fig. 6 shows a block diagram of the frequency extractor, which is a part of the *LCO measurement* block depicted in Fig. 2. The measurements is based on the detection of two zero crossing of the control signal ac value $d_{c\_ac}[n]$. A change of $d_{c\_ac}[n]$ to a positive value is detected and used to start the counter, and the following change of $d_{c\_ac}[n]$ to negative number stops it. The counter is clocked at switching frequency, which is much higher than the corner frequency of the output filter, i.e., the frequency of LCO, (typically at least 30 times higher) allowing accurate calculation of a value proportional to a half of the LCO frequency.

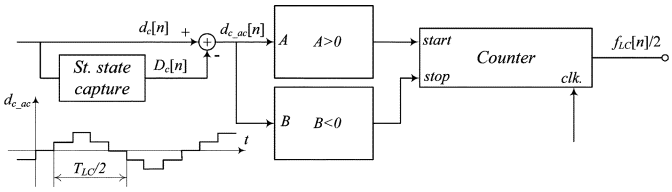



Fig. 6. Frequency extractor block diagram.

### D. Relations Between LCO Features and Power Stage Parameters

The exact relations between LCO features and power stage parameters can be found using advanced control theory tools developed for large-scale relay feedback systems [10], [11]. Still, as mentioned before, these methods give little insight in the relations between LCO features and system parameters. In here, we show that a simpler and more intuitive analysis gives fairly accurate results. It combines describing functions analytical tool with the available information about steady-state duty ratio and output voltage reference values. Also, to demonstrate the universality of this method we show the analysis procedure for buck and boost converters.

*1) Buck Converter Example:* This analysis starts form an averaged small signal model of a buck converter described with its second order control-to-output transfer function [25]

$$G_{\rm vd}(s)=\frac{v(s)}{d(s)}=G_{d0}\frac{1}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}} \tag{4}$$

where $\omega_0=(1)/(\sqrt{LC}), Q=R\sqrt{(C/L)}$, and $G_{d0}=V_g=(V)/(D)$. The output capacitance, inductance and load resistance are denoted by $C, L$, and $R$ respectively. In this case, it is assumed that the output voltage $V$ is known, and that the steady state value of duty ratio $D$ is extracted from dc value of control variable, as shown in Fig. 2.

When a buck converter is connected as shown in Fig. 4 limit cycle oscillations occur. Ideally, the frequency of the LCO corresponds to the output filter corner frequency $\omega_0$ at which the phase shift of the loop gain is 180°. In practice, this frequency is a little bit lower, due to additional phase shifts introduced by the delays of ADC and DPWM [16].

In the estimation of $R$ and $Q$-factor we assume that the value of inductance $L$ is known with a certain level of accuracy, and relatively stable, compared to those of the output load and capacitance. To further simplify analysis without loosing generality, we assume unity gain of the analog-to-digital converter and PI compensator.

The solution of (1)–(4), gives the following result for the peak-to-peak amplitude of LCO:

$$A_{\rm pp}=\frac{4}{\pi}D_qG_{d0}\frac{R}{\omega_0 L}. \tag{5}$$

By combining (4) and (5) we obtain expressions for the output resistance and $Q$-factor:

$$R=\frac{A_{\rm pp}\omega_0\pi L}{4D_qG_{d0}} \tag{6}$$

$$Q=R\frac{\omega_0}{L}=\frac{A_{\rm pp}\pi}{4D_qG_{d0}}. \tag{7}$$

These equations show that by knowing the steady state duty ratio value and analyzing LCO all parameters needed for a compensator design and load estimation can be obtained during a single SI and auto-tuning phase.

It should be noted that at very light loads a high value of $Q$ factor could result in excessive limit cycle oscillations affecting voltage regulation. However, in the targeted application this is not of a big concern. In such conditions most of the modern low-power SMPS are likely to be regulated using pulse-frequency modulation (PFM) [26], [27]. In those systems the light load operation (for example, stand-by mode of an electronic load) is usually indicated with an external signal produced by the load or can be sensed using current estimator presented in [28]. Alternatively, the excessive oscillations in $d_c[n]$ can be detected with a simple limiter and consequently the resolution of DPWM increased, i.e., $D_q$ reduced, to minimize output voltage variations.

*2) Boost Converter Example:* The proposed parameter estimation approach can be applied to other converter topologies as well, including boost, whose control-to-output transfer function is

$$G_{\rm vd}(s)=G_{d0}\frac{1-\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}} \tag{8}$$

where $\omega_0=D'/\sqrt{\rm LC}, Q=D'R\sqrt{C/L}$, and $\omega_z=\omega_0 Q$.

According to (1), in this case, the LCO frequency will not be the same as the converter corner frequency but at the point where the boost converter introduces $-90^\circ$ phase shift. Thus, the relation describing LCO condition becomes

$$\begin{aligned}G_{\rm vd}(j\omega)&=\frac{\pi A_{\rm pp}}{4D_q}\angle -90^\circ\\&=G_{d0}\frac{1-j\frac{\omega_{\rm LC}}{\omega_z}}{\left(1-\left(\frac{\omega_{\rm LC}}{\omega_0}\right)^2\right)+\frac{j\omega_{\rm LC}}{Q\omega_0}}.\end{aligned} \tag{9}$$

By solving (9), again assuming that $D, V$, and $L$ are known, we can obtain all main parameters of the transfer function (8). Besides solving for $\omega_0, Q$, and $\omega_z$, from (9) we can also extract $R$ and $C$. These relations are given as follows:

$$R=\frac{\omega_{\rm LC}LB}{D'^2} \tag{10}$$

$$C=\frac{D'^2(B^2-1)}{L\omega_{\rm LC}^2B^2} \tag{11}$$

where $\omega_{\rm LC}$ is the radial frequency of LCO, and $B=(A_{\rm pp}\pi)/(4D_qG_{d0})$ a new constant introduced for simplicity.

### E. Influence of Inductor Series Resistance

In the proposed auto-tuning method a nonnegligible inductor resistance $R_L$ can cause significant quantitative changes in the frequency and amplitude of LCO. The following analysis, including more accurate buck converter model, shows this effect. Now, the coefficients of (4) change and the converter resonant frequency and $Q$ factor become

$$\omega_0^2=\frac{R_L+R}{RCL} \tag{12}$$

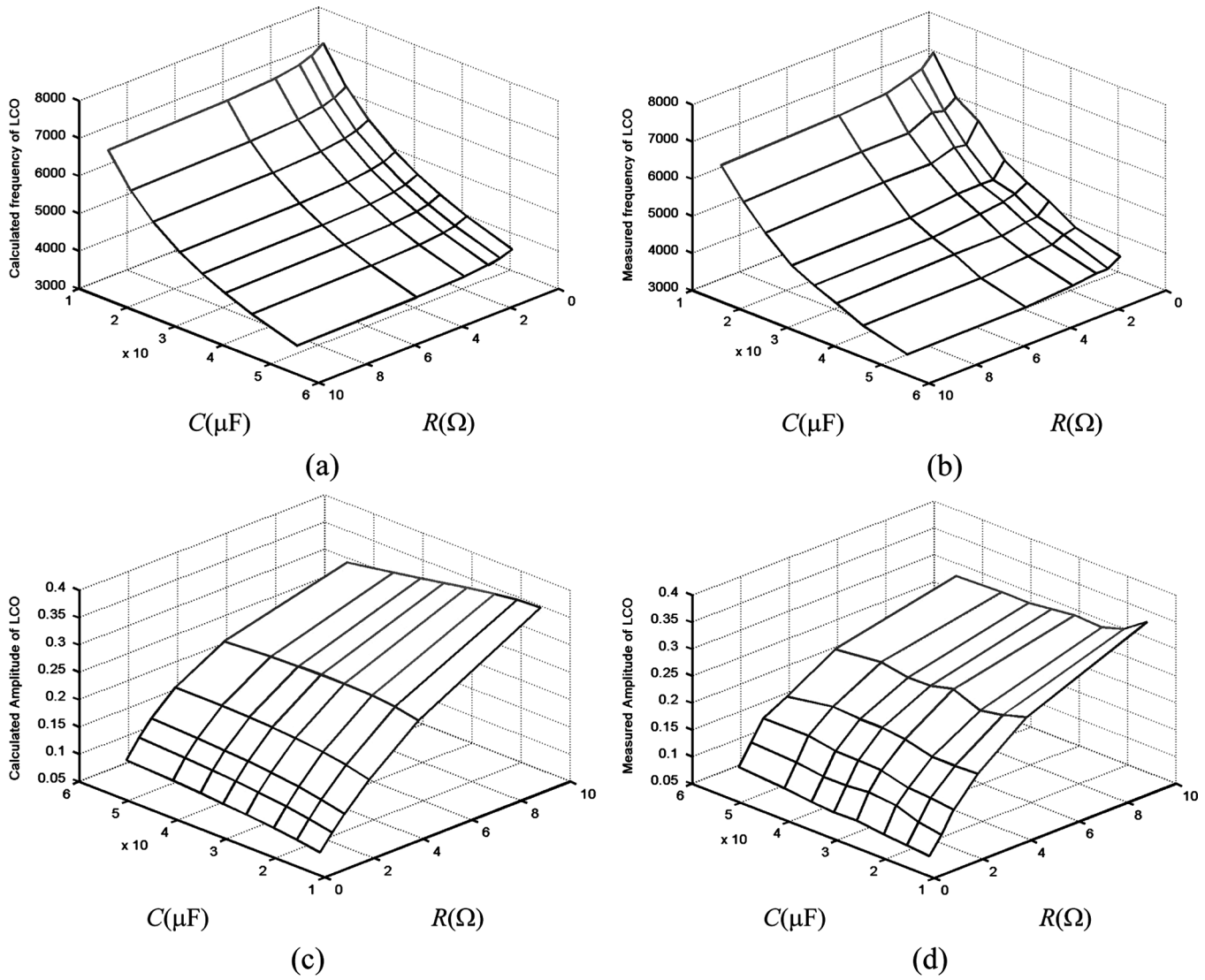



Fig. 7. Relations between LCO features on the power stage output load and capacitance values. Power stage parameters are $L = 33\,\mu$H, $R_L = 0.1\,\Omega$, $Vg = 8$ V, and $V\mathrm{out} = 3.3$ V: (a) calculated frequency of LCO; (b) measured frequency of LCO; (c) calculated amplitude of LCO; and (d) measured amplitude of LCO.

$$Q = \frac{\sqrt{(R_L + R)RCL}}{CRR_L + L}. \tag{13}$$

For this case, the relations between the amplitude and frequency of LCO and power stage parameters (1) are given with the following equations and illustrated in Fig. 7

$$\omega_{\mathrm{LC}}^2 = \frac{R_L + R}{RCL} \tag{14}$$

$$A_{\mathrm{pp}} = \frac{4}{\pi} D_q G_{\mathrm{do}} \frac{R}{CRR_L + L} \frac{1}{\omega_{\mathrm{LC}}} \tag{15}$$

$$C = \frac{R_L + LB\omega_{\mathrm{LC}}}{B\omega_{\mathrm{LC}}(R_L^2 + \omega_{\mathrm{LC}}^2 L^2)} \tag{16}$$

$$R = \frac{L + \frac{R_L}{L\omega_{\mathrm{LC}}^2}}{\frac{V_g}{B\omega_{\mathrm{LC}}} - \frac{R_L}{L\omega_{\mathrm{LC}}^2}}. \tag{17}$$

These results show that in a realistic converter both amplitude and frequency of LCO depend not only on the output capacitance but also on the load value. It can be seen that at heavy loads the resonant frequency of the converter, i.e., LCO frequency, can be significantly higher than expected causing stability problems if the compensator adjustment is not performed regularly.

To assess the accuracy of the previously described analysis we use the system of Fig. 2 and compare its results (14)–(17) with experimental measurements for various values of $R$ and $C$. As it can be seen from Figs. 7 and 8, the describing functions give a fairly accurate estimation of the system parameters.

## IV. Programmable Digital Compensator and Load Estimator

The previous analysis shows that most of power stage parameters can be extracted by analyzing limit cycle oscillations and utilizing readily available information from $d_c\,[n]$. Consequently, we use the extracted data for a digital compensator design, following the procedure presented in [29]. The procedure gives relations between the parameters of a buck converter

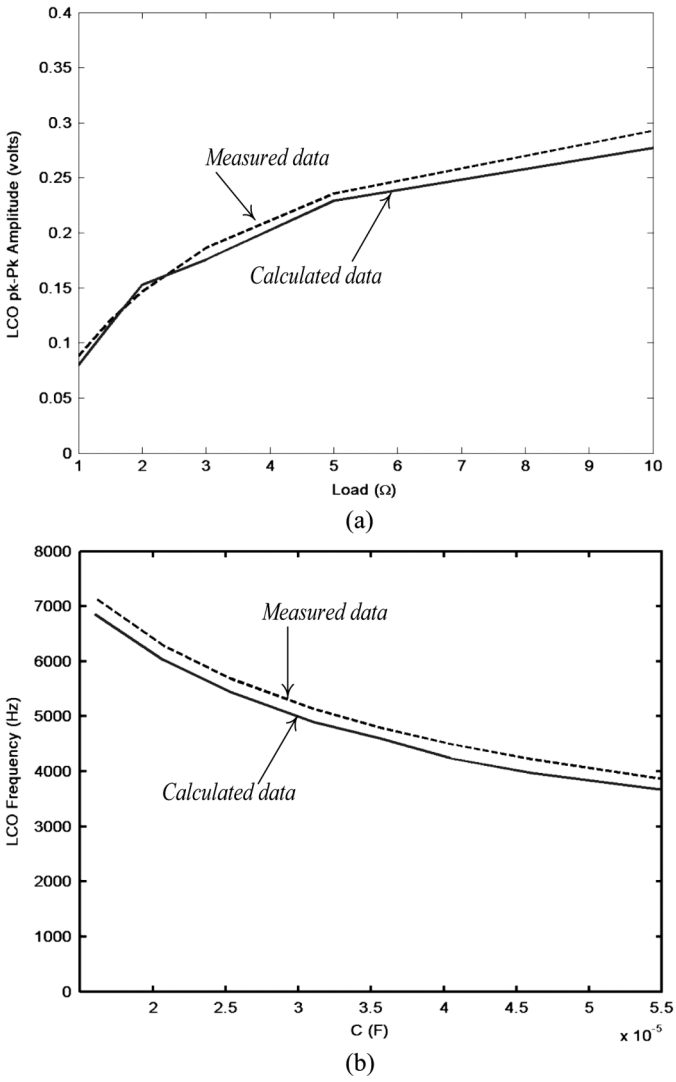



Fig. 8. Comparison of the experimentally obtained data for LCO features with analytical results: (a) dependence of $A_{LC}$ on the output load value and (b) dependence of LCO frequency on the output capacitance value.

and PID compensator coefficients. The PID compensator implements the following discrete-time control law:

$$d_c[n] = d_c[n-1] + K_d\left(e[n] - 2r\cos\left(2\frac{\pi f_z}{f_s}\right)e[n-1] + r^2 e[n-2]\right) \quad (18)$$

where $f_s$ is the system sampling frequency and $f_z$ the center frequency of a pair of compensator zeros, which are set to be the same as $f_{\rm LC}$, i.e., slightly lower than the power stage corner frequency. The parameter $r$ is defined as

$$r = e^{\left(-\frac{\pi f_z}{Q f_s}\right)} \quad (19)$$

and the gain $K_d$ is kept constant and selected based on control bandwidth requirement.

To create an auto tuner we could build a dedicated digital hardware that calculates PID coefficients from (12), (13), and (19). A problem is that, from the practical realization point of view, such solution would be quite complex. Instead, as shown in Fig. 9, we use a set of look-up tables (LUTs) for the transformation of LCO features into PID coefficients. The tables containing pre-stored values of controller coefficients are addressed by the measured LCO features $(A_{\rm pp}, f_{\rm LC})$ as well as by the steady state value $D_c\,[n]$. This architecture involves a trade off between the size of LUT and the number of possible discrete control laws. However, for most of the applications, construction of a large LUT covering all possible inputs is not necessary. We have found, through extensive simulations and experimental verifications, that the knowledge of $A_{PP}$, $f_{\rm LC}$ and $D_c$ in a relatively small number of operating points gives sufficient information for the design of a compensator covering a wide operating range. For example, for the range shown in Figs. 7 and 8, we use thirty discrete-time control laws to obtain fairly good dynamic characteristics and build a compensator which can be used to prove the presented concepts. The *address generator* selects an appropriate control law, based on $A_{pp}$, $f_{\rm LC}$ and $D_c$ values and their pre-calculated relations with the compensator coefficients. Since, in most of the cases, exact matching between the LCO parameters and addresses stored in look up tables cannot be achieved, the generator selects the control law that corresponds the closest smaller value of the measured LCO frequency. In practice, it means that the frequency of the PID's complex zeroes, designed as described in [29], is always placed bellow the corner frequency of the power stage ensuring system stability. The rounding down is performed in very simple manner, by observing only 4 most significant bits of $f_{\rm LC}\,[n]$. This results in fifteen possible values of PID zeroes (0 frequency is excluded). Two possible compensators, with different damping

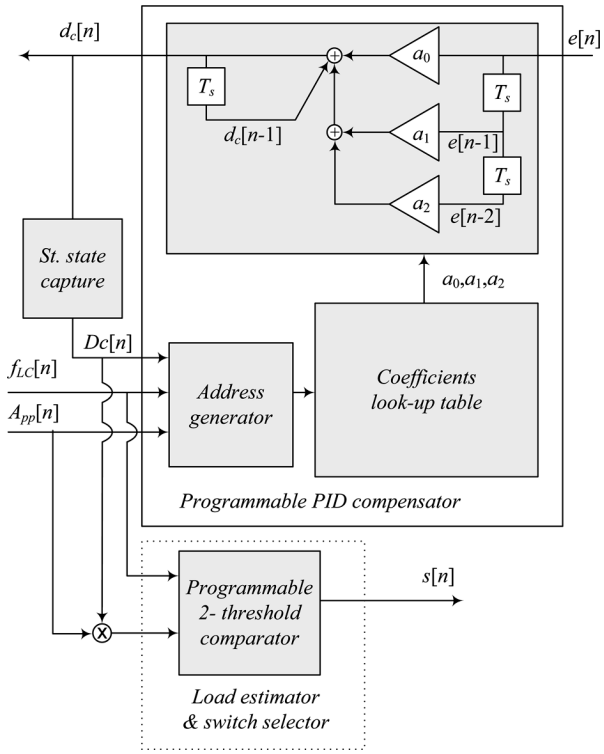



Fig. 9. Block diagram of programmable PID compensator and load estimator.

factors, are assigned to each of these frequencies. The selection of the damping factor is performed from $D$ and $A_{\rm PP}$.

This structure having thirty possible control laws obviously cannot cover all possible converter configurations and all possible output filter values. To make a truly universal controller, a massive memory, having a very large number of control laws could be potentially used. Taking into account recent advances in the reduction of size, power consumption, and cost of large-capacity storage elements, this becomes a conceivable solution. Alternatively, a self-tuning system not requiring look-up tables presented in [30] can be implemented.

### A. Load Estimator

Fig. 9 also shows *load estimator and switch selector* block used for efficiency optimization and current protection. It combines the current extraction method presented in this paper, with the switch selection logic introduced in [31]. Based on $f_{\rm LC}$ and the product $D_C\ A_{\rm PP}$ an appropriate 2-b switching sequence $s\ [n]$ is selected with a compensator having two programmable thresholds. The thresholds of the comparator depend on the amplitude of LCO and presorted current limit values. As it can be seen from (6) and Fig. 7, the largest product corresponds to the lowest current and only the small transistors $Q_{1\_L}$ and $\rm Q_{2_L}$ are enabled (see Fig. 2). Larger output currents result in lower comparator inputs and the activation of parallel switches. When the product drops below the lowest threshold, current protection is activated and all of the transistors are turned off.

To eliminate possible current stress, solution presented in [31] is applied. During each light to heavy load transition all four transistors are enabled. Only after the current estimation is completed, an appropriate driving sequence $s\ [n]$ is set.

### B. System Limitations

The losses of the switches and the resistances of the output filter components as well as nonoverlapping conduction times alter the transfer function of a converter, and consequently change the amplitude and frequency of the LCO. As a result, in some situations, the performance of the auto-tuning systems can be affected. The operation of the system is also influenced in situations when the output load is not a pure resistor. In this subsection we address these problems, focus on the most dominant ones, and suggest solutions for them. The problems are divided into two groups, first influencing compensator design and the second group having negative effect on current estimation. It should be noted that, in most of the cases these problems are not related since the compensator design predominantly relies on the knowledge of actual resonant frequency, which usually coincides with the frequency of LCO.

*1) Compensator Design Considerations:* A nonnegligible equivalent series resistance $R_{\rm esr}$ of the output capacitor $C$ introduces a zero in converter transfer function at the frequency $f_{\rm esr} = 1/(2\pi\ CResr)$. Here we show that this zero can affect the system in two ways causing noise problems or reducing the bandwidth of the loop and causing erroneous load estimation.

The first situation is depicted with the Bode plots of Fig. 10 showing continuous time representation of the discrete-time compensator (18), labeled as $G_c$ (s), control-to-output transfer

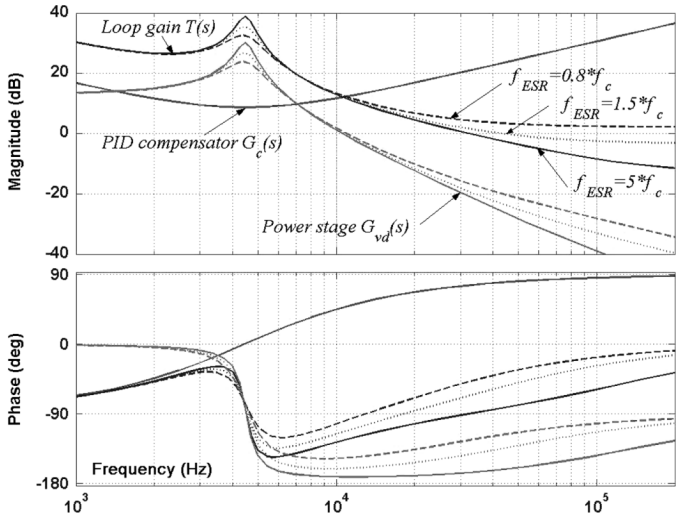



Fig. 10. Magnitude and phase characteristics of the uncompensated and compensated buck converter for the cases when the frequency of a zero introduced by $R_{esr}$ is around the desired crossover frequency of the system.

function of a buck converter for three different values of $f_{\rm esr}$, and corresponding loop gains $T\ (s)$.

The cases when the frequency of the zero is little bit higher then the desired crossover frequency of the system $f_c$, i.e., $f_{\rm esr} \approx 1.5\ f_c$ and $f_{\rm esr} \approx 5\ f_c$ as well as when it is below $f_c$, i.e., $_{\rm esr}\ \approx 0.8\ f_c$, but still significantly higher than the converter's corner frequency $f_0 = 1/2\pi\sqrt{\rm LC}$ are demonstrated.

In practice, this situation can happen when a tantalum or an aluminum capacitors with a high $R_{\rm esr}$ is used. Then, the PID (18), designed to have a pair of complex zeroes at a frequency little bit lower than $f_0$ [29] has a low attenuation of high frequency components, and in some cases, seemingly, results in nonzero-crossing. For example for $f_{\rm esr} \approx 0.8\ f_c$ from Fig. 10. In practice the nonzero-crossing is not likely to exist. An anti-aliasing filter at the ADC's input or the natural low-pass filtering effect of a delay-line or ring oscillator based ADC [2], [5] acts as a high frequency pole forcing the loop gain to drop. As it can be seen in Fig. 11, showing time-domain simulations of the system of Fig. 2, in those situations, the system stability and dynamic response are not compromised, although noise related problems can occur. The low attenuation of the high frequency components causes a poor noise rejection which can be seen at the converter output.

To minimize the noise problem, if needed, a pole at a constant frequency, higher than the desired system bandwidth, can be introduced.

A more serious, but in modern converters, having low- $R_{\rm esr}$ capacitors, not common situation is when $f_{\rm esr}$ is close to $f_0$. As shown in Fig. 12 this zero increases the frequency point where the phase shift of the open loop system is 90° and, according to (1), causes the LCO and the placement of compensator's complex zeroes beyond $f_0$. From the Bode plots it can be seen that this mismatch results in a lower crossover frequency, i.e., slower dynamic response, than expected and a wrong estimation of the output resistance, but does not cause system instability. To avoid these problems, an additional delay component, causing a phase shift proportional to the negative value of that introduced

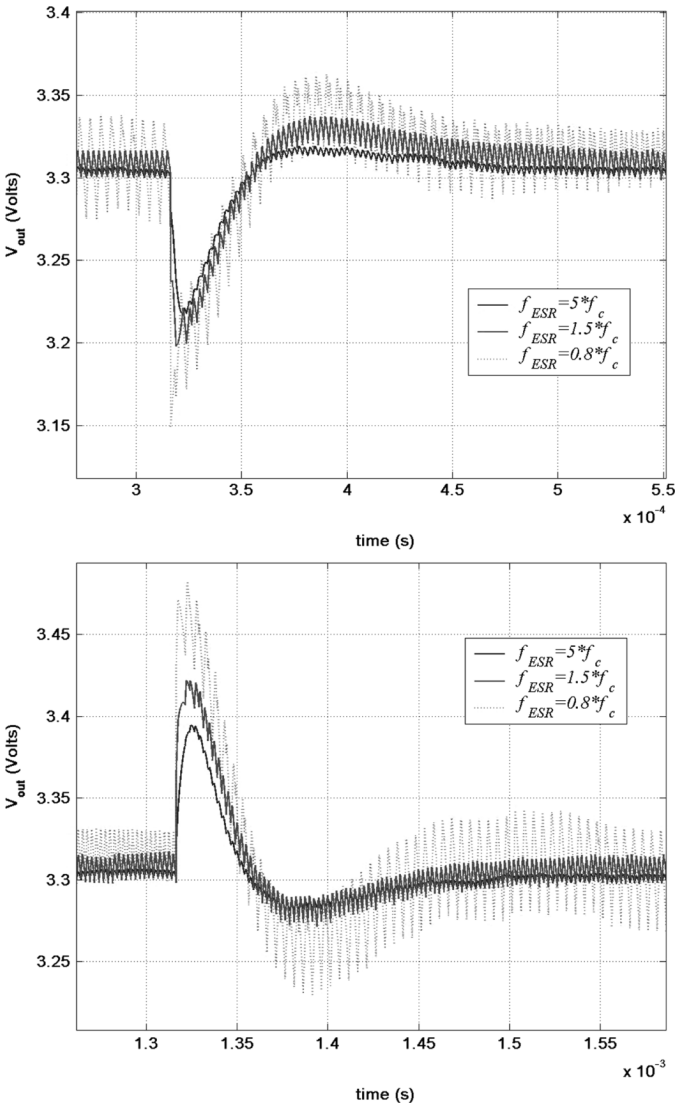



Fig. 11. Time-domain simulations of the closed-loop operation of the system of Fig. 2 when $R_{esr}$ is not negligible; Top: the output voltage $v_{\rm out}(t)$ during a light to heavy load transient (0.65 A to 1.3 A); Bottom: vout(t) during a heavy to light load transient (1.3 A to 0.65 A).

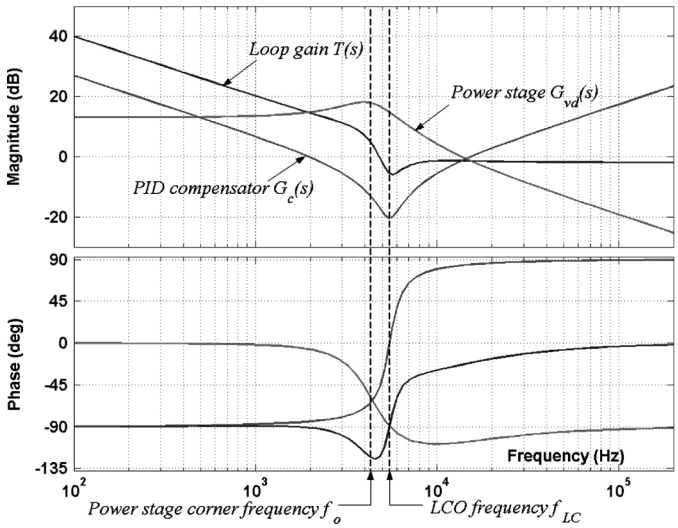



Fig. 12. Magnitude and phase characteristics of the uncompensated and compensated buck converter for the cases when the frequency of a zero introduced by equivalent series resistance is close to the corner frequency of the power stage.

by $f_{\rm esr}$-zero can applied during the system identification phase. The delay will cause the LCO at the resonant frequency and more accurate estimation of the damping factor.

*2) Load Estimation:* The presented load estimation method relying on the derivation of the output load from the *Q*-factor has limited accuracy and is more suitable for coarse current estimation and segmented switching than for the applications where an accurate knowledge about the output current is required. The examples where the coarse knowledge of the current estimation is sufficient, include consumer electronics and communication devices. In those applications several clearly distinguishable task-dependent load conditions can be easily recognized.

The accuracy of the current estimation is affected by several factors, which we have grouped in three categories.

First, is that the inductance value, which is used for calculation of the load, has a tolerance that limits the accuracy of current measurement.

The second factor is related to the variation of the damping factor $Q$. It is largely influenced by parasitic components and nonlinearities in the circuit. Namely, as described earlier, the series resistances of the inductor and the capacitor's $R_{\rm esr}$, can change $f_c$ or cause the LCO to occur at a different frequency. In addition, in converters with synchronous rectification nonoverlapping dead time [32] can also alter the value of the damping factor. In digital controllers the value of the dead-time is often known and can be accurately controlled [32], [33]. Hence, it can be taken into account, to modify the converter model, and a consequent on-line compensation can be performed.

From the system operation point of view, the most critical situation is when the output load is a digital signal processor or a downstream converter, which dynamic do not behave as a resistor but as a current and a power sinks, respectively. In those cases, the amplitude of the LCO is not proportional to the load, but is still limited due to the fact that the filter inductor and switching transistors introduce losses.

The losses can be modeled as resistors [25] and lumped in a single equivalent value $R_{\rm total}$. Now, the amplitude can be derived from (15), by replacing $R_L$ with $R_{\rm total}$ and letting $R \rightarrow \infty$

$$A_{\rm pp} = \frac{4}{\pi} D_q G_{\rm do} \frac{1}{CR_{\rm total}} \sqrt{\rm LC} = \frac{4}{\pi} D_q G_{\rm do} \frac{1}{R_{\rm total}} \sqrt{\frac{L}{C}}. \quad (20)$$

If the amplitude is too high, as suggested in Section III-C2, a protective limiter can be introduced. It should be noted that, even though the load estimation cannot be directly performed, the LCO still occurs at the resonant frequency allowing proper compensator operation and fast dynamic response. This is demonstrated with the simulation results of Fig. 13, showing the system identification phase and transient response of the converter when the load is a current sink.

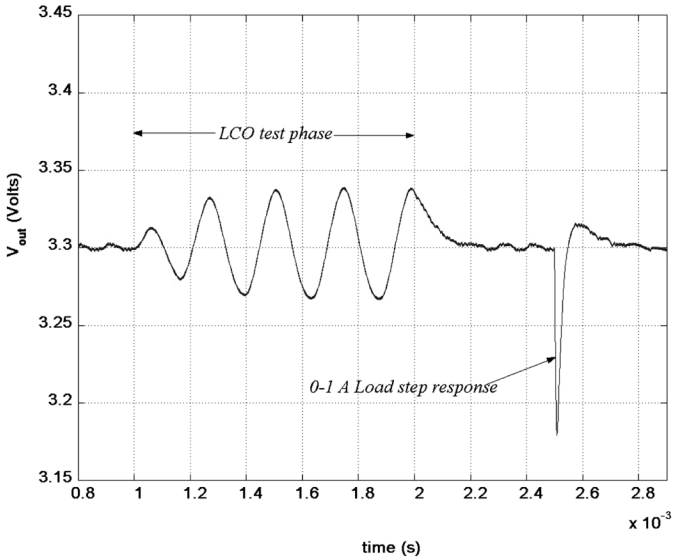



Fig. 13. Time-domain simulations of the system of Fig. 2 for the case when the load is a current sink whose value changes fro 0 A to 1 A.

To find the output for this cases, some other load estimation method can be used. For example, as described in [28], [31] a simple low-bandwidth ADC at the input of the power stage can be placed and the load can be estimated by monitoring the deviation of the steady-state value of $d\,[n]$.

## V. Experimental Results

Based on diagrams shown in Figs. 1, 2, and 9 an experimental prototype was built. The power stage of the system is a 400 kHz synchronous buck with segmented switches. The smaller transistors ($Q_{1_L}$ and $Q_{2_L}$ from Fig. 2) are IRF-IRML2402, rated for 1.2 A and the larger ones are IRF- IRMLS1902 with 3.2 A current rating. The input voltage $V_g$ is 5–9 V and the output is regulated at $V_{\rm out} = 3.3$ V. All functional blocks of the auto-tuning controller, except the DPWM, are realized with an Analog Devices, ADMC-401 DSP board. An Altera 10 K FPGA system is used for the implementation of high-frequency programmable-resolution DPWM. In steady state the DPWM's resolution is 10 b, while during the identification it is decreased to 7 b. The quantization step of the ADC around reference is set to be 20 mV. Precalculated PID coefficients are placed in three 30-word 10-b look-up tables. It should be noted that the controller utilizes only few DSP functions and can be implemented with much simpler hardware, i.e., FPGA or a small application specific IC. Figs. 14–18 show results obtained with the experimental prototype.

### A. Auto-Tuning Examples

Fig. 14 demonstrates disturbance caused by a sudden change of the output capacitance and consequent auto-tuning process. After the disturbance is detected the auto-tuning is performed in accordance with the algorithm shown in Fig. 5. During *regain stability* phase PID compensator that would be used for a conventional controller frequently changes $d_c\,[n]$ control value to establish a steady state. To provide stable system operation for all operating conditions, this PID compensator is constructed in accordance with the worst-case design procedure described in [29]. As depicted in Figs. 7 and 8 variations of $C$ and $R$ from 10 $\mu$F to 55 $\mu$F and from 1 $\Omega$ to 10 $\Omega$, respectively are considered. The worst case conditions is assumed to be $R = 10\Omega$ and $C = 55\mu$H.

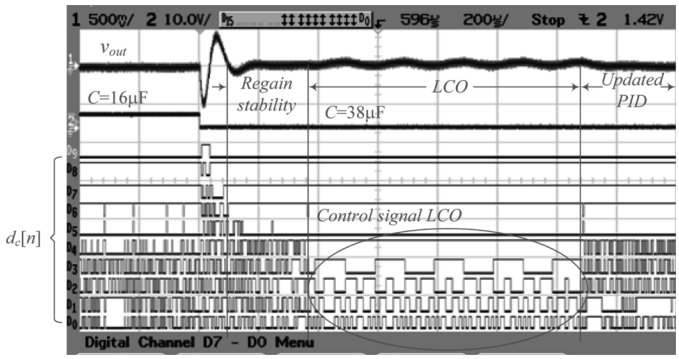



Fig. 14. Auto-tuning process after a sudden output capacitance change $V_g = 8$ V, $R = 5\ \Omega$, $L = 33\ \mu$H, $f_{sw} = 400$ kHz. The limit cycle oscillations of four least significant bits of $dc[n]$ (digital channels $\mathrm{D}_0 - \mathrm{D}_3$) are used for parameter estimation.

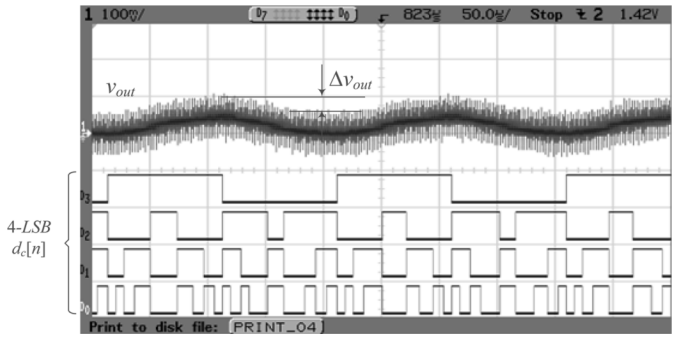



Fig. 15. Zoomed-in view of the output voltage waveform and the four least significant bits of the control signal dc[n] during LCO phase.

In the following phase LCO are introduced and a slower integral compensator regulates the output voltage. Since the bandwidth of the integrator is low, it eliminates high-frequency variations of $d_c$ [n] allowing accurate measurement of LCO. During the last phase PID compensator coefficients are updated and a new auto-tuned compensator is utilized.

A zoomed-in view of the previous waveforms during LCO phase is shown in Fig. 15. These waveforms verify that the new auto-tuning system has a small influence on the output voltage regulation. It can be seen that even though the converter operates with a relatively light load (5 $\Omega$) and high input voltage only small output voltage variations of less than 40 mV at the output exist. Still, these variations cause significant changes in four least significant bits of $d_c\,[n]$ that can be easily detected and used for parameters extraction. For even lighter loads the resolution of the DPWM can be increased to 8 b. As a result, similar values of LCO amplitude can be obtained for the twice of the output resistance value (6).

The waveforms of Figs. 16 and 17 show a comparison of load transient responses of the auto-tuned compensator and the one used during the regain stability phase, i.e., a conventional PID compensator that would be used if we had a system without auto-tuning.

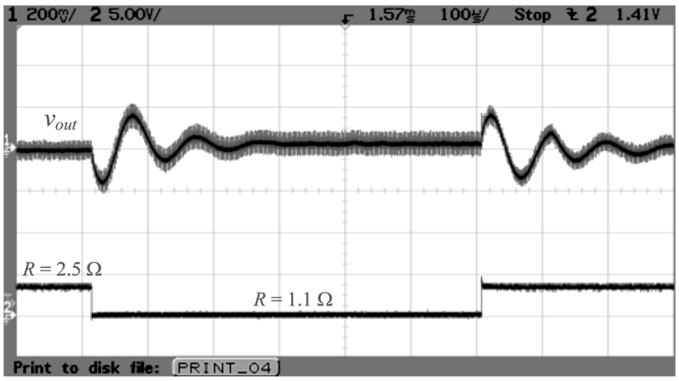



Fig. 16. Experimental load transient response of conventional controller for the output load changes between 1.3 A and 3 A; $V_g = 8$ V, $C = 38$ mF, L = 33 mH, $f_{sw} = 400$ kHz.

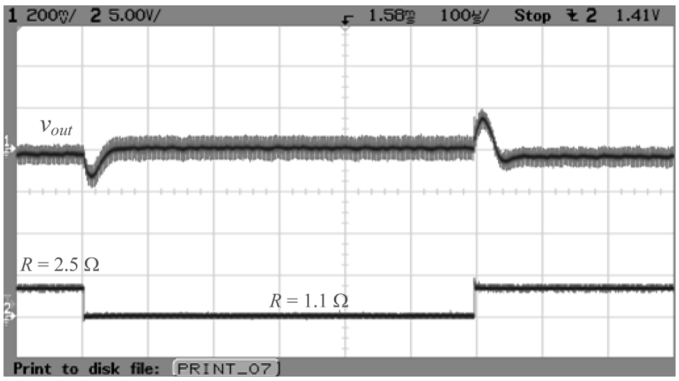



Fig. 17. Experimental load transient response of the auto-tuned controller for the output load changes between 1.3 A and 3 A; $V_g = 8$ V, $C = 38$ mF, $L = 33$ mH, $f_{sw} = 400$ kHz.

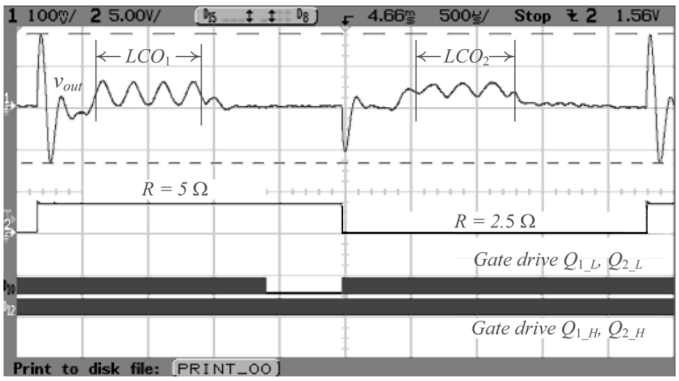



Fig. 18. Experimental load transient response for the output load changes between: $V_g = 8$ V, $C = 38$ mF, $L = 33$ mH, $f_{\rm sw} = 400$ kHz; top: conventional PID compensator; bottom: auto-tuned controller.

It can be seen that the auto-tuning improves dynamic characteristics of the controller resulting in significantly faster response with much smaller output voltage drops and overshoots.

Fig. 18 shows operation of the load estimator and the process of efficiency optimization through a selection of switching sequence. As described in Section V (b), at light loads only transistors $Q1_L$ and $Q2_L$ are active while at heavier loads all four transistors are enabled. It can be seen that during the transients all four transistors operate simultaneously. Changes of switching sequence are performed after the load estimation phases (labeled as $\mathrm{LCO}_1$ and $\mathrm{LCO}_2$) are completed. This diagram also shows the effect of offset calibration circuit, described in Section III-A. It slightly changes the reference to cause symmetric LCO. The efficiency of this system is compared to the one having larger transistors ($Q1_H$ and $Q2_H$) only. An improvement at light and medium loads of up to 7% was achieved. If a more sophisticated segmented power stage is used, similar to the one demonstrated in [31], even better improvement can be expected.

## VI. Conclusion

A digital auto-tuning control system for low-power switch-mode power supplies (SMPS) is introduced. The system utilizes a novel method of extracting parameters from the amplitude and frequency of limit-cycle oscillations LCO in duty ratio control value to minimize the influence of the auto-tuner on the output voltage. This provides good voltage regulation during auto-tuning and, consequently, on-line system calibration. Furthermore, the dc value of the control variable and reference are used to obtain additional information about the state of the system. Based on collected data the controller performs compensator adjustments and output load estimation. The estimate of the output load is used for efficiency improvement in power stage containing segmented transistors. The system operation is experimentally verified with very simple hardware elements that can be realized in practically any implementation technology. The experimental results show significant improvements in dynamic response and converter efficiency. They also confirm the validity of the proposed auto-tuning approach and are in a good agreement with the supporting mathematical analysis.

## References

[1] A. V. Petrchev, J. Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, pp. 356–364, Jan. 2003.

[2] B. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC for dc–dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[3] E. O'Malley and K. Rinne, "A programmable digital pulsewidth modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 mHz," in *Proc. IEEE APEC Conf.*, 2004, pp. 53–59.

[4] A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, "High-efficiency multiple-output dc–dc conversion for low-voltage systems," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 8, pp. 252–263, Jun. 2000.

[5] J. Xiao, A. Peterchev, J. Zhang, and S. R. Sanders, "An ultra low-power digitally-controlled buck converter IC for cellular phone applications," in *Proc. IEEE APEC Conf.*, 2004, pp. 383–391.

[6] A. V. Petrchev and S. R. Sanders, "Digital loss-minimizing multimode synchronous buck converter," in *Proc. IEEE PESC Conf.*, 2004, pp. 20–25.

[7] A. Prodić, R. W. Erickson, and D. Maksimović, "Digital controller chip set for isolated dc–dc power supplies," in *Proc. IEEE APEC Conf.*, 2003, pp. 866–872.

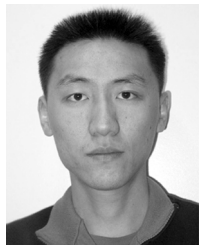
[8] K. Hirayama, Y. Tone, K. Takagi, H. Murakami, M. Shibata, H. Nagamura, and Y. Takagi, "Digital AVR application to power plants," *IEEE Trans. Energy Conv.*, vol. 8, pp. 602–609, Dec. 1993.

[9] K. J. Åström and T. Hagglund, *Automatic Tuning of PID Controllers*. Research Triangle Park, NC: Instrum. Soc. Amer., 1988, ISBN 1-55617-081-5.

[10] I. Kaya and D. P. Atherton, "Exact parameter estimation from. relay autotuning under static load disturbances," in *Proc. IEEE Amer. Control Conf.*, 2001, pp. 3274–3279.

[11] S. Majhi and D. P. Atherton, "Autotuning and controller design for processes with small time delays," *Proc. Inst. Elect. Eng.*, vol. 146, pp. 415–425, Sep. 1999.

[12] T. Kim and E. H. Abed, "Closed-loop monitoring systems for detecting incipient instability," in *Proc. IEEE Decision Control Conf.*, 1998, pp. 3033–3039.
[13] B. Miao, R. Zane, and D. Maksimović, "Practical on-line identification of power converter dynamic response," in *Proc. IEEE APEC Conf.*, 2005, pp. 57–62.
[14] B. Miao, R. Zane, and D. Maksimović, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron.*, vol. 20, pp. 1093–1099, Sep. 2005.
[15] A. Kelly and K. Rinne, "A self-compensating adaptive digital regulator for switching converters based on linear prediction," in *Proc. IEEE APEC*, 2006, pp. 712–718.
[16] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of digitally controlled buck converters based on relay feedback," in *Proc. IEEE PESC Conf.*, 2005, pp. 2140–2145.
[17] R. White, "Emerging on-board power architectures," in *Proc. IEEE APEC Conf. 2003*, Feb. 2003, pp. 799–804.
[18] M. F. Schlecht, "Distributed power architecture system stability requires compensation of dc–dc converter inputs," *PCIM Mag.*, vol. 26, pp. 52–56, Feb. 2000.
[19] D. L. Logue and P. T. Krein, "Preventing instability in dc distribution systems by using power buffering," in *Proc. IEEE PESC Conf.*, 2001, pp. 33–37.
[20] V. J. Thottuvelil and G. C. Verghese, "Analysis and control design of paralleled dc/dc converters with current sharing," *IEEE Trans. Power Electron.*, vol. 13, pp. 635–644, Jul. 1998.
[21] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron*, vol. 18, pp. 301–308, Jan. 2003.
[22] H. Peng, D. Maksimovic, A. Prodic, and E. Alarcon, "Modeling of quantization effects in digitally controlled dc–dc converters," in *Proc. IEEE PESC Conf.*, 2004, pp. 4312–4318.
[23] J. H. Taylor, "Describing Functions," in *Electrical and Electronics Engineering Encyclopedia*. New York: Wiley, 2000, pp. 77–98.
[24] E. Davison and D. Constantinesou, "A describing function technique for multiple nonlinearities in a single-loop feedback system," *IEEE Trans. Autom. Contr.*, vol. AC-16, Feb. 1971.
[25] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2000.
[26] B. Sahu and G. A. Rincon-Mora, "A high-efficiency, dual-mode, dynamic, buck-boost power supply IC for portable applications," in *Proc. IEEE VLSI Conf.*, 2005, pp. 858–861.
[27] J. Xiao, A. V. Peterchev, Z. Jianhui, and S. R. Sanders, "A 4- $\mu$a quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *IEEE J. Solid State Circuits*, vol. 39, pp. 2342–2348, Dec. 2004.
[28] A. Prodić and D. Maksimović, "Digital PWM controller and current estimator for a low-power switching converter," in *Proc. IEEE COMPEL*, 2000, pp. 123–128.
[29] A. Prodić and D. Maksimović, "Design of a digital PID regulator based on look-up tables for control of high-frequency dc–dc converters," in *Proc. IEEE COMPEL*, 2002, pp. 18–22.
[30] Z. Zhao, A. Prodić, and P. Mattavelli, "Self-Programmable PID compensator for digitally controlled SMPS," in *Proc. IEEE COMPEL*, 2006, pp. 112–116.
[31] O. Trescases, W. T. Ng, H. Nishio, M. Edo, and T. Kawashima, "A digitally controlled dc–dc converter module with a segmented output stage for optimized efficiency," in *Proc. IEEE ISPSD Conf.*, 2006, pp. 1–4.
[32] A. V. Peterchev and S. R. Sanders, "Digital multimode buck converter control with loss-minimizing synchronous rectifier adaptation," *IEEE Trans. Power Electron.*, vol. 21, pp. 1588–1599, Nov. 2006.
[33] V. Yousefzadeh and D. Maksimović, "Sensorless optimization of dead times in dc–dc converters with synchronous rectifiers," *IEEE Trans. Power Electron*, vol. 21, pp. 994–1002, Nov. 2006.



**Zhenyu Zhao** (S'02) was born in Tianjin, China, in 1978. He received the B.Eng. degree in electrical engineering from the Shanghai Jiao Tong University, Shanghai, China, in 1999 and the M.E.Sc. degree from the University of Western Ontario, ON, Canada in 2004. He is currently pursuing Ph.D. degree in electrical engineering at the University of Toronto, Toronto, ON, Canada.

Since May 2005, he has been a Research Assistant in the Laboratory of Low-Power Management and Integrated Switch-Mode Power Supplies, University of Toronto. His research interests include modeling and control techniques, power electronics, and mixed-signal VLSI and/or DSP implementation for power management applications.

**Aleksandar Prodić** (S'00–M'03) received the Dipl. Ing. degree in electrical engineering from the University of Novi Sad, Novi Sad, Serbia, in 1994 and the M.Sc. and Ph.D. degrees from the Colorado Power Electronics Center, University of Colorado, Boulder, in 2000 and 2003, respectively.

Since 2003, he has been with the University of Toronto, Toronto, ON, Canada, where he is an Assistant Professor at the Department of Electrical and Computer Engineering. In 2004, at the University of Toronto, he established Laboratory for Low-Power Management and Integrated Switch-Mode Power Supplies. His research interests include digital control of low-power high-frequency SMPS, mixed-signal IC design, DSP techniques for power electronics, and the development of systems-on-chip (SoC) for power management.