Continuous-Time Digital Controller for High-Frequency DC-DC Converters

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***Abstract*—This paper introduces a voltage mode digital controller for low-power high-frequency dc-dc switch-mode power supplies (SMPS) that has fast transient response, approaching physical limitations of a given power stage. In steady state, the controller operates as a conventional pulsewidth modulation regulator and during transients it utilizes a novel fast voltage recovery mechanism, based on real-time processing of the output voltage in digital domain. This continuous-time digital signal processing mechanism is implemented with a very simple processor consisting of a set of asynchronous comparators, delay cells, and combinatorial logic. To eliminate the need for current measurement and calculate the optimal switching sequence of the power stage transistors, the processor performs a capacitor charge balance algorithm, which is based on the detection of the output voltage peak/valley point. The effectiveness of the controller is demonstrated on an experimental 5 W, 5 V to 1.8 V, 400 kHz buck converter. The converter recovers from load transients through a single on-off action of the power switch, virtually reaching the shortest possible time, limited by the values of the power stage filter components only.**

***Index Terms*—Low-power dc-dc converters, digital control, continuous-time digital signal processing, capacitor charge-balance.**

I. Introduction

In modern low-power dc-dc switch-mode power supplies (SMPS), processing power ranging from a fraction of watt to tens of watts, fast response to load transients and tight voltage regulation are among the most important requirements [1]. In cost-sensitive point-of-load (POL) applications and portable systems, improvements in the load transient response usually result in a substantial reduction of the size and weight of the power stage filter components [2]. In distributed power systems (DPS) for personal computers and telecom, the faster control also reduces voltage and current stress on downstream converters providing more reliable operation of the supplied equipment.

Even though numerous fast transient response methods have been developed [3]–[22], in most commercial low-power SMPS, analog voltage mode pulsewidth modulation (PWM) or current-program mode regulators with quite limited bandwidth of the voltage loop [23], [24] are predominantly used. Among the main reasons are operation at a constant switching frequency minimizing noise problems, tight output voltage regulation, and simple cost-effective practical implementation [1].

Fast transient response methods based on various modifications of voltage-mode hysteretic control [4], [5], including those with variable hysteretic band [25] for achieving constant switching frequency, have proven to be a viable alternative in some applications. Still, in the targeted systems their use is often limited. The voltage mode hysteretic control cannot directly be applied for boost converters [25], while in buck topologies it can compromise voltage regulation. This is because the SMPS behaves as a second-order system and a delay between the switching action and actual increase/decrease of the output voltage always exists. As a solution, current-mode hysteretic controllers have been proposed [6]. They can eliminate the previously mentioned problems but their practical realization is challenging. Similar to switching surface [7]–[10] and trajectory path [22], [23] methods, these controllers often require measurement of the output capacitor current and/or a costly high gain-bandwidth current amplifying circuit. Since the complexity of these systems significantly exceeds that of a complete conventional PWM controller [1], they have not been widely adopted in high-frequency low-power SMPS.

In [11] and [22] it has been shown that for a given converter topology the fastest possible, *i.e., optimal-time*, transient response can be obtained through a single on/off action of the power switches, where the on and off times are calculated based on the output capacitor charge balance [5], [7]–[9], [11]–[16]. The presented fast voltage recovery mechanism was verified through simulations and through analog implementation capable of operating for a single predefined load change. No attempt was made to create a practical system capable of operating over a wide operating range. This is probably due to the requirement for a relatively complex calculation of optimal switching sequence, i.e., on and off transistor times, which cannot be easily realized with analog hardware. In [12], a more practical implementation, achieving optimal response for a wide range of voltage reference changes and a fast but still suboptimal response for the load variations, was presented. It combines linear and nonlinear control utilizing both analog and digital circuits. The digital hardware ensures optimal response time for the voltage reference changes. In this case, the optimal switching sequences for all references are pre-calculated and stored in look-up tables. During load transients that are usually unknown, the presented controller applies constant-frequency

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analog hysteretic control, relying on the indirect output capacitor current measurements. A fully-digital optimal-time controller was shown in [13]–[16]. The proposed current-mode implementation is well suited for converters processing larger power than the systems targeted in this paper. By using superior flexibility and computational power of a digital processor it performs on-line calculation of the switching sequence resulting in the optimal response for various loads. In this solution, the fast transient response comes at the price of fairly complex controller hardware. Its practical realization requires a fairly powerful processor, a high-gain bandwidth current sensing/amplifying circuit and three high-sampling rate analog-to-digital converters (ADC). Because of that, in emerging digitally controlled low-power SMPS, where the hardware simplicity is a key requirement, equivalents of analog voltage mode PWM controllers [26] are mostly used. There, the hardware simplicity is one of the key requirements. Due to the sampling effect and inherent delays of digital systems, at the very best, the digital PWM controllers have dynamic characteristics comparable to their analog counterparts. Yet, potentially, they could offer advanced features such as auto-tuning [27]–[29], multi-mode operation, design flexibility and the design portability.

The main goal of this paper is to introduce a new digital controller with load transient response approaching physical limitations of a given power stage that is suitable for low-power SMPS. It can be realized with fairly simple components, allowing full utilization of the advantages of digital implementation without introducing a significant hardware overhead. The controller eliminates the delay-related problems of digital systems by using a simple continuous-time digital signal processor (CT-DSP) [30]–[33], which executes an algorithm for the optimal-time output voltage recovery. The algorithm relies on the capacitor charge balance principle [5], [7]–[9], [11], [13] and performs detection of the peak/valley point of the output voltage deviation to eliminate the need for a costly current sensing/amplifying circuit [34].

In the following section we describe system operation and briefly review basics of continuous-time digital signal processing. Section III explains the capacitor charge balance based algorithm of this controller. In Section IV, we describe the architecture of a novel application-specific CT-DSP that implements the algorithm. Section V shows results obtained with a dc-dc converter utilizing the continuous-time digital controller, as an experimental verification of the effectiveness of the proposed system and method.

II. System Description

The continuous-time digital controller of Fig. 1 has two distinctive modes of the output voltage regulation. In steady-state it operates as a conventional digital PWM regulator producing signal $c(t)$. Every $T_{\rm sw} = 1/f_{\rm sw}$, where $f_{\rm sw}$ is the switching frequency, the PID compensator calculates a new value $d[n]$, controlling the digital pulse-width modulator (DPWM), according to

$$d[n] = d[n-1] + Ae[n] + Be[n-1] + Ce[n-2] \qquad (1)$$

where, $e[n], e[n-1]$, and $\mathrm{e[n-2]}$ are digital equivalents of the present value of the output voltage error, and the errors of one

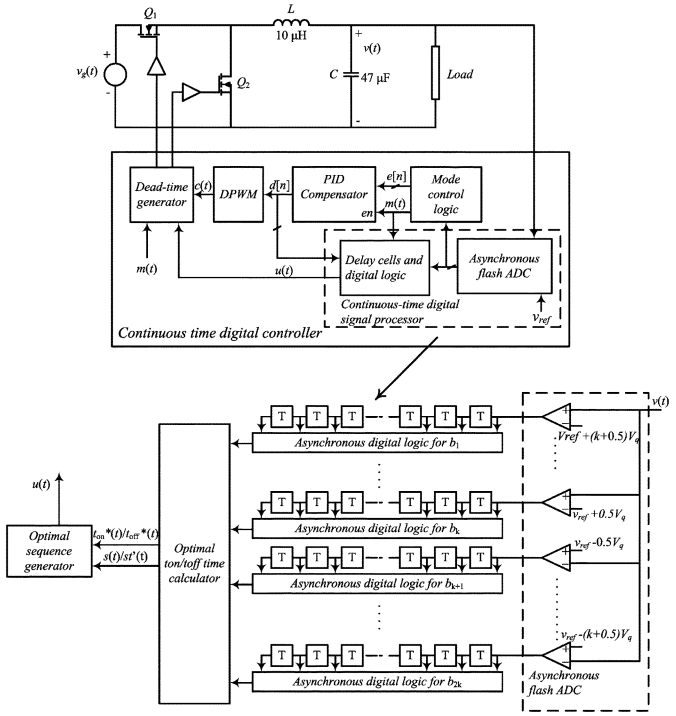

Fig. 1. Continuous-time digital controller regulating operation of a buck converter (top); a simplified structure of the continuous-time digital signal processor (CT-DSP) used for a fast voltage recovery (bottom).

and two switching cycles before, respectively. The coefficients A, B, and C are setting the compensator gain and zeroes [35].

As soon as a transient of the output voltage occurs, without waiting for any clock signal, the mode control logic detects the deviation and switches the system into dynamic mode. Then, the key part of this controller, the The application-specific continuous-time digital signal processor (CT-DSP) starts recovering the output voltage. The CT–DSP consists of a set of asynchronous comparators forming a windowed flash analog-to-digital converter (ADC), delay cells with a very short propagation time $T \ll T_{\rm sw}$, and asynchronous digital logic. The CT-DSP utilizes the general concept of the real-time processing of quantized analog signals in the digital domain, recently introduced by Tsividis [30]–[33]. This concept makes the full use of the best properties in both analog and digital signal processing. It combines the superior speed of analog implementation with the flexibility and computational power offered by digital hardware only. Any change at the input of the CT-DSP isinstantly sensed by the asynchronous ADC, captured by the set of delay cells, and processed by asynchronous digital logic. Having no synchronous sampling eliminates the aliasing effect that limits the bandwidth of conventional digital systems and also minimizes the quantization error [33]. The error is minimized due to the fact that at the comparators transition points the value of the input signal is exactly known and equal to the pre-defined thresholds. An additional benefit of continuous time digital signal processing is power savings [33]. The processor is active only when the input signal changes and, unlike clocked systems, does not burn power in steady state. This allows for the design of digital controllers taking very low-power, which is of very high importance in SMPS

for low-power systems, where the controller power consumption can have a significant effect on the overall power supply efficiency [27].

In this particular case, the CT-DSP implements a capacitor charge balance algorithm. It detects the time instant of the maximum output voltage deviation as well as the magnitude of that peak/valley point. Based on those two values only, the asynchronous digital logic determines the transistor on/off times $t_{\rm on}/t_{\rm off}$ that result in the fastest possible voltage recovery, i.e., optimal recovery time. The results of the calculation are sent to the *optimal sequence generator* creating the optimal on/off transistor switching sequence $u(t)$. When the mode control logic detects that the voltage is in a close proximity to its reference $V_{\rm ref}$, the CT-DSP passes the control task to the PID compensator.

III. Optimal Recovery Time Algorithm

The optimal recovery time algorithm, implementing charge balance principle [5], [7]–[9], [11], [13], can be described by observing Fig. 2 showing a buck converter's output capacitor voltage and inductor current recovery after a light-to-heavy load transient (or some other disturbance causing a loss of the output capacitor charge). The response can be divided into two phases. In the first phase, immediately following the transient, the CT-DSP turns on the main switch Q_1 (see Fig. 1) increasing the inductor current $i_L(t)$. The first phase ends when the maximum voltage deviation, in this case valley point, is detected. At this time instant *the load and inductor currents are equal*. In the following phase the CT-DSP calculates $t_{\rm on}$ and $t_{\rm off}$ transistor times (Fig. 2) and produces a switching sequence such that:

- at first, the inductor current further increases exceeding the load value, to make up for the loss of the output capacitor C charge

$$Q = C\Delta v \tag{2}$$

  where Δv is the maximum output voltage deviation during the transient;
- right after the optimal switching sequence is completed, the inductor current returns to its new steady-state value $I_L = I_{\rm load}$.

In other words, the optimal-time response is obtained by sizing the shaded triangle shown in Fig. 2, such that its area $Q_{\rm on} + Q_{\rm off}$ (the capacitor charge introduced by the inductor current) is equal to Q.

To simplify the calculation of $t_{\rm on}$ and $t_{\rm off}$ times, and consequently CT-DSP implementation, it is assumed that voltage deviation during transient is relatively small compared to its regulated dc value (less than 10 %), i.e., $v \approx V_{\rm ref} = V_{\rm out}$, which for most properly designed power supplies is the actual case.

Under such an approximation, the amounts of charge comprising the shaded triangle can be expressed as:

$$Q_{\rm on} = \int_0^{t_{\rm on}} \int_0^t \frac{V_g - V_{\rm out}}{L} dt d\tau \tag{3}$$

$$Q_{\rm off} = \int_0^{t_{\rm off}} \int_0^t \frac{V_{\rm out}}{L} dt d\tau \tag{4}$$

where V_g is the input voltage of the converter.

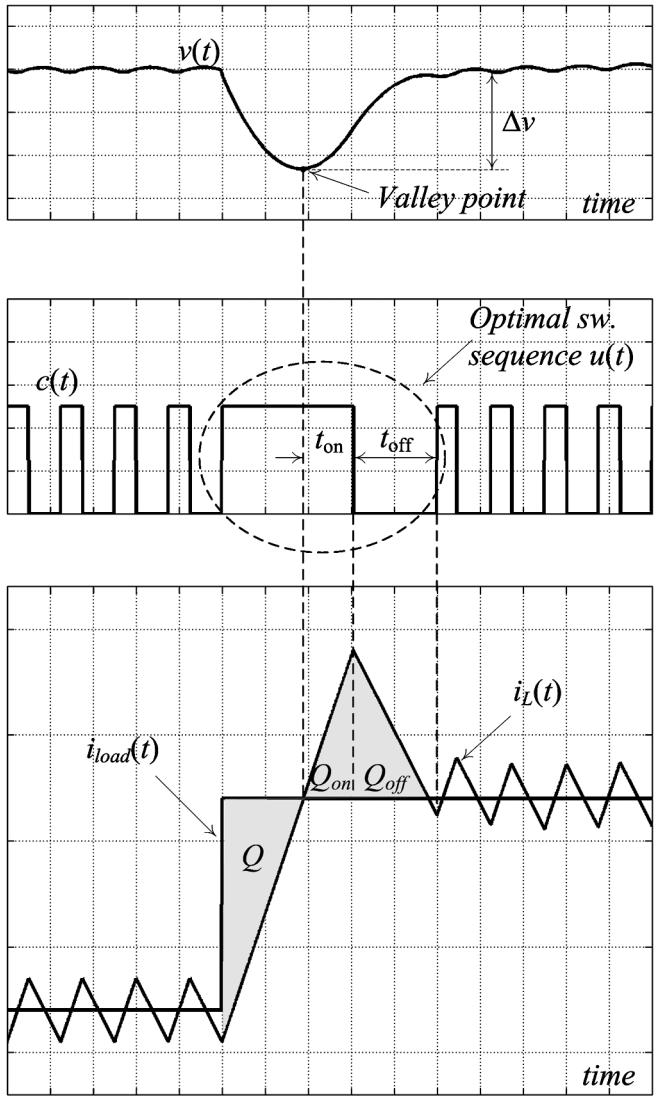

Fig. 2. Optimal recovery after a disturbance causing the output voltage drop. Top: the output capacitor voltage, $v(t)$; middle: gate-drive control signal $c(t)$; bottom: inductor and load currents $i_L(t)$ and $i_{\rm load}(t)$.

Furthermore, by observing the waveform of Fig. 2 the relation between $t_{\rm on}$ and $t_{\rm off}$ can be obtained geometrically

$$\frac{t_{\rm on}}{t_{\rm off}} = \frac{Q_{\rm on}}{Q_{\rm off}} = \frac{V_{\rm out}}{V_g - V_{\rm out}}. \tag{5}$$

By combining (2), (3), and (4) and the capacitor charge balance equation

$$Q_{\rm on} + Q_{\rm off} = Q = C\Delta v \tag{6}$$

we derive the following expressions for the optimal transistor on and off times:

$$t_{\rm on} = \sqrt{\frac{2LC\Delta v V_{\rm out}}{V_g(V_g - V_{\rm out})}} = k_1 \frac{D}{\sqrt{1-D}}\sqrt{\Delta v}, \tag{7}$$

$$t_{\rm off} = \sqrt{\frac{2LC\Delta v(V_g - V_{\rm out})}{V_g V_{\rm out}}} = k_1\sqrt{1-D}\sqrt{\Delta v}, \tag{8}$$

where D is the steady-state value of duty ratio, and $k_1 = \sqrt{2LC/V_{\rm out}}$.

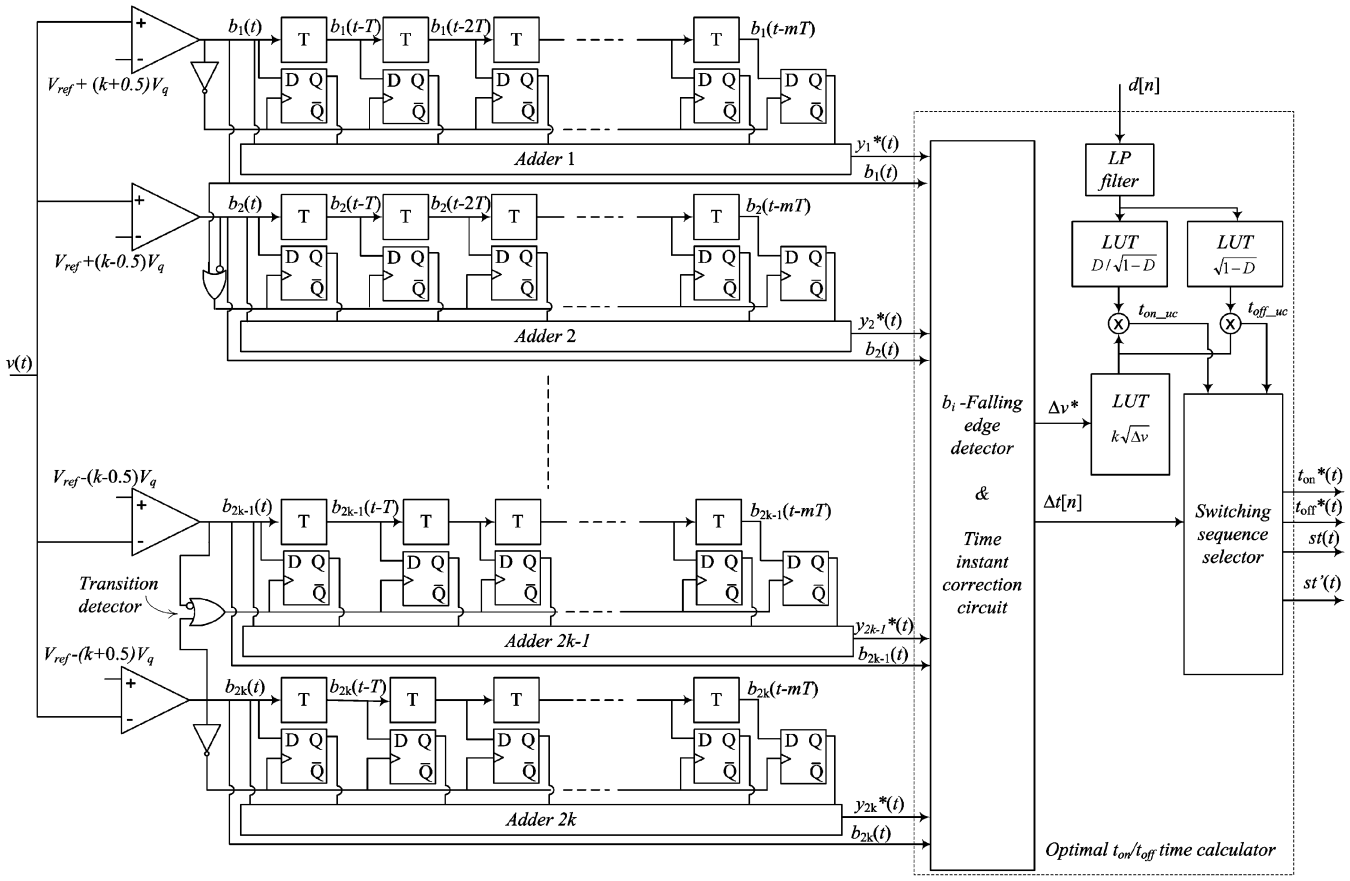

Fig. 3. Architecture of the application-specific continuous-time digital signal processor.

It can be easily shown that the same results for optimal $t_{\rm on}$ and $t_{\rm off}$ times are obtained for a heavy-to-light load transition, with a difference that the switching sequence is reversed. Analysis for other converter topologies yields optimal times expressions of similar complexity.

IV. Practical Implementation

Seemingly, the practical implementation of (7) and (8) requires a fairly powerful processor as well as fast and accurate analog hardware. However, as shown in this section, by utilizing digital correction of measurement errors and easily accessible information of the PID loop, this application specific CT-DSP can be realized with simple elements.

A. Application Specific CT-DSP

The architecture of the application-specific continuous-time digital signal processor for obtaining the optimal switching sequence and its waveforms during the recovery from a voltage drop are shown in Figs. 3 and 4.

The CT-DSP has two main blocks. The first comprising comparators, delay cells, and adders, captures the time instant and magnitude of the maximum deviation, i.e., valley point. The second block is the optimal $t_{\rm on}/t_{\rm off}$ calculator. It creates control signals for the optimal switching sequence (Fig. 1). After a comparator $i, 0 \leqslant 2k$, is triggered by a change of the output voltage, the corresponding continuous-time digital signal $y_i^*(t)$ (Fig. 4) is generated. Like the signals of conventional continuous-time systems, it can start at any point in time without a sampling delay, which typically exists in clocked digital systems. The digital value of $y_i^*(t)$ is calculated by an asynchronous adder. It is a stair function with the time step T and magnitude proportional to the number of delay cells signal $b_i(t)$ has propagated through.

The rise of $y_i^*(t)$ ends when the comparator i resets to zero or a neighboring one is triggered. The change of comparators states is sensed by a simple detector (Fig. 3) and, at that point, the state of $y_i^*(t)$ is captured with D-latches. In this way the conversion of a short time interval between two changes of comparators' states into a digital value is performed, with the time resolution equal to the propagation time of a delay cell. The value produced by the comparator that is last to set and first to reset is used to determine the time instant of the valley point shown in Fig. 2, is the time reference for $t_{\rm on}$ and $t_{\rm off}$ time intervals. For the voltage deviation given with the example of Fig. 4 the continuous-time digital signal $y_5^*(t)$ is used for the instant determination.

At the same time, detection of the magnitude of the maximum voltage deviation is performed by the block named b_i-falling edge detector and time instant correction circuit, shown in Fig. 3. It detects the output of the comparator that first changes its state from high to low and, as described shortly, uses the results of time-to-digital output conversion, to precisely determine parameters of the extreme deviation point.

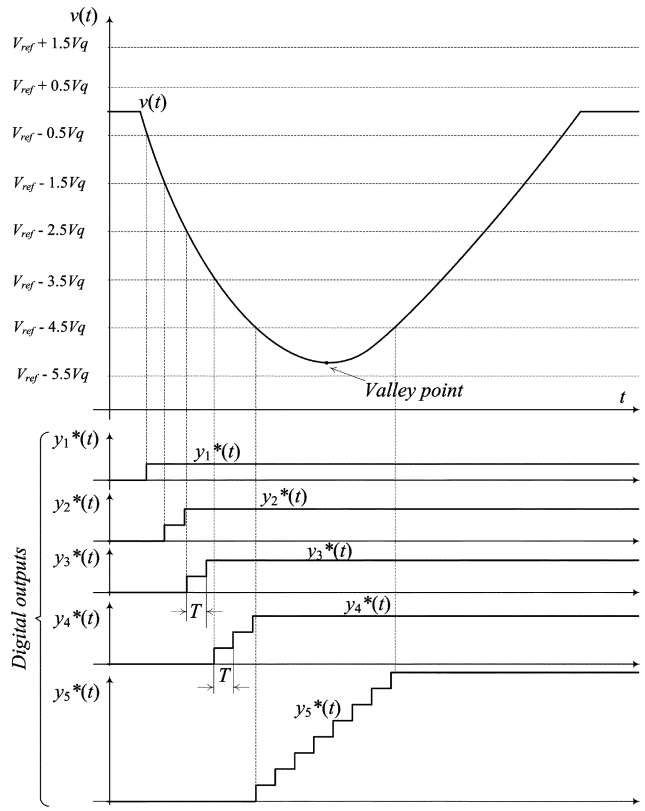

Fig. 4. Main signals of the application-specific continuous-time digital signal processor during a voltage dip. Top: output voltage. Bottom five: continuous-time digital outputs.

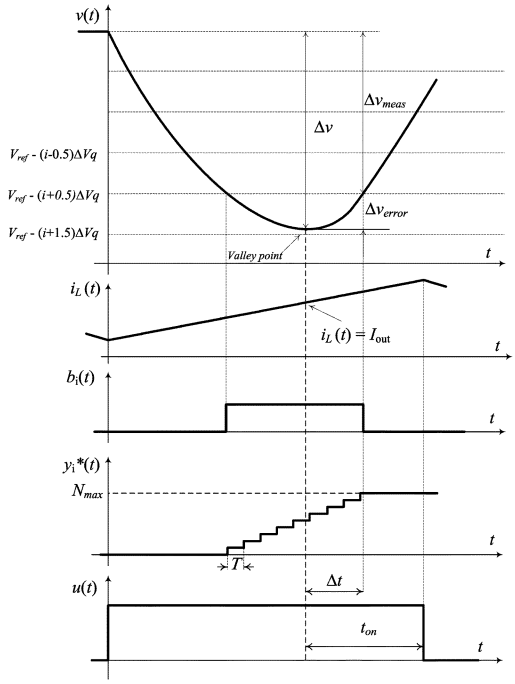

Fig. 5. Signals of the CT-DSP during a voltage dip. Top to bottom: output voltage $v(t)$, inductor current $i_L(t)$, the output of the last triggered comparator $b_i(t)$, corresponding continuous-time digital signal $y_i^*(t)$, the optimal switching sequence $u(t)$.

To eliminate the need for an extra ADC, out of the two forms of (7) and (8), the equations for calculating $t_{\rm on}$ and $t_{\rm off}$ not requiring information about the input voltage V_g are implemented. The obtained amplitude of the voltage deviation is fed to a look-up table (LUT) that produces $k_1\sqrt{\Delta v[n]}$. Then, the output of the LUT is multiplied by $D/\sqrt{1-D}$ and $\sqrt{1-D}$, respectively. Immediately after the computations of the optimal times are completed the results are sent to the optimal sequence generator of Fig. 1, together with a peak detection signal $st(t)$, used for the generator triggering.

The steady-state duty ratio value D is obtained by low-pass filtering of the PID compensator output, as shown in Fig. 3. Due to recent advances in mass-memory design [37] the above mentioned square-root functions are also implemented with look-up tables occupying a small silicon area.

1) Digital Correction of Measurement Errors: To accurately capture the point of the maximum voltage deviation a large number of very precise high-speed comparators and delay cells can be used. However, such a solution would probably increase the controller complexity so that its implementation is impractical, both in terms of the overall system cost and its power consumption. Instead, we use a windowed flash ADC, with large quantization steps V_q, sized to barely satisfy the output voltage regulation requirements [27]. This selection significantly simplifies the hardware by minimizing the number of comparators, but at the same time compromises the accuracy in finding both the magnitude and time instant of the peak/valley point.

The effects of the coarse ADC resolution are demonstrated in Fig. 5. We can see that, since the valley occurs in between two quantization thresholds, the calculation of the deviation parameters is delayed by Δt. It is possible only after $y_i^*(t)$ reaches its final value $N_{\max}$. Also, an error in amplitude measurement $\Delta v_{\rm error}$ can be observed.

To compensate for these, digital error correction is applied. First, the delay is approximated as $\Delta t = N_{\max}T/2$ and used for the correction of the calculated $t_{\rm on}$ value, as shown in Fig. 3. The estimated delay time is also used for effective resolution improvement, where the quantization error for the buck converter of Fig. 1 is calculated as

$$\begin{aligned}\Delta v_{\rm error} &= \frac{1}{C}\int_{t_0}^{t_0+\Delta t} \Delta i_L \cdot d\tau \\ &= \frac{1}{C}\int_{t_0}^{t_0+\Delta t} \frac{V_g - V_{\rm out}}{L}\cdot\tau\cdot d\tau \\ &= \frac{1}{2}\frac{V_g - V_{\rm out}}{LC}\Delta t^2 = k_2\frac{1-D}{D}\Delta t^2 \end{aligned} \tag{9}$$

and added to the initially measured voltage deviation $\Delta v_{\rm meas,}$, where $k_2 = V_{\rm out}/(2LC)$.

It might be interesting to note that fast processing of the signals during transients could also be obtained with an oversampling ADC and a powerful processor. However, to achieve the same time resolution as that of a delay cell, a very high frequency ADC would be needed. For example, for a time step of 1 ns, easily achievable with a 5-transistor delay cell [38], an ADC with 1-GHz sampling rate would be required. Such an ADC is probably more complex and costly than a complete low-power SMPS.

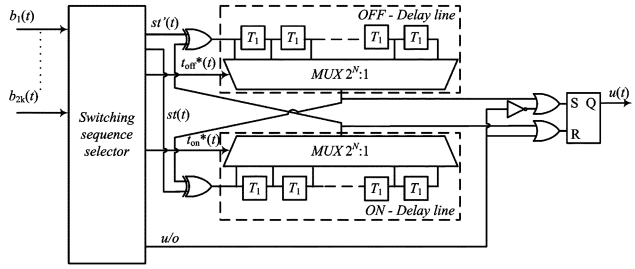

Fig. 6. Optimal sequence generator.

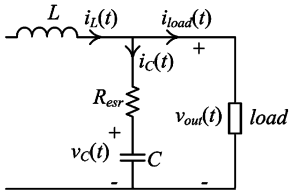

Fig. 7. Model of the output filter of a buck converter that includes capacitor ESR.

B. Optimal Sequence Generator

The optimal sequence generator is shown in Fig. 6. It comprises two delay lines for generating $t_{\rm on}$ and $t_{\rm off}$ time intervals, an S-R latch, and 2-XOR gates. An output voltage deviation activates the generator. At that time, the switching selector recognizes the type of the transient and the SR-latch controlling the transistor Q_1 of Fig. 1 is set or reset, through the u/o signal. After the maximum voltage deviation is sensed and optimal times calculated either the triggering pulse $st(t)$ for the ON-delay line or $st'(t)$ for the OFF-delay line is created, depending on the type of transient. As a result, $u(t)$ goes from high to low after $t_{\rm on}$ in the case of a voltage dip or in the other direction after an overshoot. As soon as the initially excited delay line changes its output, it triggers the opposite line as well as the SR latch changing the value of $u(t)$. After the signal propagates through the second delay line the optimal switching sequence is completed and the PID compensator of Fig. 1 resumes voltage regulation.

C. Influence of the Output Capacitor and LC Parameter Variations

1) Equivalent Series Resistance: Even though this system is designed for low-power SMPS, where predominantly ceramic capacitors with very small equivalent series resistance (ESR) are used, it might be interesting to analyze the influence of a non-negligible ESR. Then, the output capacitor can be modeled as shown in Fig. 7 and the output voltage $v_{\rm out}(t)$ written as

$$\begin{aligned} v_{\rm out}(t) &= v_c(t) + R_{\rm esr} i_c(t) \\ &= v_c(t) - R_{\rm esr}(i_L(t) - i_{\rm load}(t)) \end{aligned} \tag{10}$$

where $R_{\rm esr}$ is the ESR value and $v_c(t)$ voltage across the ideal capacitor. Ideally, ESR should not affect the optimal switching sequence. At the point where the inductor and load currents are the same, i.e., $i_c(t) = 0$, the ESR does not have any influence on the output voltage deviation and the equations for the optimal sequence remain the same as in the ideal case. The sequence should start when the zero capacitor current is detected and have the $t_{\rm on}$ and $t_{\rm off}$ times defined by (8) and (9). However, as described below, ESR causes the peak/valley point to happen at $i_c(t) \neq 0$ and erroneous detection of the key time instant. As a consequence, the $t_{\rm on}$ and $t_{\rm off}$ times can be miscalculated and a suboptimal switching sequence created.

To quantify this influence we observe the buck converter of Fig. 1, as an example. Again, a light-to-heavy load transient is analyzed, where at $t = 0$ a step of $\Delta I_{\rm load}$ occurs and the CT-DSP immediately turns on the main switch Q_1 responding to the transient. For this case (10) can be rearranged as

$$\begin{aligned} v_{\rm out}(t) = V_{\rm out} + R_{\rm esr}\left(\frac{V_g - V_{\rm out}}{L}t - \Delta I_{\rm load}\right) \\ + \frac{1}{C}\int_0^t \left(\frac{V_g - V_{\rm out}}{L}t - \Delta I_{\rm load}\right) dt. \end{aligned} \tag{11}$$

Now the valley happens at the point where the time-derivative of (11) is zero. By finding the derivative and replacing the result in (11) both the time instant of the valley point $t_{\rm esr}$, and its magnitude $\Delta v_{\rm esr}$ can be obtained

$$t_{\rm esr} = \frac{LC}{V_g - V_{\rm out}}\Delta I_{\rm load} - CR_{\rm esr} \tag{12}$$

$$\begin{aligned} \Delta v_{\rm esr} = \left(\frac{\Delta I_{\rm load} t_{\rm esr}}{C} - \frac{V_g - V_{\rm out}}{LC}\frac{t_{\rm esr}^2}{2}\right) \\ + R_{\rm esr}\left(\Delta I_{\rm load} - \frac{V_g - V_{\rm out}}{L}t_{\rm esr}\right). \end{aligned} \tag{13}$$

It can be seen that the ESR causes the valley to happen before $i_c(t) = 0$ (while $i_{\rm load}(t)$ is still larger than $i_L(t)$) and, consequently, a pre-mature triggering. This effect also increases the magnitude of the valley and, as shown in the following section, in most of the practical cases, causes an undershoot and a slower than ideal response.

From (12), we can see that compared to the ideal case, the valley leads by $\tau_{\rm esr} = CR_{\rm esr}$. If $\tau_{\rm esr}$ is known with a certain accuracy it can be taken into account and the CT-DSP algorithm modified accordingly. More precisely, the sampling of the peak deviation and the triggering of the switching sequence can be delayed by $\tau_{\rm esr}$ to compensate for the ESR influence.

2) LC Parameter Variations: From (7) and (8) it can be seen that the parameter k_1, depends on the L and C values affecting the calculation of $t_{\rm on}$ and $t_{\rm off}$ times. Hence, the tolerance of the components and their changes due to external influences can result in a non-optimal switching sequence. However, since k_1 depends on the square root of the *LC* product, this effect is often small over a relatively large range of the product variations, causing a slight undershoot or overshoot that can be compensated by the PID regulator.

In the case of a large variation, auto-compensation methods can be applied [29], [40]. For example, the gain k_1 can be adjusted in two steps, as demonstrated in a predictive current mode controller [40] suffering from a similar problem. First, the initial value of k_1 can be set, then, in the next step, it can be adjusted depending on the size of undershoot/overshoot. A similar two-step gain correction technique for the compensation of the *LC* variations has also been applied in a modification of the previously mentioned all-digital optimal controller [15]. Alternatively, the

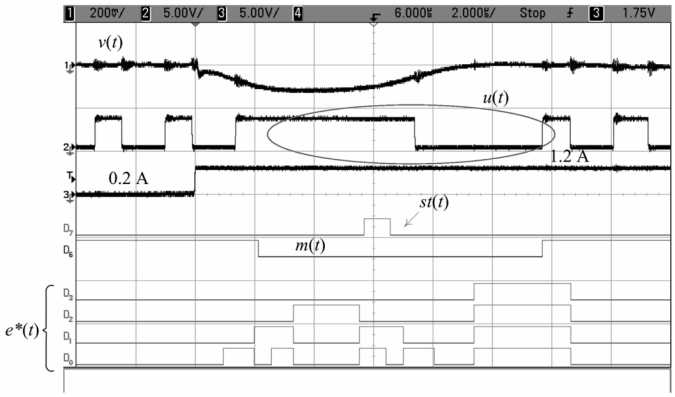

Fig. 8. Signals of the CT-DSP during a 0.2 A to 1.2 A load transient. Ch.1: Output voltage $v(t)$, 200 mV/div; Ch 2: gate-drive signal; Ch.3: control signal for load transient circuit; D0-D3: binary-weighted continuous-time digital error $e^*(t)$ of the PID compensator; D6: mode control signal; D7: peak detection signal $st(t)$. The time scale is 2 μs/div.

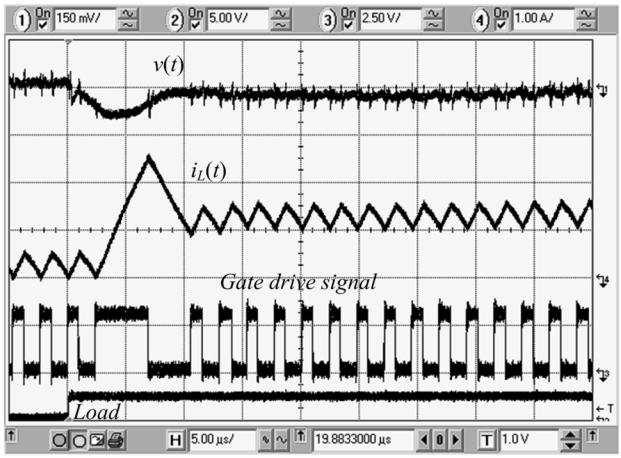

Fig. 9. Voltage and current waveforms of the experimental system during a 0.2 A to 1.2 A load transient. Ch.1: Output voltage $v(t)$, 150 mV/div—ac; Ch.2: the control signal of a load change circuit; Ch.3: Gate drive signal; Ch.4: Inductor current $i_L(t)$, 1 A/div—dc; The time scale is 5 μs/div.

LC product can be estimated from the frequency of limit-cycle oscillations, as described in [29].

V. Experimental System and Results

Based on the diagrams shown in Figs. 1, 3, and 6 an experimental controller system was built around a 5 V to 1.8 V, 5 W buck converter operating at switching frequency $f_{\rm sw} = 400$ kHz. The continuous-time digital controller is implemented with an FPGA based system as well as with commercially available comparators and programmable delay lines. To design an asynchronous flash ADC, only eight comparators were used and a constant quantization step of $V_q = 25$ mV was set. The delay lines are comprised of 64 cells, each having 40-ns propagation time. They provide sufficiently long total delay to capture a time interval between two successive triggerings of CT-DSP's comparators which is usually shorter than the switching period. It should be noted that in on-chip implementation, where it is desired to minimize silicon area, the number of cells can be significantly reduced by sharing only one delay line among all comparators and using current-starved delay elements. The propagation time of the current starved cells can be shorter than 1 ns, allowing the use of the continuous-time digital controller in SMPS operating at switching frequencies of several MHz and higher.

A. Functional Verification

To verify the operation of the developed continuous-time digital signal processor, its key signals were observed during a 0.2 A to 1.5 A load transient. The results are shown in Figs. 8 and 9. As it can be seen from Fig. 8, right after the transient, the mode signal $m(t)$ (also shown in Fig. 1) enables the CT-DSP and the transistor Q_1 stays in on state (had it been open it would have turned on immediately). When the peak point is detected, the detection signal $st(t)$ is activated, with a delay Δt. The remaining part of the optimal $u(t)$ is generated by the programmable delay line and the voltage recovers in a single on-off switching cycle. Once the steady state is reached, the mode control signal disables the CT-DSP and the PID compensator of Fig. 1 used for the regulation and compensation of small voltage variations is active again. Waveforms of the binary weighted error signal that is fed into the PID compensator are also shown.

The waveforms also verify proper operation of the digital error correction block described in Section IV.A.1 It can be seen that due to the coarse quantization steps of the flash ADC the peak detection signal $st(t)$ is delayed. Still, the previously described algorithm takes the delay into account and corrects the transistor on time to achieve virtually optimal response.

It should be noted that compared to the ideal case, shown in Fig. 2, a slight delay in the reaction to a load transient, indicated by signal $m(t)$, exists. This is because of the digital logic for load transient recognition that only reacts on the output voltage variations larger than 2 quantization steps and finite propagation time of the FPGA's digital circuits. Since the $t_{\rm on}$ and $t_{\rm off}$ times are calculated with respect to the peak/valley point, this delay does not affect CT-DSP algorithm but does have influence on the overall response time. If the CT-DSP is fully implemented on a chip, this effect can be significantly minimized by using faster application-specific digital logic and/or a simple high-pass filter for transient detection.

Fig. 9 shows experimental voltage and current waveforms similar to the idealized signals of Fig. 2. As described in Section III, over the duration of the optimal switching sequence the inductor current exceeds the load value to make up for the lost capacitor charge and returns to the new steady state right at the end of the sequence.

Also, it can be seen that the PID compensator completely eliminates the steady state error, which the CT-DSP itself is not able to accomplish, due to components variations and other imperfections that are not take into account in the optimal sequence calculations.

B. Performance Comparison

To verify the advantages of the continuous-time digital controller over commonly used voltage mode digital PWM regulators, load transient response with and without the CT-DSP based recovery mechanism was compared. The conventional

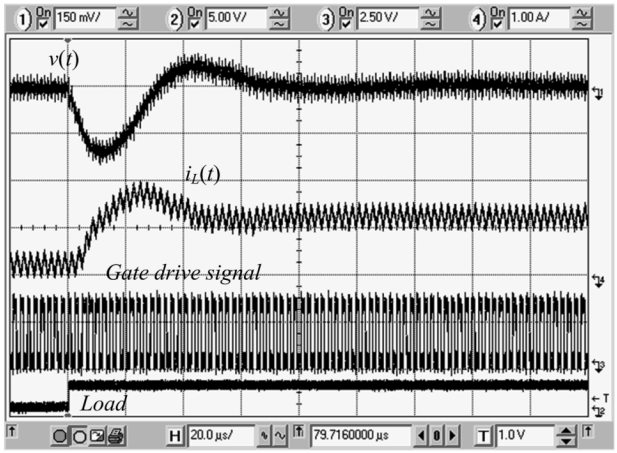

Fig. 10. PID controller's response to a 0.2A to 1.2A load step change. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

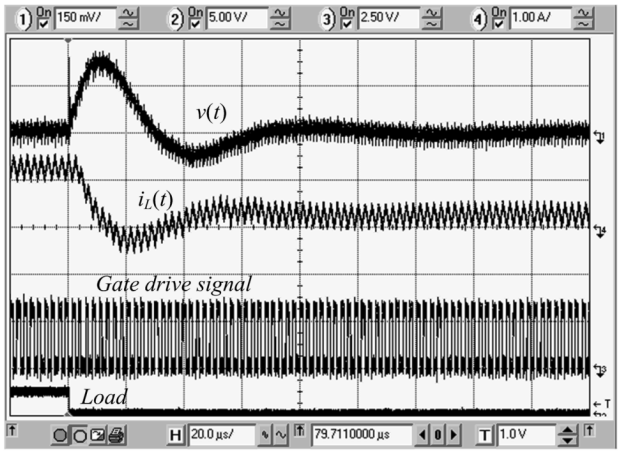

Fig. 12. PID controller's response to a 1.2 A to 0.2A load step change. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

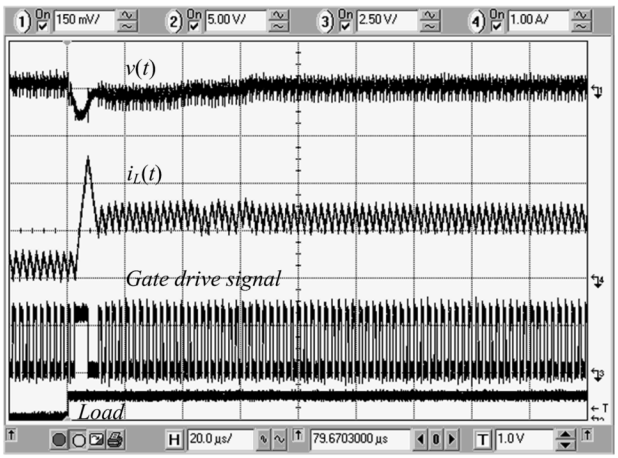

Fig. 11. CT-DSP controller's response to a 0.2A to 1.2A load step change. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

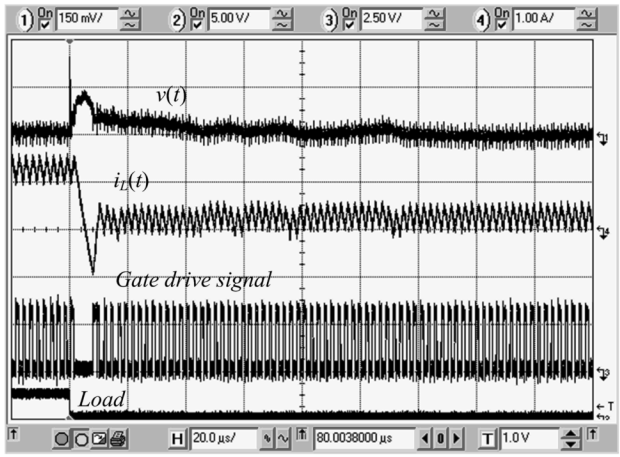

Fig. 13. CT-DSP controller's response to a 1.2 A to 0.2 A load step change. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

controller has a PID compensator designed such that the crossover frequency of the system is $f_c \approx f_{\rm sw}/15$, which is a common choice in the conventional digital PID design [27] where the sampling imposes bandwidth limitations. The results for heavy-to-light and light-to-heavy load transients are shown in Figs. 10 –13. They verify that the CT-DSP results in much better load transient response. In this case, the recovery time is about three to four times shorter and the overshoots/undershoots are about three times smaller, allowing for the proportional reduction of the output capacitor [2]. The response of the CT-DSP is practically limited by the power stage inductor and capacitor values only.

C. System Behavior for Parameter Variations

To show the influence of *LC* variations and that of the ESR two modifications on the power stage of the original system were performed while the CT-DSP algorithm was left unchanged. First, the value of the output ceramic capacitor was changed by 20%. Then, the widely available ceramic capacitor with $R_{\rm esr}$ smaller than 5 m Ω was replaced with a tantalum capacitor, having approximately seven times larger ESR.

Fig. 14 shows a load transient response for the case when the output capacitance is 80% of the rated value. It can be seen that in this case $t_{\rm on}$ and $t_{\rm off}$ times, given by (7) and (8) are miscalculated so they are larger than optimal, causing a 70-mV overshoot after the switching sequence is completed. This overshoot is followed by a smaller much smaller dip. Even in this case the load transient causes about 2.5 times smaller deviation than when the PID regulator is used and about 1.5 times shorter settling time. As mentioned earlier, by applying a two-step gain correction algorithm [15], [40] or the auto-tuning methods presented in [27], [29] this response can be improved.

A load transient response with a tantalum capacitor having large ESR ($R_{\rm esr} \approx 35$ m Ω) is shown in Fig. 15. As described in Section IV-C1, the ESR causes earlier triggering, a shorter capacitor charging time than optimal, and incomplete recovery of the lost capacitor charge after the sequence produced by the CT-DSP is completed. However, since at the end of the sequence a new steady-state is almost reached and voltage deviation is

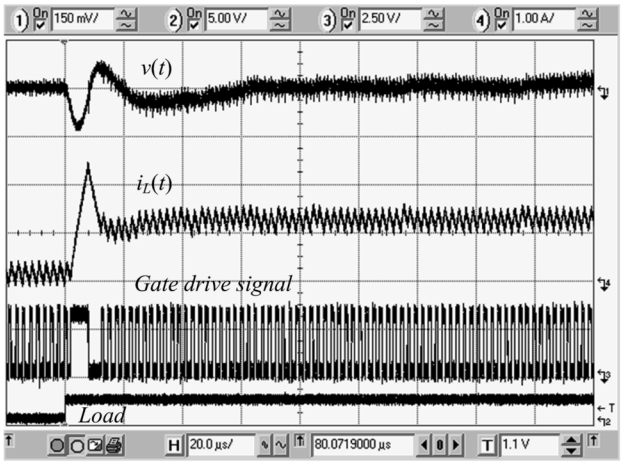

Fig. 14. CT-DSP controller's response to a 0.2A to 1.2A load step change for the case when the output capacitance is 20% smaller than the rated value. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

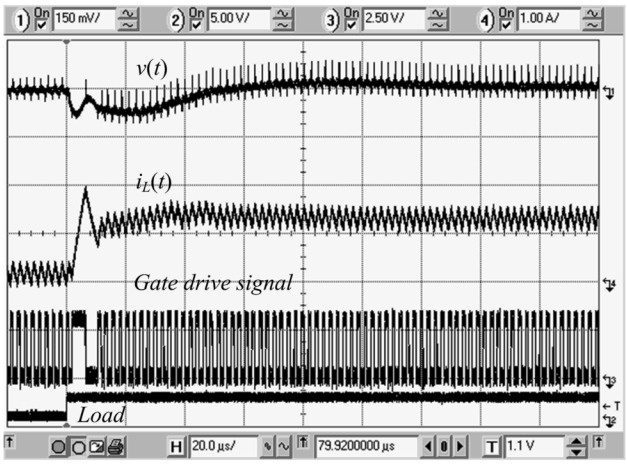

Fig. 15. CT-DSP controller's response to a 0.2A to 1.2A load step change for the case when the. Ch.1: output voltage $v(t)$, 150 mV/div—ac; Ch.3: gate drive signal, 2.5 V/div; Ch.4: load change command; Ch.4: inductor current $i_L(t)$, 1 A/div. Time scale is 20 μs/div.

relatively small, the PID compensator compensates for the mismatch. By comparing the response with that of the conventional PID, shown in Fig. 10, we can see that even in the presence of a large ESR the proposed method significantly improves the load transient response.

VI. Conclusion

A voltage mode digital controller for low-power high-frequency dc-dc converters that has a recovery time approaching physical limitations of a given power stage is presented. To achieve such a quick response, during transients the controller utilizes an asynchronous windowed flash analog-to-digital converter, delay lines, and digital logic forming an application-specific continuous-time digital signal processor (CT-DSP), which is the key part of this new system. The CT-DSP processes signals that are continuous in time and have a quantized magnitude to exploit the advantages of both digital and analog worlds. By eliminating sampling, the characteristic for conventional digital systems, the aliasing and delay problems are eliminated allowing for significant increase in processing speed. On the other hand, the quantization in amplitude makes advanced data processing, a main advantage of digital implementation, possible. To eliminate the need for current measurement, and consequently, significantly simplify the system implementation, the CT-DSP implements a capacitor-charge balance based algorithm. Based on the maximum amplitude of voltage deviation and its time instant, it calculates the optimal on and off times of the power switch resulting in virtually the fastest recovery time possible. To further ease the hardware requirements, a digital error correction, minimizing the magnitude quantization effects and compensating for delays in the system, is applied. An FPGA-based controller prototype was built and tested with a low-power dc–dc converter operating at 400-kHz switching frequency. The experimental results show very fast recovery time limited by the values of the power stage inductor and capacitor only.

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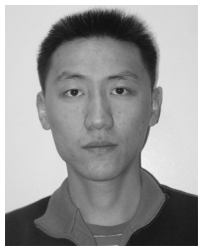

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