Predictive Efficiency Optimization for DC–DC Converters With Highly Dynamic Digital Loads

Olivier Trescases, *Member, IEEE*, Guowen Wei, *Student Member, IEEE*, Aleksandar Prodić, *Member, IEEE*, and Wai Tung Ng, *Senior Member, IEEE*

***Abstract*—This paper presents a novel technique and system for increasing the efficiency of dc–dc converters that supply dynamic electronic loads, such as modern audio and video equipment and other devices whose power consumption largely depends on the digital data they process. The optimization does not require a current-measurement circuit and is well-suited to portable applications. It is based on a real-time prediction of the dc–dc converter output current from easily accessible digital data streams present in the targeted loads. The result of the prediction is used for dynamic adjustment of the power-stage transistor size and/or for switching into pulse-frequency-mode of output voltage regulation, in order to maximize the instantaneous converter efficiency on-the-fly. The use of a segmented power-stage allows the effective power-transistor size to be changed on-the-fly, and the tradeoff between the gate-drive and rms conduction losses is continuously optimized over the full range of operation. The effectiveness of the optimization is demonstrated on an experimental system, including a 1-W digitally controlled 4-MHz, 3.6 V–1.8 V buck converter with an integrated segmented power-stage and a digital high-fidelity class-D audio amplifier acting as the digital load. The results show a good agreement between the digitally predicted and actual dc–dc converter load current, as well as a reduction in total energy consumption of up to 38%.**

***Index Terms*—Class-D amplifier, digital control, efficiency optimization, low-power dc–dc converter, segmented power stage.**

I. Introduction

MODERN switched-mode power supplies (SMPS) for low-power portable applications often employ a number of efficiency improvement techniques to extend battery life. The techniques usually utilize dynamic adjustments, where the SMPS mode of operation is dynamically changed with the goal of achieving the maximum power-conversion efficiency for a given operating condition. Some examples include dead-time optimization [1]–[4], reconfiguration of the power-stage transistors [5], [6], gate-drive circuits with charge conservation [7]–[9], and combined pulsewidth/pulse-frequency modulated (PWM/PFM) control [10], [11]. In all of these methods, the power-stage's operation mode is optimized around a certain steady-state operating point, according to input voltage and the load current. In most cases, the current is either measured directly through integrated sensing schemes such as senseFET [12], [13] or estimated using digital algorithms [4], [5], [14].

Even though the aforementioned techniques greatly improve the overall converter efficiency in numerous applications, under highly dynamic loads their effect is limited, or in some cases even negative. They react only after the load-change has happened and a steady-state reached. Because of this delay, the SMPS spends a significant amount of time operating in-between modes, not achieving maximum efficiency. As a result, the current-sensing and estimation-based efficiency optimization techniques have not found a wider use in a large number of systems having digitally fed electronic loads, such as portable devices. These applications include speakers with audio amplifiers, liquid crystal displays (LCDs), LED arrays, small motors, and enhanced data rates for global evolution (EDGE) amplifiers. A general block diagram of a power-supply system with a digitally fed electronic load is given in Fig. 1(a). In most cases, an analog-controlled SMPS provides a tightly regulated supply voltage to the load, which can be modeled as a signal dependent current-source. The source's current-draw is a linear or a nonlinear function of a processed digital signal $s[m]$, i.e., $I_{\text{out}} = f\{s[m]\}$.

The main goal of this paper is to introduce a new load-prediction technique and system for improving the efficiency of SMPS supplying digital electronic loads, as shown in Fig. 1(a). The optimization relies on the fact that, in most of the targeted applications, an easily accessible digital stream $s[m]$ can be used to directly predict the load-current, without requiring current-sensing hardware. Consequently, the mode-switching delay that causes additional losses in conventional measurement and steady-state estimation based methods can be eliminated.

The interaction with sophisticated digital loads not only improves the overall converter efficiency, but also eliminates the need for any analog circuitry for current-measurement, making the system suitable for implementation in advanced digital CMOS technologies [15]. The new power-supply system, shown in Fig. 1(b), consists of a segmented power-stage, a multimode digital controller, and a digital load-predictor, which is the key element.

The predictor estimates the real-time value of the load current based on the digital stream $s[m]$. Accordingly, the multimode digital controller changes the mode of the power-stage operation to optimize the efficiency at each operating point. In the ideal

Manuscript received May 8, 2007. Published July 7, 2008 (projected). This work was supported by NSERC, CMC, Auto21, U of T Open fellowship, Fuji Electric Device Technology Co., Ltd., and Fuji Electric Advanced Technology Co., Ltd. Recommended for publication by Associate Editor S. Pekarek.

O. Trescases was with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada. He is now with Infineon Technologies AG, 9500 Villach, Austria (e-mail: trescas@vrg.utoronto.ca).

G. Wei was with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada. He is now with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA.

A. Prodić and W. T. Ng are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2008.924823

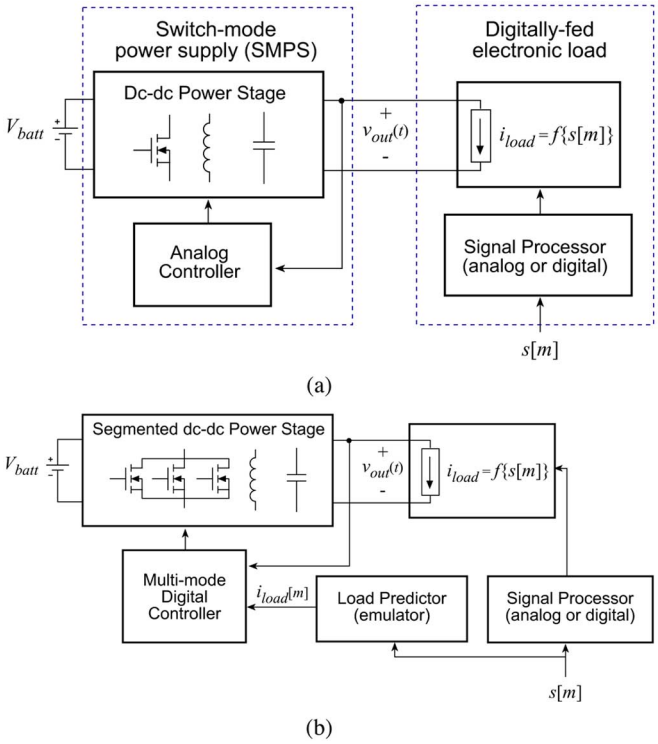


Fig. 1. (a) Conventional power system for supplying digitally fed electronic loads. (b) Digitally controlled predictive efficiency optimization system.

case, the timing of the multimode controller and the change of load current are perfectly synchronized so that the SMPS always operates at the most efficient operating point. The actual minimization of the SMPS losses is performed by two means. First, as shown in Fig. 1(b), the lumped power-stage transistor is replaced with a segmented switcher, where several smaller transistors are connected in parallel [16]. Depending on the load conditions, the number of active transistors is dynamically changed to optimize the tradeoff between the switching and conduction losses. Second, at light loads, the converter switches from PWM mode of output voltage regulation to PFM, to reduce the dominant switching losses.

In Section II, we show how the new optimization technique is implemented on a practical system. As an application example of the optimization technique, a digital class-D audio amplifier and a speaker fed by a digital pulse-code-modulated (PCM) stream are used. The system functional blocks and operation of the predictor are described in detail. Section III is devoted to the segmented power-stage design. We address the problem of reduced efficiency of conventional lumped power transistor SMPS when operating at medium and light loads. The tradeoff between conduction, gate-drive, and hard-switching transistor losses is briefly explained in order to justify the use of a segmented power-stage. Section IV includes details regarding the practical implementation of the proposed system, as well as experimental results. This section also addresses the effect of imperfect synchronization between the predicted and actual current and shows that even when a relatively crude estimation method is applied, a significant energy savings of up to 38% can be achieved, compared to non-optimized systems.

II. Application to a Digital Class-D Audio Amplifier

In this section, we demonstrate how the load-prediction optimization introduced in the previous section can be applied to fully digital class-D audio amplifier. Class-D amplifiers have a higher efficiency than their class-AB counterparts due to switched-mode operation. These amplifiers are frequently used in portable applications, where they account for a significant portion of the total power-consumption. The applications include MP3 players, cell phones, personal data assistants (PDAs), portable computers, and camcorders.

The architecture of a typical digital class-D amplifier is shown in Fig. 2. A PCM audio stream $s[m]$ with a standard sampling rate of 44.1 kHz is up-sampled, fed to a digital noise shaping $(\Delta\Sigma)$ modulator, and then to a digital pulsewidth modulator (DPWM). In some cases, a 1-b $\Delta\Sigma$ modulator architecture may be used [17]. It eliminates the need for the DPWM, while guaranteeing high linearity at the output. A high-Q *LC* reconstruction filter extracts the original audio signal from the PWM output.

The H-bridge power-stage produces $v_{\rm spk} = (2d_{\rm amp}-1)V_{\rm bus}$, where $d_{\rm amp}$ is the duty-cycle of the DPWM output $c_{p1}(t)$ and $V_{\rm bus}$ is the bus voltage. The H-bridge power-stage topology is popular for achieving a relatively high power-supply rejection ratio (PSRR). Furthermore, it eliminates the need for ac-coupling capacitors and maximizes the output swing at the speaker terminals, resulting in a maximum delivered rms power of

$$P_{\max} = \frac{V_{\rm bus}^2}{2R} = \frac{V_{\rm batt}^2}{2R} \tag{1}$$

where R is the speaker resistance and a sinusoidal input is assumed. The distortion introduced by the nonideal power-transistors in the H-bridge can be suppressed using a local feedback loop [18]. In order to illustrate the operation of a class-D amplifier, the DPWM output signal $c_{p1}(t)$ and the filtered speaker voltage $v_p(t)$ are shown in Fig. 3 for an audio input $s[m]$ consisting of a 1.5-kHz single tone.

A. Class-D Amplifier Powered by a DC–DC Converter

The H-bridge of the digital open-loop class-D amplifier generally requires a low-noise power-supply; otherwise, the noise severely degrades the total harmonic distortion (THD) at the speaker terminals due to limited PSRR. In order to avoid signal-to-noise ratio (SNR) degradation, a dc–dc converter with tight output regulation is usually used for generating $V_{\rm bus}$. In addition, the dc–dc converter reduces the noise injected onto the battery terminals by the class-D amplifier. This minimizes the potential for conducted electromagnetic interference (EMI) problems with neighboring devices. As shown in Fig. 4, the resulting combination is equivalent to two cascaded dc–dc converters, where the second converter operates in open-loop. Dynamically, the class-D amplifier behaves as a positive incremental resistance, which simplifies the dc–dc converter compensation.

Using a buck topology in the dc–dc converter is common, though it reduces the maximum peak output-power that can be delivered to the speaker compared to (1)

$$P_{\max} = \frac{(V_{\rm batt}D)^2}{2R} \tag{2}$$

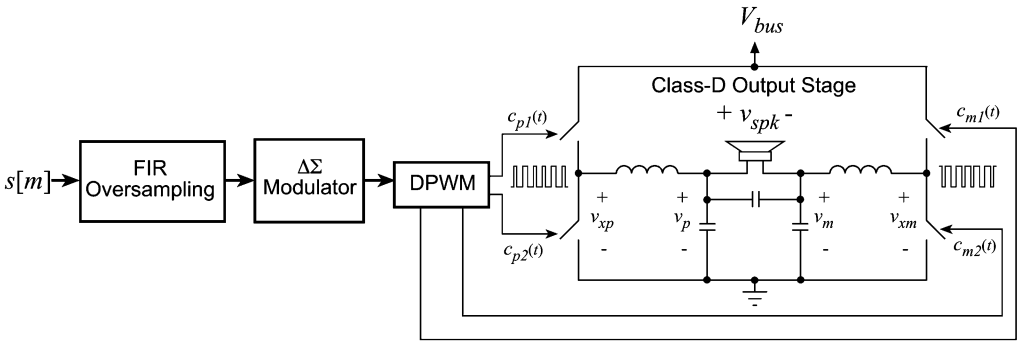


Fig. 2. Simplified architecture of a digital class-D amplifier with an H-bridge power-stage.

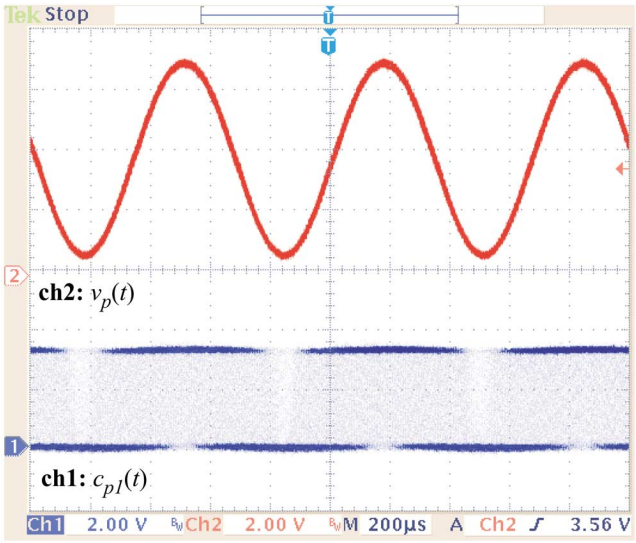


Fig. 3. Output of the class-D amplifier for a 1.5-kHz single tone audio input. Ch-1: $c_{p1}(t), 2\text{V/div}$; Ch-2: $v_p(t), 2\text{V/div}$.

where $D \leq 1$ is the steady-state duty-cycle of the buck converter.

Alternatively, a boost converter may be employed to raise V_{bus} above V_{batt} to increase $P_{\max}$. This is an attractive option in single-battery-cell powered devices, when high output power is desired at low battery voltages. While directly using a boost topology within the class-D power-stage is certainly more cost effective, it is not recommended in open-loop applications since the inherently nonlinear conversion ratio of the boost topology $(m = v_{\text{spk}}/v_{\text{batt}} = 1/(1 - d_{\text{amp}}))$ makes it very challenging to achieve high-fidelity sound over the full bandwidth and dynamic-range of the audio signal.

The switching-frequency of the dc–dc converter, f_{s1} can be significantly higher then the switching-frequency of the class-D amplifier f_{s2}. This differs from classical cascaded dc–dc converter design, where the downstream, or point-of-load, converter has the highest switching-frequency and bandwidth. In the case of open-loop digital class-D amplification with multibit $\Delta\Sigma$ modulation, the switching-frequency is, in part, constrained by the need for high linearity in the DPWM block, in order to achieve reasonable THD specifications (typically $\leq 0.1\%$). DPWMs based on delay-lines [19] used extensively in digitally controlled dc–dc converters to allow multi-MHz switching-frequency, are generally unsuitable for high-fidelity open-loop class-D amplifiers. This is mainly due to poor linearity compared to counter-based DPWMs, even despite calibration mechanisms [20]. Instead, counter-based DPWMs are used with a PLL-derived clock frequency of $2^N f_{s2}$ or $2^{N+1} f_{s2}$ for edge-aligned and center-aligned N-bit DPWM, respectively [21]. The power and THD tradeoff between counter and delay-line-based DPWMs for class-D amplifiers is well covered in the literature [22].

B. DC–DC Converter Load Prediction for Efficiency Optimization

The single-channel class-D amplifier architecture with predictive efficiency optimization used in this work is shown in Fig. 4.

The system includes a custom audio digital signal processor (DSP) integrated circuit (IC), a counter-based DPWM, a full-bridge differential power-stage, and two LC reconstruction filters. The PCM audio data is processed by the specialized DSP IC that includes a PLL, a finite-impulse response (FIR) $8\times$ interpolator, and a $\Delta\Sigma$ modulator. The audio stream is also fed to the digital load current predictor and segment controller, as explained in the following section. The audio stream data $s[m]$ is converted into a differential speaker voltage $v_{\text{spk}}(t)$ by the class-D amplifier. Assuming that the speaker load can be approximated with a linear impedance $Z_{\text{spk}}(j\omega)$, then the speaker current $i_{\text{spk}}(t)$ can be predicted by feeding $s[m]$ into $Y_{\text{spk}}(z)$, where $Y_{\text{spk}}(z) = 1/Z_{\text{spk}}$ is the discrete-time equivalent of the speaker admittance $Y_{\text{spk}}(j\omega)$. For a sinusoidal speaker voltage $v_{\text{spk}}(t) = V_{\text{spk}} \sin(\omega t)$, the input current to the class-D amplifier is nonlinear with respect to the audio data, since it is proportional to the instantaneous power in the speaker and occurs at 2ω

$$i_{\text{bus}}(t) = \frac{i_{\text{spk}}(t) v_{\text{spk}}(t)}{V_{\text{bus}}\eta} \tag{3}$$

$$= \frac{V_{\text{spk}}^2}{2V_{\text{bus}}\eta|Z_{\text{spk}}(j\omega)|}(\cos\phi - \cos(2\omega t + \phi)) \tag{4}$$

where V_{bus} is the regulated output voltage of the dc–dc converter, ϕ is the phase between $v_{\text{spk}}(t)$ and $i_{\text{spk}}(t)$, $|Z_{\text{spk}}(j\omega)|$ is the magnitude of the speaker impedance, and η is the class-D amplifier efficiency. The resulting load prediction process is shown in Fig. 5(a).

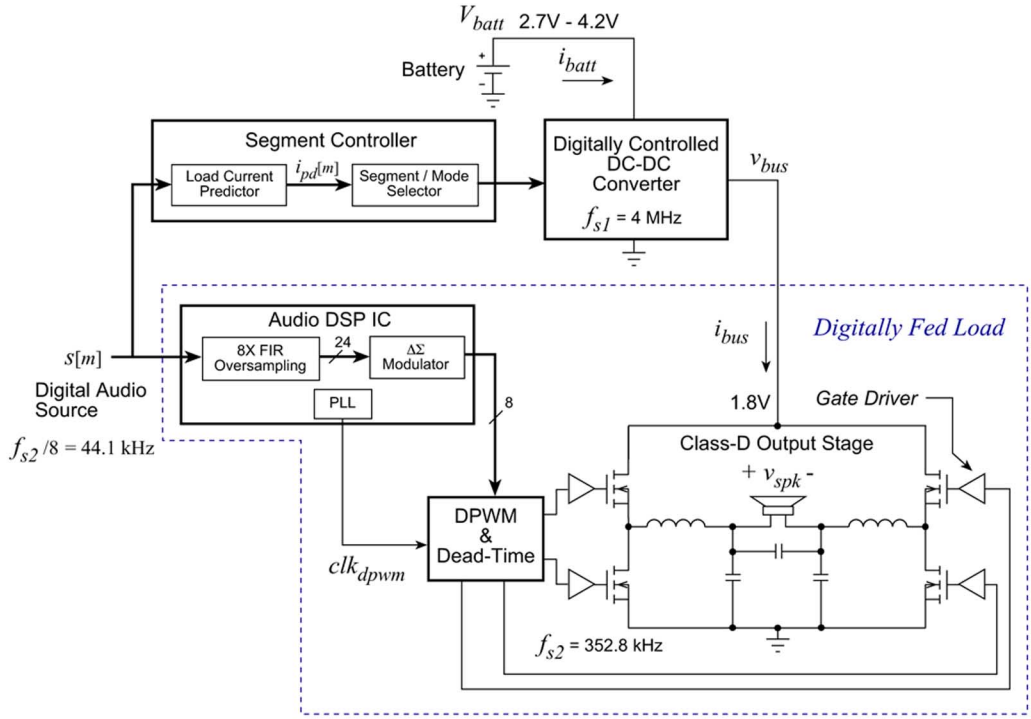


Fig. 4. Simplified diagram of the dc–dc powered class-D audio amplifier system. A sensorless digital current predictor is used to dynamically optimize the power-stage sizing and switch between PFM/PWM based on the digital audio stream.

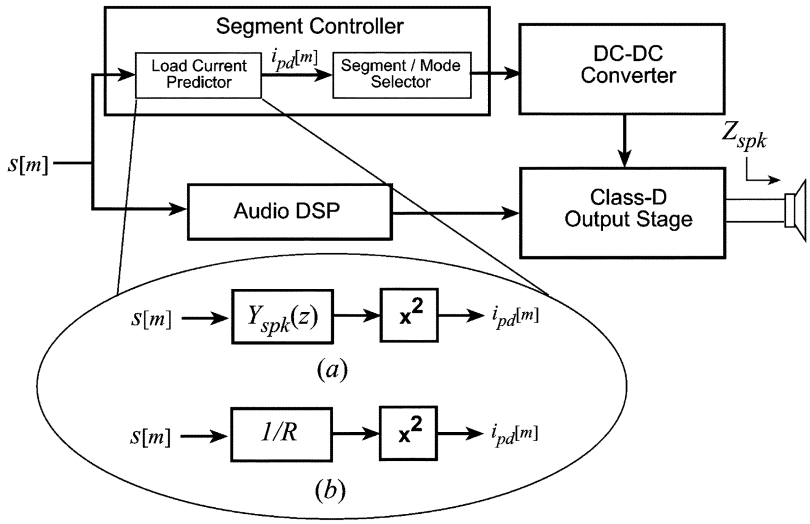


Fig. 5. Load prediction implementation when the speaker is modeled as (a) a general admittance $Y_{\rm spk}(z)$ and (b) a resistor.

The technique of Fig. 5(a) presents some obvious challenges and limitations. In general, the impedance of audio speakers varies greatly between different manufacturers due to the electromechanical nature of the system. The uncertainty in the speaker impedance $Z_{\rm spk}$ implies that dedicated network analyzer hardware would be required within the load-current predictor to extract $Z_{\rm spk}$. Alternatively, the impedance data for different speakers could be prestored in large lookup tables. Both of these approaches are feasible in applications where the processed power exceeds tens of watts, but not in very low power SMPS ($\leq$ 5 W) considered in this work. Second, even if the speaker impedance can be characterized, the additional digital hardware required to implement the $Y_{\rm spk}(z)$ digital filter/emulator may outweigh the benefits of the efficiency optimization; therefore, a simplified approach is employed in this work.

As described in Section IV-A, it was found that even a crude resistive approximation of $Y(j\omega) \approx 1/R$ can lead to a reasonably accurate prediction of the dc–dc converter load current $i_{\rm bus}(t)$. In this case, (3) is simplified to

$$i_{\rm bus}(t) = \frac{v_{\rm spk}^2(t)}{V_{\rm bus}\eta R} = \frac{V_{\rm spk}^2}{2V_{\rm bus}\eta R}(1-\cos(2\omega t)) \propto v_{\rm spk}^2(t). \quad (5)$$

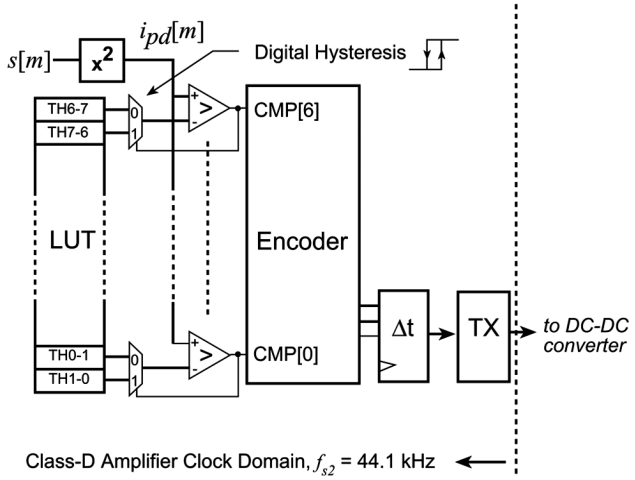


Fig. 6. Segment controller and digitally controlled dc–dc converter communicate using an asynchronous interface.

1) Load Predictor and Segmented Power-Stage: The block diagram of the segment/mode controller and digitally controlled dc–dc converter used in this work are shown in Figs. 6 and 7, respectively. In accordance with the guidelines provided in the following section, to obtain a good optimization between the gate-drive and conduction losses, the pMOS and nMOS power transistors are each segmented into seven identical cells, whose gate-drive inputs are connected in a binary weighted fashion to achieve 3-b of control. This results in 49 possible power-stage configurations in synchronous PWM mode, since the pMOS and nMOS can be controlled independently and at least one segment segment must be *on*.

The segment/mode controller is clocked at the audio sampling rate of $f_{s2}/8 = 44.1$ kHz and thus consumes very low dynamic power, despite the need for a hardware-based multiplier. The eight most significant bits of the audio signal $s[m]$ are first squared, truncated, and then fed to an array of digital comparators to generate the thermometer code [23] signal CMP[6:0]. A 2-to-1 multiplexer is used with each comparator to implement hysteresis in the segment-selection process. An area-efficient lookup table (LUT) stores the thresholds, based on the efficiency measurements presented in Fig. 17. The output of the comparators is encoded into the 3-b segment enable codes $enP$and enN. The combination of $enP = enN = 0$ is used to encode the PFM operating mode, where the synchronous rectifier is disabled. Finally, the data is sent asynchronously to the dc–dc converter, allowing a flexible selection of f_{s1}, irrespective of f_{s2}. In general, it is desirable to synchronize the dc–dc converter clock to the class-D amplifier clock to reduce the ripple on the $V_{\rm bus}$ capacitor; however, this might not be practical in multichip solutions where the high frequency clocks should remain on-chip to minimize noise. Using the flexible approach of Fig. 4, the optimal segment-code is computed every audio sample at $f_{s2}/8 = 44.1$ kHz. A programmable delay buffer is used to account for the average inherent latency of the class-D audio signal path.

The dc–dc controller includes a self-oscillating hybrid delay-line-based DPWM [15], a digital compensator, a windowed analog-to-digital converter (ADC), a dead-time circuit, and a PFM regulator. The 3-b gating pulses for the power-stage are generated within the dead-time block based on the received enable codes. The internal enable codes are updated on the falling edge of the DPWM signal to avoid glitches.

III. Segmented Power-Stage: Optimizing Mid-Load Efficiency

The power MOSFETs in switched-mode power supplies are usually sized to achieve the target peak efficiency and current handling at maximum load, resulting in suboptimal efficiency at other operating points. While at very light loads, the efficiency can be significantly improved by operating in PFM mode, PFM is not effective at light-to-mid loads. In this medium current range, the high peak-current in the power transistors increases the conduction losses, and the resulting dependence of the switching-frequency on the load current can cause EMI problems in sensitive audio applications.

In constant-frequency PWM operation, the main source of losses is the MOSFET's fixed product of the gate capacitance and on-resistance $Q_{\rm gate}R_{\rm on}$, imposed by the process technology. This can be overcome by varying the power-stage MOSFET's effective width-to-length ratio W/L on-the-fly, according to the estimated load-current [5], [6]. A dual-width power-stage was first proposed by [16], and further developed in [5], [6], and [24].

The basic principle of the transistor size optimization and tradeoffs between conduction, gate drive, and hard-switching losses can be described through the following approximate equations. The total conduction losses in the buck converter and power-stage can be easily derived from the dc-model [25] and are given by

$$P_{\rm cond} = P_{\rm cond-DC} + P_{\rm cond-AC} \tag{6}$$

$$P_{\rm cond-DC} = I_{\rm out}^2(DR_{{\rm on},P} + D'R_{{\rm on},N}) \tag{7}$$

$$P_{\rm cond-AC} = \frac{\Delta i_L^2}{12}(DR_{{\rm on},P} + D'R_{{\rm on},N}) \tag{8}$$

where $I_{\rm out}$ is the converter output current, D is the steady-state duty ratio, $D' = 1-D$, Δi_L is the peak-to-peak inductor current ripple, and $R_{{\rm on},P} \propto 1/(W/L)_P$ and $R_{{\rm on},N} \propto 1/(W/L)_N$ are the pMOS and nMOS on-resistance, respectively. The gate-drive losses are given by [8]

$$P_{\rm gate} = f_s(C_{{\rm gate},N}V_{gs,N}^2 + C_{{\rm gate},P}V_{sg,P}^2) \tag{9}$$

where $C_{{\rm gate},P} \propto (W/L)_P$ and $C_{{\rm gate},N} \propto (W/L)_N$ [6] are the pMOS and nMOS lumped capacitance associated with charging and discharging the MOSFET gates, including the relevant transistors within the gate-drivers. Unlike the gate-drive losses, the converter hard-switching losses do not scale linearly with $W_{\rm eff}$. This is due to the fact that the transistor's parasitic capacitances are present at the switching node $v_x(t)$ (see Fig. 7) regardless of whether or not the transistor is enabled. As a result, the rise and fall-times of the switching node are increased as $W_{\rm eff}$ is reduced. By combining the previous three equations, an approximate derivation in [6] leads to an optimal effective transistor width $W_{\rm eff,opt} \leq W_{\rm total}$ given by

$$W_{\rm eff,opt} \propto \frac{P_{\rm out}}{\sqrt{f_s}} \tag{10}$$

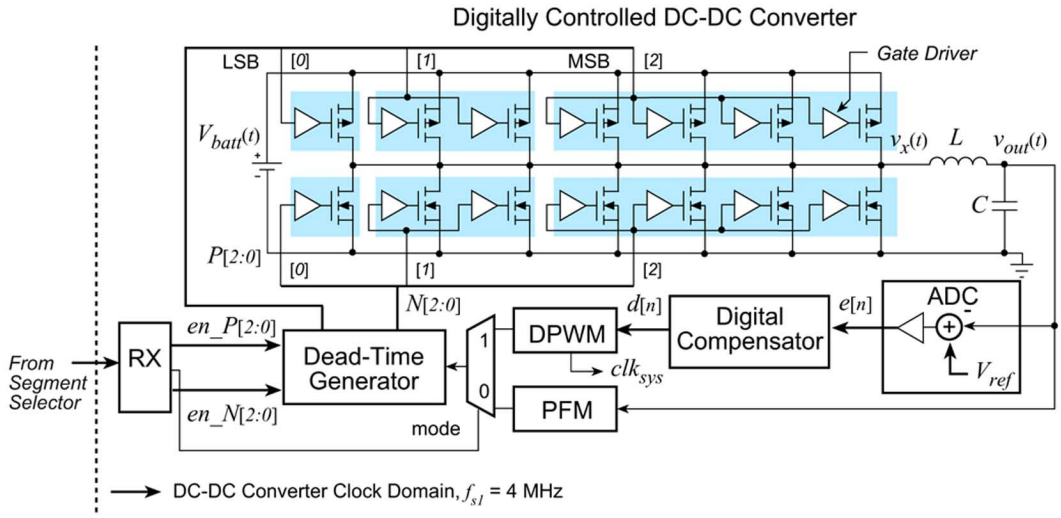


Fig. 7. Digitally controlled dc–dc controller architecture.

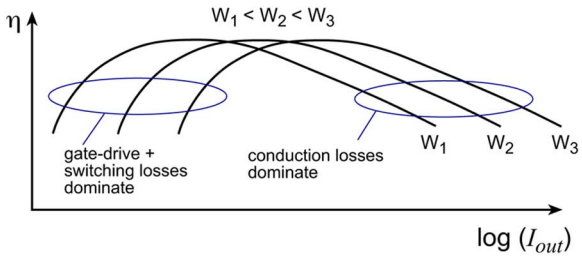


Fig. 8. Efficiency curves for increasing power-stage transistor size.

where P_{out} is the output power of the dc–dc converter. The exact relationship is difficult to predict due to a number of high-order effects and therefore, in most cases, must be determined experimentally. The tradeoff between the gate-drive losses and conduction losses can thus be continuously optimized over a wide load-range while maintaining fixed-frequency operation as illustrated in Fig. 8.

IV. Implementation and Experimental Results

The system shown in Figs. 4 and 7 was implemented using a combination of off-the-shelf and custom designed components, including two low-cost field programmable gate arrays (FPGAs) and two custom fabricated ICs; the segmented power-stage and the class-D audio processor DSP of Fig. 4. A CD player having an optical output was used as the digital audio source for the digital class-D amplifier prototype.

A. Current Prediction

Two miniature 8 Ω speakers (GC0251K and GC0351K) [26] with a 1-W nominal power-handling capibility were used in the prototype. Their measured impedance is given in Fig. 9. The GC0251K and GC0351K are designed to operate up to 20 and 11 kHz, respectively, and have a measured resonant frequency of 950 and 400 Hz, respectively. It can be seen that, in both cases, the magnitude of the impedance remains well within ±13% of the nominal 8 Ω over the specified frequency operating range,

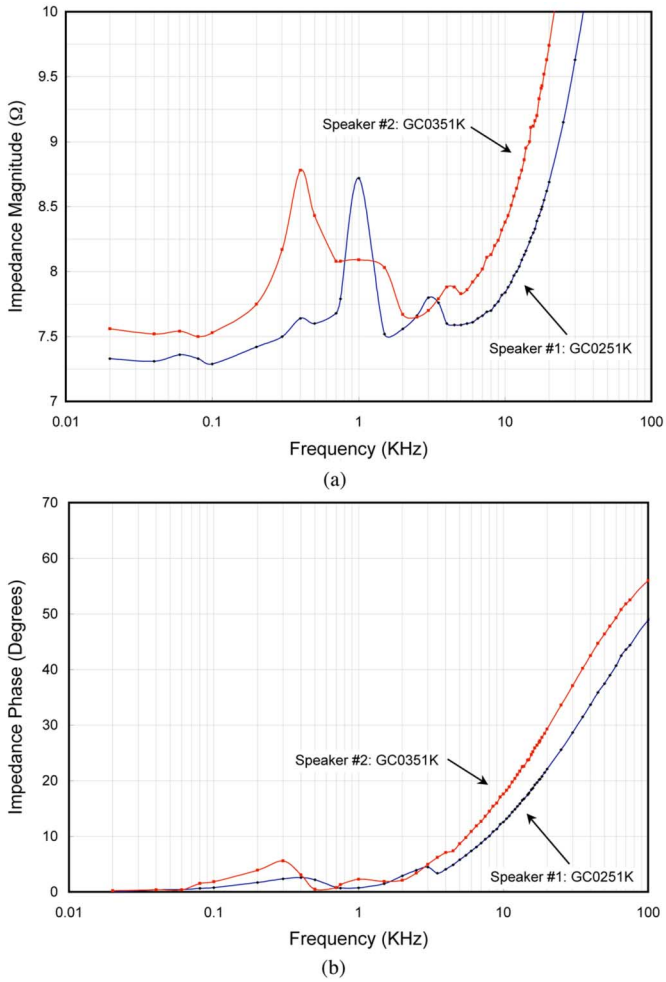


Fig. 9. Measured (a) magnitude and (b) phase of the speaker impedance.

giving a fairly good justification for using the resistive approximation. Furthermore, we can rely on the fact that the power in typical audio signals is generally concentrated in the low-frequency range (below several kHz), following what is referred to as a pink spectrum [27]. The power density of a pink noise

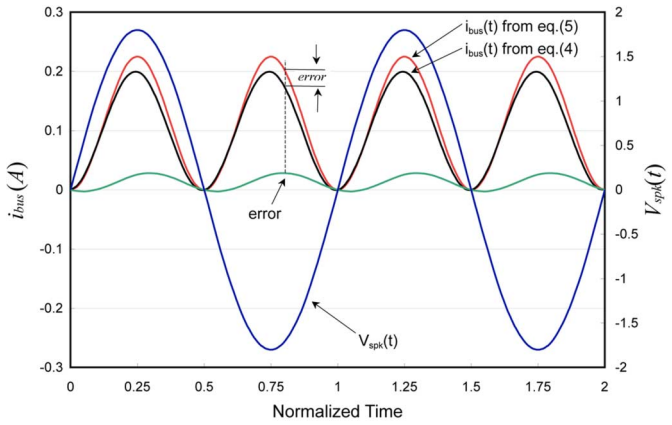


Fig. 10. Illustration of the error in the bus current estimation arising from the approximation $Y(j\omega) \approx 1/R$.

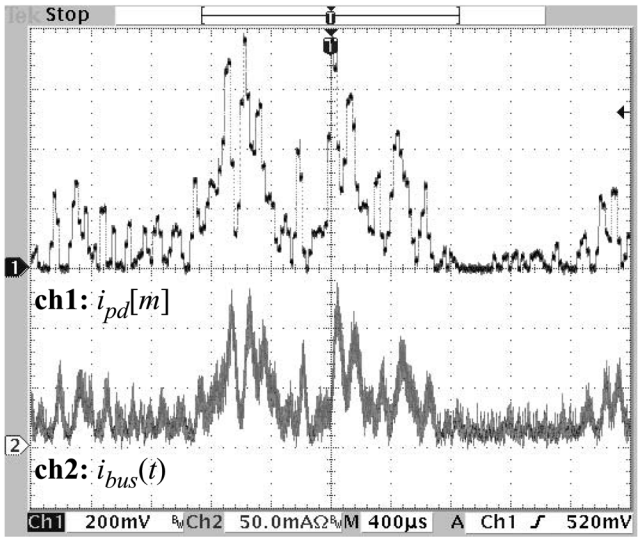


Fig. 11. Predicted and actual dc–dc converter load current with a speaker load. The predicted current $i_{\rm pd}[n]$ is shown using an 8-b flash D/A. Ch-1: $i_{\rm pd}[m]$, 200 mV/div; Ch-2: $i_{\rm bus}(t)$, 50 mA/div.

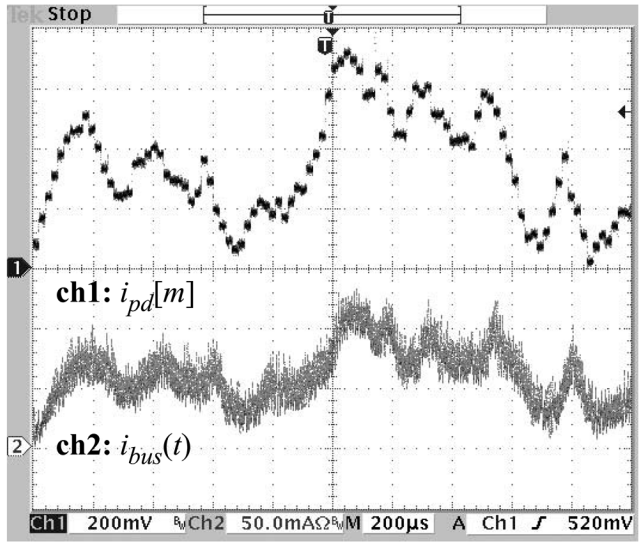


Fig. 12. Predicted and actual dc–dc converter load current with a speaker load. Ch-1: $i_{\rm pd}[m]$, 200 mV/div; Ch-2: $i_{\rm bus}(t)$, 50 mA/div.

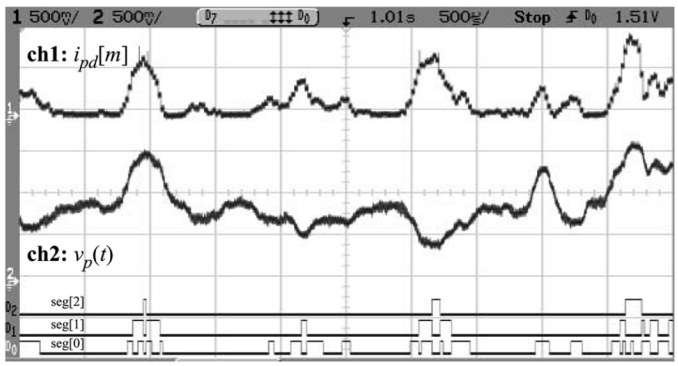


Fig. 13. Predicted dc–dc load current, speaker terminal voltage, and segment enable codes during audio playback. A segment-code of $\rm seg = 0$ indicates that the converter operates in PFM mode. Ch-1: $i_{\rm pd}[n]$, 500 mV/div; Ch-2: $v_p(t)$, 500 mV/div.

decreases by 3 dB per octave compared to white noise [27]. In general, the human ear has reduced sensitivity at low frequencies, and therefore requires a higher acoustic power to achieve equal perceived loudness [28]. In practical terms, this means that the amplitude of the speaker's current at the lower frequencies is several orders of magnitude larger than at higher frequencies. Hence, the relatively large phase-shift at higher frequencies has a negligible effect on the current estimation accuracy. The phase of the speaker impedance within the dominant energy carrying band is below 5° for both speakers.

In order to quantify the accuracy of the estimation method, we can use the worst case analysis for the low-frequency components. The error in the estimation of $i_{\rm pd}[m]$ that arises from the resistive approximation $Y(j\omega) \approx 1/R$ can be estimated by subtracting the two expressions for $i_{\rm bus}(t)$, (5) and (3) for a given worst case phase $\phi \neq 0$ and magnitude $|Z_{\rm spk}(j\omega)| \neq R$ of the measured speaker impedance. The result is shown in Fig. 10 for a single tone and $|Z_{\rm spk}(j\omega)| = 8\ \Omega + 13\%$ and $\phi = 5°$. The maximum error under these conditions is shown in Fig. 10 and corresponds to 16% of the actual current $i_{\rm bus}(t)$, which is fully tolerable for the power-stage used in this prototype.

The output of the digital current predictor block $i_{\rm pd}[n]$ is shown in Figs. 11 and 12, along with the actual dc–dc converter load current $i_{\rm bus}(t)$. An 8-b flash digital-to-analog converter was used to display $i_{\rm pd}[n]$ on an oscilloscope for convenience. It can be seen that a good matching between $i_{\rm pd}[n]$ and $i_{\rm bus}(t)$ is achieved, despite the complex impedance of the speaker. Slight phase and amplitude errors in $i_{\rm pd}[n]$ are inevitable due to simplified load prediction technique. These phase errors result in the temporary selection of the nonoptimal segment-code but the overall energy is still significantly reduced, as shown in Section IV-C.

The dynamic operation of the segment controller during audio playback is shown in Fig. 13. The converter remains in PFM mode for $\rm seg[2:0] = 0$. The segment-codes clearly follow the changes in $i_{\rm pd}[n]$. The automatic PWM-to-PFM transition is shown in Fig. 14 during audio playback. The opposite transition is shown in Fig. 15.

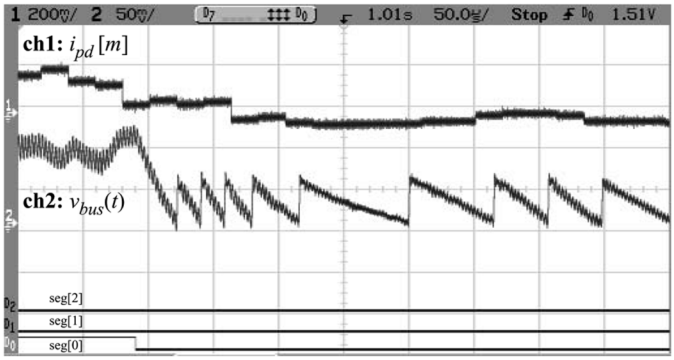


Fig. 14. Predicted dc–dc load-current and regulated output voltage during a transition from PWM to PFM mode. The load-current varies continuously during audio playback; hence, this does not correspond to a traditional load step response. Ch-1: $i_{\rm pd}[n]$, 200 mV/div; Ch-2 (ac-coupled): $v_{\rm bus}(t)$, 50 mV/div.

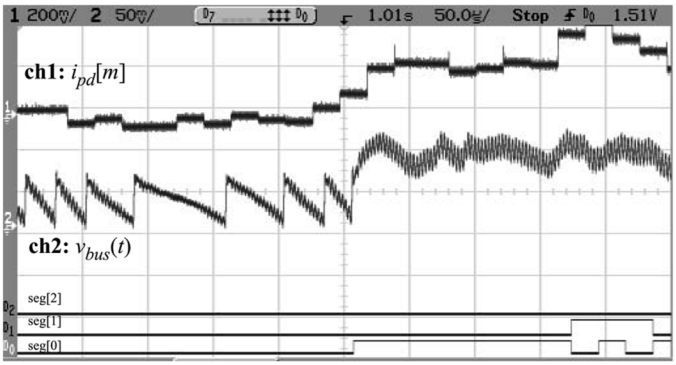


Fig. 15. Predicted dc–dc load-current and regulated output voltage during a transition from PFM to PWM mode.Ch-1: $i_{\rm pd}[n]$, 200 mV/div; Ch-2 (ac-coupled): $v_{\rm bus}(t)$, 50 mV/div.

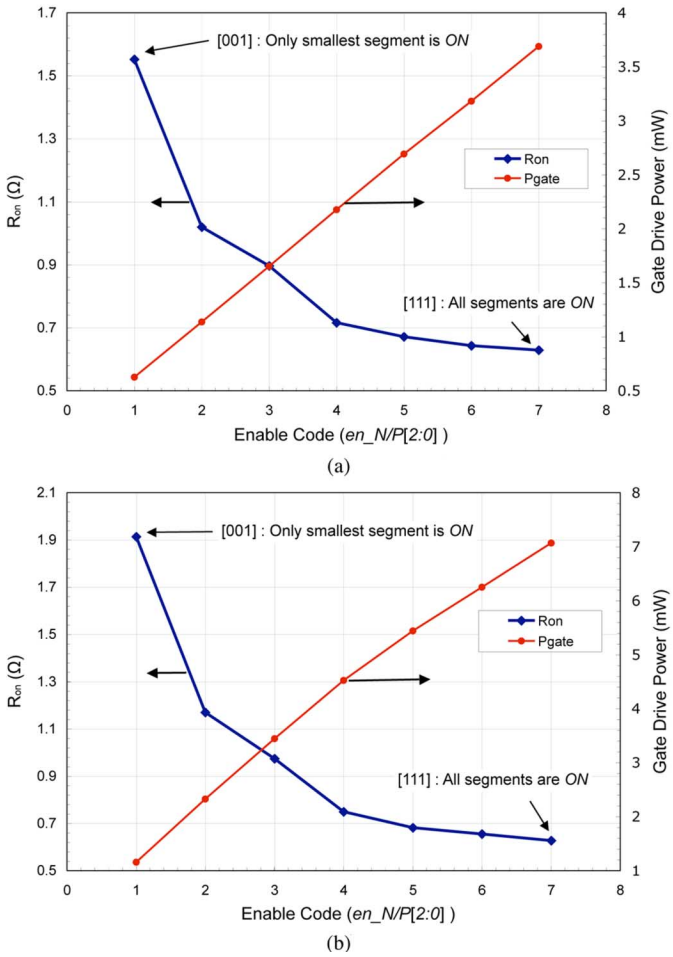


Fig. 16. Measured $R_{\rm on}$ and $P_{\rm gate}$ at $f_s = 4$ MHz and $V_{\rm batt} = 3.6$ V for the (a) nMOS and (b) pMOS power transistors.

B. Segmented Power-Stage IC

An IC having on-chip gate-drivers and complimentary segmented output-stage transistors was fabricated in a 0.6-μm CMOS process technology [5]. The output-stage consists of high-side pMOS and low-side nMOS power transistors divided into seven segments, which are driven by dedicated gate-drivers, as shown in Fig. 7. The total active area of the power transistors is not affected by the segmentation, since the drain and source terminals are common to all segments. The measured $R_{\rm on}$ and gate-drive power consumption $P_{\rm gate}$ versus the segment enable code are given in Fig. 16(a) and (b) for the nMOS and pMOS, respectively. The distributed nature of the segmented gate-drivers and close proximity to each segment greatly reduces the gate voltage rise/fall times compared to a single lumped gate-driver.

The resulting efficiency curves at $f_{s1} = 4$ MHz and $V_{\rm batt} = 3.6$ V for several segment enable codes including PFM are shown in Fig. 17. This plots confirms the obvious advantage of operating with variable effective size, for both and nMOS and the pMOS.

The chip micrograph of the fabricated power-stage IC is shown in Fig. 18, while the custom chip-size-module (CSM) package [5] used in this work is shown in Fig. 19. The CSM measures only 2.4 mm $\times$ 2.95 mm $\times$ 1 mm and includes a

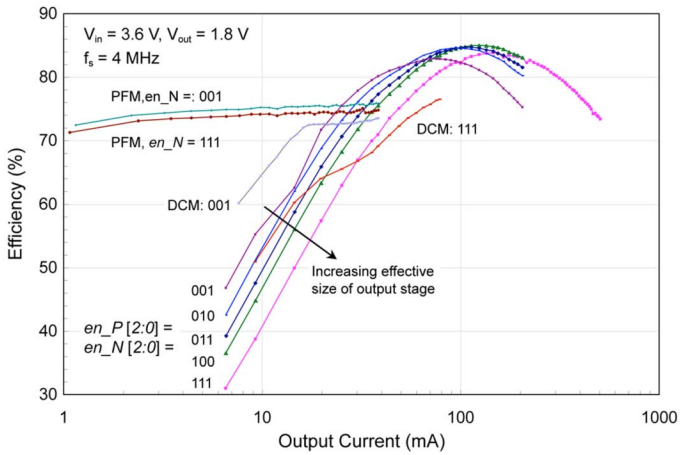


Fig. 17. Measured efficiency versus load with different segment enable codes and modes of operation for the power-stage IC.

miniature 2-μH inductor fabricated in a ferrite core [5]. The resulting performance of the power-stage IC is summarized in Table I. Three figures of merit (FOM) are used to characterize the power-stage IC. The first, $\rm FOM_1$, is given by

$$\rm FOM_1 = Q_{gate} \cdot R_{ch} \tag{11}$$

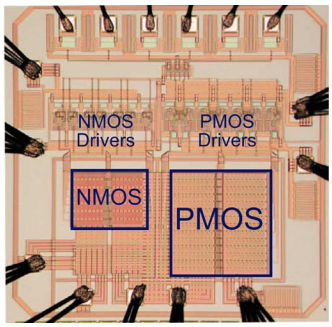


Fig. 18. Chip micrograph for the segmented power-stage IC.

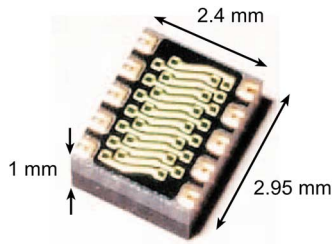


Fig. 19. Custom chip-size-module (CSM) package that includes the micro inductor from Fuji Electric Advanced Technology Company, Ltd.

TABLE I
SUMMARY OF RESULTS OF THE SEGMENTED POWER-STAGE IC

	Output Stage IC		Units	Condition
	pMOS	nMOS		(V_{batt} = 3.6 V)
CMOS Process	0.6 μm			
Total W	107.6	39.2	mm	
Drawn Length L	0.6	0.6	μm	
Active Area A	0.370	0.145	mm^2	
R_{ch}	202	129	mΩ	Simulated
Q_{gate}	655	250	pC	Simulated I_D = 500 mA
FOM$_1$	132.3	32.25	nC·mΩ	$Q_{gate} \cdot R_{ch}$
R_{on}	626	629	mΩ	Meas. inc. pkg
P_{gate}	7.07	3.68	mW	Measured f_s = 4 MHz
FOM$_2$	231.6	91.2	mΩ mm^2	Meas. inc. pkg
FOM$_3$	1.106	0.579	pJ·mΩ	$\frac{P_{gate}}{f_s} \cdot R_{on}$
Peak Efficiency	85.0		%	V_{batt} = 3.6 V V_{out} = 1.8 V
Peak Efficiency	88.8		%	V_{batt} = 2.7 V V_{out} = 1.8 V

where FOM$_1$ is based on the simulated prelayout gate-charge $Q_{\rm gate}$ and intrinsic MOSFET on-resistance $R_{\rm ch}$, based on HSPICE simulations. FOM$_1$ provides a direct performance measure of the process technology regardless of the packaging or layout structure. The remaining figures-of-merit FOM$_2$ and FOM$_3$, given by (12) and (13), respectively, are based on the measured device performance

$$\text{FOM}_2 = R_{\rm on} \cdot A \tag{12}$$

$$\text{FOM}_3 = \frac{P_{\rm gate}}{f_s} R_{\rm on}. \tag{13}$$

FOM$_2$ is the specific on-resistance of the device after packaging. The gate-driver energy ($P_{\rm gate}/f_s$) is used in FOM$_3$ since the gate charge cannot be measured directly due to the segmented power-stage and limited pin count. The achieved specific on-resistance of $R_{\rm on,sp} = 91.2$ mΩ mm^2 is limited by the use of standard thick-oxide I/O transistors and could be further reduced by using optimized LDMOS structures available in more expensive processes [29]. A peak efficiency of 88.8% is achieved at $V_{\rm batt} = 2.7$ V. The peak efficiency is mainly limited by the embedded inductor's conduction losses [5] and the high switching losses in the hard-switching power-stage at $f_s = 4$ MHz. The efficiency could be further improved by incorporating an automatic dead-time control scheme [2] to achieve zero voltage switching (ZVS). An optimized segmented power-stage IC with greatly improved figures-of-merit is described in [30].

TABLE II
TOTAL ENERGY CONSUMPTION WITH AND WITHOUT AUTOMATIC SEGMENT/MODE CONTROL

Song Type	Length (s)	Total Samples ($\times 10^6$)	Total Energy (J)		**Savings** (%)
			All ON	Automatic Control	
1. Rock	149	6.57	11.16	8.80	**21.2**
2. Classical	380	16.8	23.77	17.18	**27.7**
3. Jazz	140	6.17	7.08	4.36	**38.3**

C. Energy Savings

The total energy flowing into the dc–dc converter was measured for three varieties of music pieces, in order to quantify the effectiveness of the segment/mode control scheme. The results are given in Table II. Despite the accuracy limitations of the load-current estimation, the total energy was reduced by a maximum of 38% when compared to operating as conventional systems, without PFM mode and with all segments ON. The experimental results prove the merit of this sensorless efficiency optimization technique. In a separate test, PFM mode was disabled and energy savings of up to 20% were observed when only the segment control was activated. Similar power savings can be expected with other loads present in handheld devices, such as displays. The statistical distribution of the instantaneous power resulting from each audio sample is given in Fig. 20(a) for the three songs. Each audio sample was squared and placed into a power bin according to the resulting eight MSBs. From this distribution it is clear that vast majority of the audio samples are concentrated in the low power bins, especially for the Classical song. This further explains why improving the light-load efficiency has a significant impact on the total energy consumption.

The distribution of selected segment enable-codes was computed based on the thresholds that were programmed in the segment selector of Fig. 6. The result is shown in Fig. 20(b) for the audio sample listed as song 1 in Table II. Based on the current thresholds extrapolated from the efficiency characterization of Fig. 17, the converter seldom operates with all segments on, which explains the energy reduction observed in Table II. In general, it can be concluded that while the power-stage must be sized to deliver the desired peak power, it is more efficient to operate with a smaller effective W/L ratio during most of the audio playback. Clearly, the achievable energy reduction varies on a number of factors including the dc–dc converter power-stage sizing, the energy distribution of the audio sample, and the playback volume.

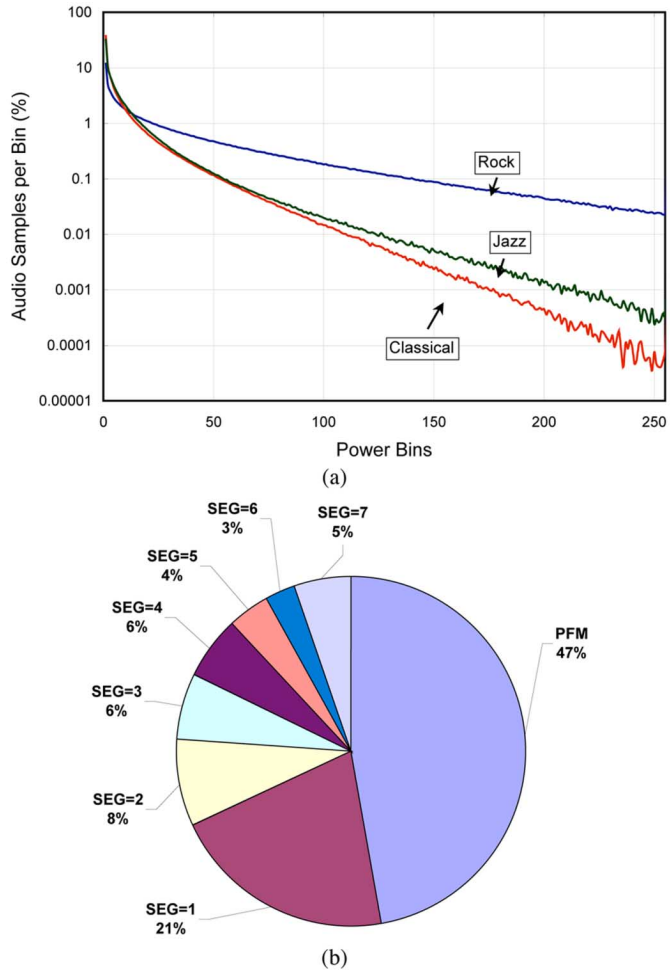


Fig. 20. (a) Statistical power distribution for the three songs listed in Table II. (b) Percentage of audio samples of song 1 falling into each segment enable code.

V. Conclusion

A novel efficiency optimization technique and system, based on a real-time prediction of the load current of dc–dc converters are introduced. The technique is suitable for on-chip implementation in advanced digital processes and is mainly designed for modern dynamic electronic loads, whose power depends on the real-time processed digital data stream. In this paper, the current is estimated from the digital stream by using a digital predictor that emulates the admittance of the supplied system. The results of the prediction are then used to dynamically adjust the effective size of the power-stage transistors and/or switch to pulse-frequency mode of output voltage regulation. As a result, at each operating point, the instantaneous efficiency of the power-stage is maximized. The effectiveness of the method is demonstrated on a 1-W, 4-MHz digitally controlled buck prototype. As an application example, a digitally fed class-D amplifier and miniature speaker are used. The experimental results confirm that significant energy savings of up to 38% can be achieved, compared to that of conventional nonoptimized systems.

References

[1] B. Acker, C. Sullivan, and S. Sanders, "Synchronous rectification with adaptive timing control," in *Proc. IEEE Power Electron. Specialists Conf.*, 1995, vol. 1, pp. 88–95.

[2] O. Trescases, S. Chen, and W.-T. Ng, "Precision gate drive timing in a zero-voltage-switching dc–dc converter," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs*, May 2004, pp. 55–58.

[3] W. Lau and S. Sanders, "An integrated controller for a high frequency buck converter," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 1997, vol. 1, pp. 246–254.

[4] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead-times in dc–dc converters with synchronous rectifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2005, pp. 911–917.

[5] O. Trescases, W.-T. Ng, H. Nishio, E. Masaharum, and T. Kawashima, "A digitally controlled dc–dc converter module with a segmented output stage for optimized efficiency," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs*, 2006, pp. 409–413.

[6] S. Musuniri and P. Chapman, "Improvement of light load efficiency using width-switching scheme for CMOS transistors," *Power Electron. Lett.*, vol. 3, no. 3, pp. 105–110, 2005.

[7] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electronics Specialists Conf.*, 1991, pp. 527–532.

[8] M. Mulligan, B. Broach, and T. Lee, "A constant frequency method for improving light-load efficiency in synchronous buck converters," *Power Electron. Lett.*, vol. 3, no. 1, pp. 24–29, Mar. 2005.

[9] Y. Chen, F. Lee, L. Amoroso, and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.

[10] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4-μA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[11] A. Prodić and D. Maksimović, "Digital PWM controller and current estimator for a low-power switching converter," in *IEEE Comput. Power Electron. 2000*, 2000, pp. 123–128.

[12] W. Schultz, Motorola, "Lossless current sensing with SENSEFETs enhances the motor drive," Tech. Rep., 1988.

[13] S. Yuvarajan, "Performance analysis and signal processing in a current sensing MOSFET (SENSEFET)," in *Proc. Ind. Applicat. Soc. Annu. Meeting*, 1990, vol. 2, pp. 1445–1450.

[14] A. V. Peterchev and S. Sanders, "Digital loss-minimization multi-mode synchronous buck converter control," in *Proc. IEEE Power Electron. Specialists Conf.*, Jul. 2004, pp. 3694–3699.

[15] D. Maksimović, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, May 2004, pp. 13–22.

[16] R. Williams, W. Grabowski, A. Cowell, M. Darwish, and J. Berwick, "The dual-gate W-switched power MOSFET: A new concept for improving light load efficiency in dc–dc converters," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 1997, pp. 193–196.

[17] J. Varona, A. Hamoui, and K. Martin, "A low-voltage fully-monolithic delta sigma based class-D audio amplifier," in *Proc. IEEE Eur. Solid-Solid Circuits Conf.*, 2003, pp. 545–548.

[18] P. Midya, B. Roeckner, and S. Bergstedt, "Digital correction of PWM switching amplifiers," *Power Electron. Lett.*, vol. 2, no. 2, pp. 68–72, 2004.

[19] A. Dancy and A. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 1997, pp. 21–27.

[20] O. Trescases, G. Wei, and W.-T. Ng, "A segmented digital pulsewidth modulator with self-calibration for low-power SMPS," in *Proc. EDSSC'05*, Hong Kong, Dec. 2005, pp. 367–370.

[21] C. Neesgaard, R. Antley, C. Kaya, K. Mochizuki, F. Nyboe, L. Risbo, D. Skelton, S. Unnikrishnan, and A. Zhao, "Class D digital power amp (purepath digital) high Q musical content," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 97–100.

[22] B. Gwee, J. Chang, and H. Li, "A micropower low-distortion digital pulsewidth modulator for a digital class D amplifier," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 4, pp. 245–256, Apr. 2002.

[23] D. Johns and K. Martin, *Analog Integrated Circuit Design.*. New York: Wiley, 1997.

[24] D. Guckenberger and K. Kornegay, "Integrated dc–dc converter design for improved WCDMA power amplifier efficiency in SiGe BiCMOS technology," in *Proc. IEEE ISLPED*, 2003, pp. 449–454.

[25] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[26] "GC0251K specifications," Cui, Inc., 2003 [Online]. Available: http://www.cui.com

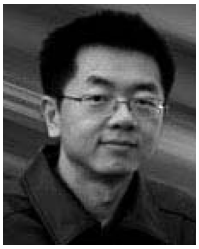
[27] W. Yost and D. Nielsen, *Fundamentals of Hearing: An Introduction*. New York: Academic, 1994.

[28] D. Robinson, "A new determination of the equal-loudness contours," *IRE Trans. Audio*, vol. 6, no. 1, pp. 6–13, 1958.

[29] S. Pendharkar, R. Pan, T. Tamura, B. Todd, and T. Efland, "7 to 30 V state-of-art power device implementation in 0.25 μm LBC7 BiCMOS-DMOS process technology," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs*, 2004, pp. 419–422.
[30] O. Trescases, "Integrated power-supplies for portable applications," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. of Toronto, Toronto, ON, Canada, 2007.

Olivier Trescases (S'01–M'08) received the B.A.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2002, 2004, and 2007, respectively.

In 2007, he joined the High-Integration Group, Automotive Power Department, Infineon Technologies AG, Villach, Austria. He is responsible for developing dc–dc converters in smart-power technologies for automotive applications, including next-generation airbag systems. His past research interests include high-frequency/high-efficiency SMPS for portable applications, mixed-signal IC design, motor drives, and digital class-D amplifiers.



Guowen Wei (S'04) received the B.A.Sc. degree in engineering science and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2005 and 2007, respectively, and is currently pursuing the Ph.D. degree at the University of California at San Diego, La Jolla, working on high-speed ADC design.

His research interests include analog mixed-signal circuits, integrated class-D audio amplifiers, and smart power management ICs.

Aleksandar Prodić (S'00–M'03) received the Dipl. Ing. degree in electrical engineering from the University of Novi Sad, Novi Sad, Serbia, in 1994 and the M.Sc. and Ph.D. degrees from the Colorado Power Electronics Center, University of Colorado, Boulder, in 2000 and 2003, respectively.

Since 2003, he has been with the University of Toronto, Toronto, ON, Canada, where he is an Assistant Professor with the Department of Electrical and Computer Engineering. In 2004, at the University of Toronto, he established the Laboratory for Low-Power Management and Integrated Switch-Mode Power Supplies. His research interests include digital control of low-power high-frequency SMPS, mixed-signal IC design, DSP techniques for power electronics, and the development of systems-on-chip (SoC) for power management.

Wai Tung Ng (M'90–SM'04) received the B.A.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1983, 1985, and 1990, respectively. His graudate research work was focused on analog integrated circuits design and smart power integrated fabrication processes.

In 1990, he joined the Semiconductor Process and Development Center, Texas Instruments, Inc., Dallas, to work on LDMOS power transistors for automotive applications. His academic career started in 1992 when he joined the Department of Electrical and Electronic Engineering, University of Hong Kong. In 1993, he joined the University of Toronto and was promoted to Associate Professor in 1998. His research interests cover a wide spectrum, ranging from advanced MOS and RF BJT device designs and analog circuits. His recent work includes VLSI power management circuits, integrated dc–dc converters, smart power integrated circuits, and fabrication processes.