Digitally Controlled Current-Mode DC–DC Converter IC

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***Abstract*—The main focus of this paper is the implementation of mixed-signal peak current mode control in low-power dc–dc converters for portable applications. A DAC is used to link the digital voltage loop compensator to the analog peak current mode loop. Conventional DAC architectures, such as flash or $\Delta\Sigma$ are not suitable due to excessive power consumption and limited bandwidth of the reconstruction filter, respectively. The charge-pump based DAC (CP-DAC) used in this work has relatively poor linearity compared to more expensive DAC topologies; however, this can be tolerated since the linearity has a minor effect on the converter dynamics as long as the limit-cycle conditions are met. The CP-DAC has a guaranteed monotonic behavior from the digital current command to the peak inductor current, which is essential for maintaining stability. A buck converter IC, which was fabricated in a 0.18 μm CMOS process with 5 V compatible transistors, achieves a response time of 4 μs at $f_s = 3$ MHz and $V_{\rm out} = 1$ V, for a 200 mA load-step. The active area of the controller is only 0.077 mm^2, and the total controller current-draw, which is heavily dominated by the on-chip senseFET current-sensor, is below 250 μA for a load current of $I_{\rm out} = 50$ mA.**

***Index Terms*—CPM, current-mode, dc–dc converter, digital control, integrated circuits, power management, SMPS, voltage regulators.**

I. Introduction

HIGH-FREQUENCY dc–dc converters are increasingly being integrated into system-on-chip (SoCs) designs, in order to provide one or more tightly regulated supply voltages for various mixed-signal blocks. In most low-power applications, the power conversion efficiency of the converters must be maximized over the full range of operating current. At the same time, the PCB footprint of the LC filter components should be minimized by operating at the highest possible switching frequency, which makes low-power design very challenging.

In sub-1 W applications, the controller power-consumption must be minimized to avoid degrading the overall converter efficiency. A typical experimental efficiency versus load-current curve is shown in Fig. 1. The maximum current draw of the controller operating in PWM mode is also shown for an efficiency degradation ranging from 0.2% to 2%, which is considered acceptable. Below $I_{\rm out} = 150$ mA, the total controller current-consumption is limited to 250 μA for an efficiency degradation of 0.2%, which is very challenging for high-performance, high-frequency controllers.

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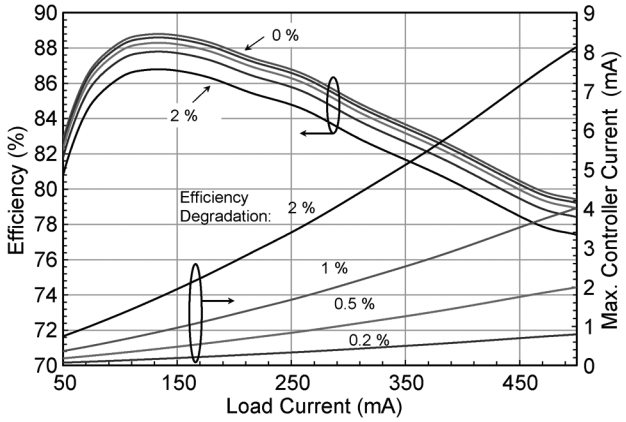

Fig. 1. Efficiency degradation due to controller power consumption.

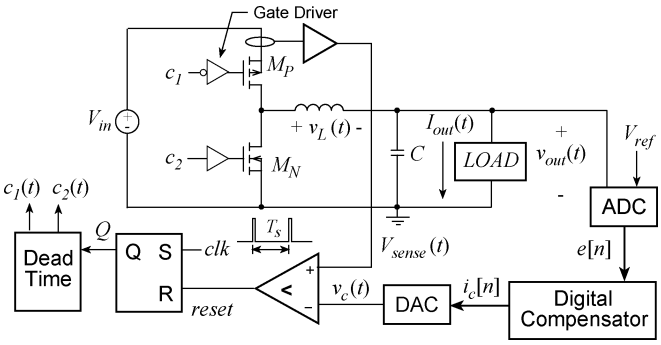

Fig. 2. Synchronous buck converter with mixed-signal current mode control.

Below several hundred MHz, full monolithic integration in CMOS processes is not feasible today, due to size and cost constraints for the passive components [1]. Instead, the system-in-package (SiP) solution is gaining momentum for high-efficiency conversion in the several-to-ten's of MHz range. SiP consists of packaging the die and passives together to reduce the footprint and parasitics [2]. Several dc–dc converters having in-package inductors that use proprietary packaging/integration techniques have been introduced [2]–[4]. Including the inductor in the same package as the die allows further optimization of the efficiency compared to traditional designs, where the inductor characteristics are unknown to the IC manufacturer. This work is targeted to SiP applications in the 2–10 MHz range.

Peak current-mode control (CPM) provides inherent cycle-by-cycle current-limiting in the power transistors and simplified loop dynamics, which allows simple and robust compensation of the control-loop [5] as shown in Fig. 2. Low-power analog integrated CPM buck converters have been reported [6]–[9] with a switching frequency of up to 2.5 MHz [8]. Mixed-signal CPM [10], [11] is a hybrid control scheme, where voltage-loop compensation is carried out in the digital

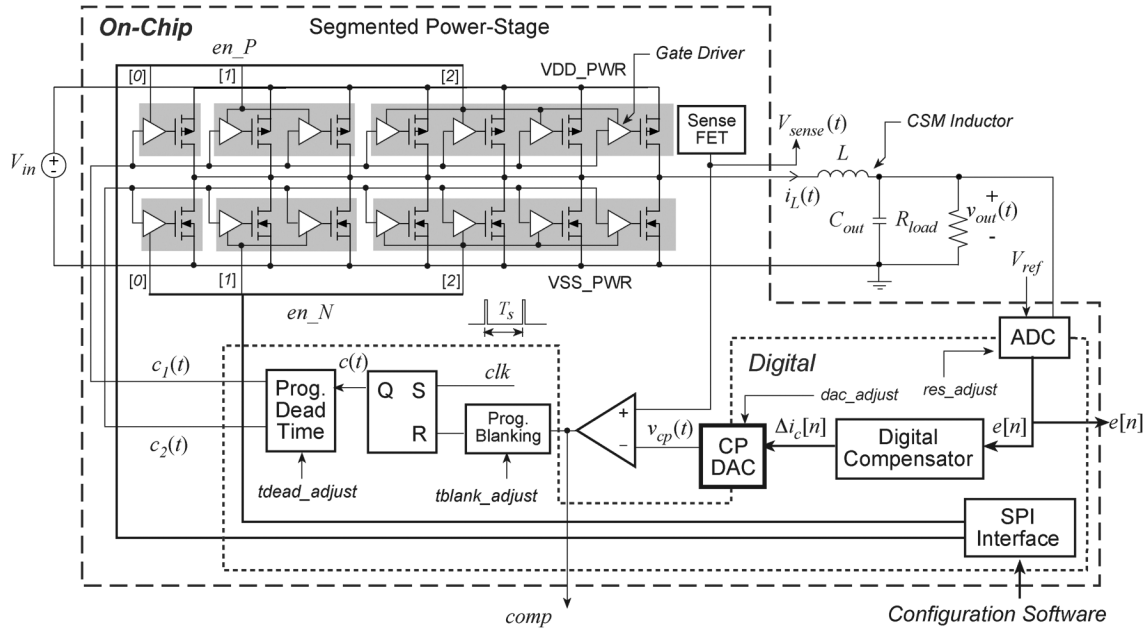

Fig. 3. Simplified architecture of the integrated dc–dc converter with a hybrid CPM control scheme and the novel DAC.

domain, while the current-regulation loop has a traditional analog implementation. Using this architecture, a DAC is required at the interface of the two loops, in order to generate an analog current command. Mixed-signal CPM benefits from the simplicity of the analog current loop and the flexibility of the digitally compensated voltage loop. With this approach, a reconfigurable digital compensator can be used without the need for sampling the inductor current. The high-frequency digital pulse-width modulator (DPWM) required for fully digital CPM schemes [12]–[14] is also eliminated, resulting in a practical, low-cost implementation.

The design of a low-power DAC specialized for mixed-signal CPM is the main focus of this work. A flash architecture is not appropriate due to high power consumption, which limits the light-load efficiency of the buck converter. In [11], a one-bit ($\Delta\Sigma$) DAC was used to meet the tight resolution requirements of mixed-signal CPM; however, the low-pass reconstruction filter in the DAC introduces an undesirable pole in the system transfer function. This pole limits the control bandwidth and overall regulation performance. An adaptive control scheme was developed to address this issue [11], where the DAC over-sampling rate and filter corner frequency of the $\Delta\Sigma$ DAC are varied in real-time to achieve both low steady-state power consumption and fast transient response. In this work, the aim is to eliminate the main shortcomings of the previous $\Delta\Sigma$ DAC approach, namely the bandwidth restriction imposed by the DAC's low-pass filter, while at the same time generating a high resolution voltage reference for the current-loop. The simple low-power DAC architecture is applied to the hybrid scheme for a synchronous buck converter IC, as shown in Fig. 3. The IC includes the control circuits, as well as a segmented power-stage [15] for improving light-load efficiency. Unlike $\Delta\Sigma$ topologies, the proposed DAC does not require extensive digital signal processing (noise shaping) or high-frequency clocks beyond the switching frequency, f_s.

The CP-DAC basic architecture was first reported in [16]. In addition to providing numerous additional implementation details and new measurement results, this paper examines the effect of charge/discharge current mismatch inside the charge-pump on the converter's closed-loop operation and reaches new conclusions about the application range of this topology. This paper also investigates the effect of current source mismatch in the DAC architecture.

This paper is organized as follows. The limit-cycle phenomenon for mixed-signal CPM is analyzed in Section II, leading to minimum resolution requirements for the DAC. The proposed low-power DAC architecture for linking the voltage and current loops is presented in Section III. The high-bandwidth analog current sensing scheme is presented in Section V and experimental results for the fabricated prototype are reported in Section VII.

II. Limit-Cycle Oscillations in Current-Mode Control

Unless otherwise stated, it is assumed that the converter runs in CPM without slope-compensation, which implies that the steady-state duty-cycle is limited to $D < 0.5$, in order to avoid inherent instability in the current loop [5]. Instability in the uncompensated current loop has been shown to appear slightly below $D = 0.5$ [17].

The two quantizers (the DAC and the ADC) in the feedback loop make hybrid CPM prone to limit-cycle oscillations, a phenomenon which is well understood in digital voltage-mode controllers [18], [19]. In this section, the analysis method presented in [18] is extended for the hybrid CPM. The DC output voltage change caused by changing the DAC input by one LSB, $\Delta V_{\rm dac}$, is given by

$$\Delta V_{\rm dac} = \frac{G_{\rm vc}(s=0)}{K_s} \cdot \frac{V_r}{2^M} = \frac{G_{\rm vc0}}{K_s} \cdot \frac{V_r}{2^M} \qquad (1)$$

where M is the DAC resolution, K_s is the current-sensing gain, V_r is the DAC reference voltage, and $G_{\rm vc0}$ is the dc control-to-output gain of the current loop. The dc condition to avoid limit-cycles and the resulting minimum DAC resolution are given by (2) and (3), respectively

$$\Delta V_{\rm dac} = \frac{G_{\rm vc0}}{K_s} \cdot \frac{V_r}{2^M} < \Delta V_{\rm adc} \tag{2}$$

$$M > \left\lceil \log_2 \left(\frac{V_r}{\Delta V_{\rm adc} K_s} \cdot G_{\rm vc0} \right) \right\rceil \tag{3}$$

Without slope compensation, the peak inductor current is ideally equal to the current command $i_c[n]$, which gives

$$I_c = I_{\rm load} + \frac{\Delta i_L}{2} \tag{4}$$

where Δi_L is given by

$$\Delta i_L = \frac{V_{\rm out}\left(1 - \frac{V_{\rm out}}{V_{\rm in}}\right)}{L f_s}. \tag{5}$$

Substituting $I_{\rm load} = v_{\rm out}/R_{\rm load}$ in (4) gives the following quadratic equation:

$$\frac{-1}{2Lf_s V_{\rm in}} V_{\rm out}^2 + \left(\frac{1}{R_{\rm load}} + \frac{1}{2Lf_s} \right) V_{\rm out} - I_c = 0. \tag{6}$$

The current-loop gain $G_{\rm vc0}$ is obtained by solving (6) for $V_{\rm out}$ and differentiating the result with respect to I_c

$$G_{\rm vc0} = \frac{\partial V_{\rm out}}{\partial I_c} = \left(\left(\frac{1}{R_{\rm load}} + \frac{1}{2Lf_s} \right)^2 - \frac{2I_c}{Lf_s V_{\rm in}} \right)^{-\frac{1}{2}}. \tag{7}$$

The highest and worst case gain occurs for $I_{\rm load} = 0$, $R_{\rm load} \to \infty$, and $I_c = \Delta i_L/2$. Eliminating I_c in (7) gives

$$\lim_{R_{\rm load}\to\infty} G_{\rm vc0} = \frac{2Lf_s}{\sqrt{1 - 4\frac{V_{\rm out}}{V_{\rm in}}\left(1 - \frac{V_{\rm out}}{V_{\rm in}}\right)}}. \tag{8}$$

By combining (8) and (3), the worst-case minimum DAC resolution is given by

$$M > \left\lceil \log_2 \left(\frac{V_r}{\Delta V_{\rm adc} K_s} \cdot \frac{2Lf_s}{\sqrt{1 - 4\frac{V_{\rm out}}{V_{\rm in}}\left(1 - \frac{V_{\rm out}}{V_{\rm in}}\right)}} \right) \right\rceil. \tag{9}$$

If slope compensation is used, (4) becomes

$$I_c = I_{\rm load} + \frac{\Delta i_L}{2} + m_a D T_s \tag{10}$$

where m_a is the slope of the compensation ramp. This leads to the following modified expression for the gain $G_{\rm vc0}$:

$$G_{\rm vc0} = \left(\left(\frac{1}{R_{\rm load}} + \frac{1}{2Lf_s} + \frac{m_a}{V_{\rm out} f_s} \right)^2 - \frac{2I_c}{Lf_s V_{\rm in}} \right)^{-\frac{1}{2}}. \tag{11}$$

The output voltage versus current command, obtained from solving (6), is shown in Fig. 4(a) for different values of $R_{\rm load}$ and for the parameters given in Table I. The current-loop gain from (7) is plotted in Fig. 4(b). In both cases, the duty-cycle limit of $D = 0.5$ is shown by the dashed line, beyond which the current loop is inherently unstable [5].

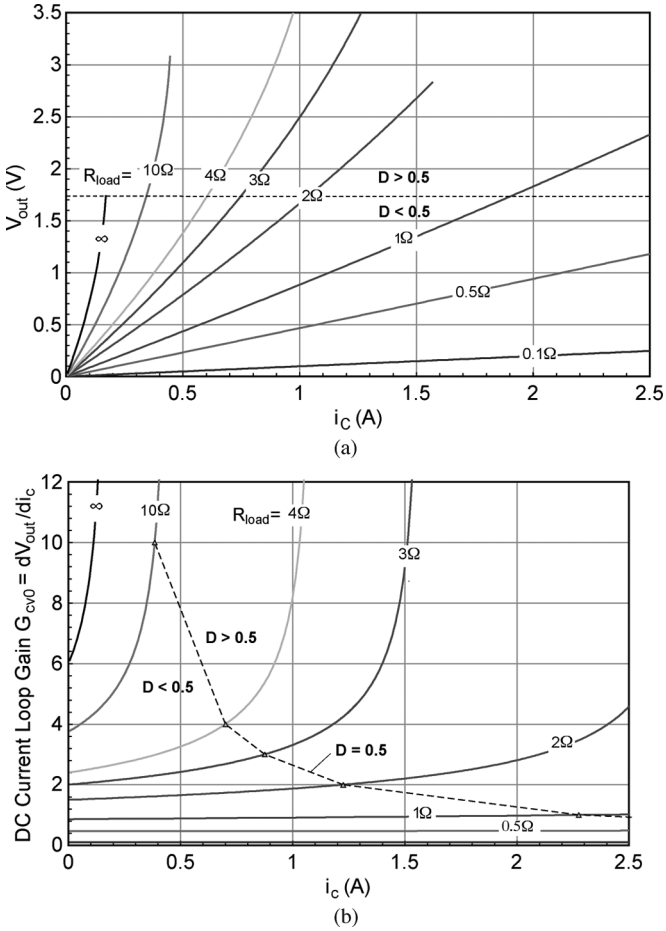

Fig. 4. (a) Output voltage versus current-command and (b) small-signal gain for different values of $R_{\rm load}$.

TABLE I
SYSTEM SPECIFICATIONS

Specification	Value	Units
Input Voltage, V_{in}	2.7-4.2	V
CMOS Process (HV)	0.18	μm
Output Voltage, V_{out}	1	V
Rated Load, I_{load}	0.5	A
Filter, L	1	μH
Filter, C_{out}	4.7	μF
Switching Frequency, f_s	3	MHz
ADC Error Bin (zero error), ΔV_{adc}	13	mV
ADC Error Bin (other bins), ΔV_{adc}	6	mV
ADC Conversion time $t_{conv,adc}$	162	ns
DAC resolution, ΔV_{dac}	2.2	mV
Closed-loop Load Step Response	< 4	μs

The M predicted by (9), which is only valid if slope compensation is not used, is quite conservative, since the system may be designed to operate in pulse-frequency modulation (PFM) or discontinuous current-mode (DCM) at light-loads. In that case, the gain $G_{\rm vc0}$ in (2) should be calculated from (7) at the maximum load resistance $R_{\rm load,max}$, leading to a lower value for M compared to (9). The result is shown in Fig. 5, for the parameters of Table I. The high control-to-output gain in CPM results in a higher resolution requirement for the DAC, compared to the DPWM in voltage-mode control. It can be seen that unlike

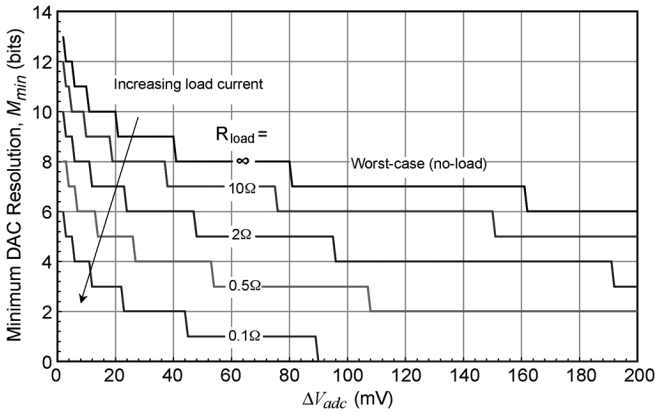

Fig. 5. Minimum DAC resolution for different values of $R_{\rm load}$.

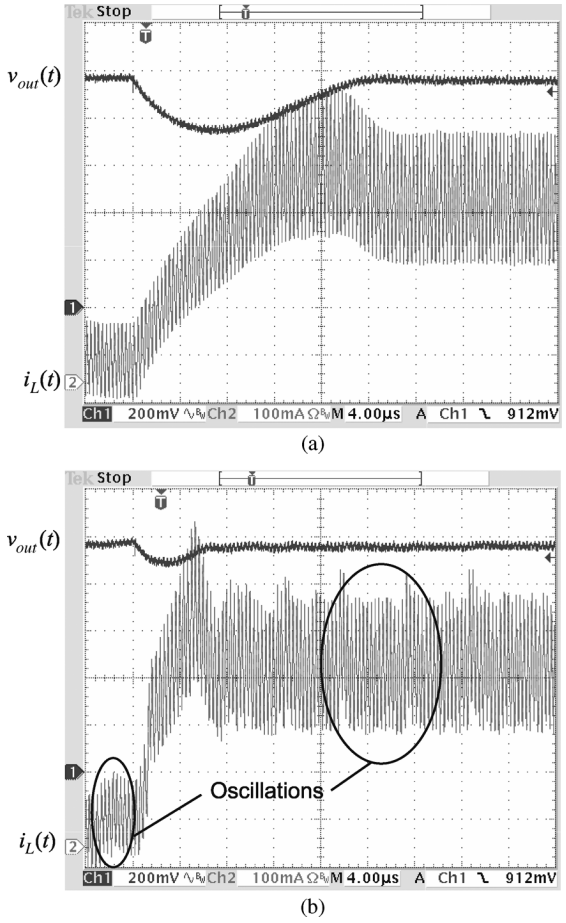

Fig. 6. Load-step response showing the effect of decreasing K_s by 2.5× from (a) to (b).

voltage-mode control in continuous-conduction mode (CCM), the minimum resolution is highly load dependent. The resolution requirements in DCM mode are analyzed in [20]. The presence of limit-cycle oscillations in the inductor current is confirmed experimentally in the load-step response of Fig. 6. For a fixed DAC resolution, reducing the sensing gain K_s by 2.5× leads to visible limit-cycle oscillations in Fig. 6(b), while the response-time is reduced due to the increased loop bandwidth. The oscillations in Fig. 6(b) disappear when the voltage loop is opened, proving that the oscillations are due to the outer regulation loop.

III. Low-Power Charge-Pump DAC

In CPM, the buck converter can be approximated by a first-order system at frequencies well below f_s [5], [21] and therefore a simple digital compensator can be used for the voltage loop, where the difference equation is given by

$$\Delta i_c[n] = i_c[n] - i_c[n-1] = C_0 e[n] - C_1 e[n-1] \quad (12)$$

where $e[n]$ is the digital error and C_{0-1} are the compensation coefficients. While this compensator was chosen to demonstrate the operation of the specialized DAC under closed-loop control, a higher order compensator, or a nonlinear controller can easily be adopted to further improve the transient response if needed. A specialized DAC architecture was developed by using the differential nature of (12), where the input to the DAC consists only of the *change* in the current command, $\Delta i_c[n]$.

The CP-DAC functions as a delay-to-voltage converter, as shown in Fig. 7. All transistors in the CP-DAC are implemented using standard 1.8 V devices. The analog current-command, $v_{\rm cp}(t)$, is stored on the charge-pump capacitor $C_{\rm cp}$, hence the actual digital current command $i_c[n]$ is not explicitly stored in the digital domain, as explained in Section VI. The 8-bit differential current-command $\Delta i_c[n]$ is decoded into three components by the CP-DAC decoder block: a sign-bit, *sign*, a 4-bit delay select code, $DT\langle 3:0\rangle$, and a 4-bit current-select code, $I\_SEL\langle 3:0\rangle$. The switches M_1 and M_4 are activated by the charge-pump logic block for a duration of $\Delta t_{\rm dac}$. The transistors M_2 and M_3 mirror the current generated in the programmable current-sink. For a given differential current-command $\Delta i_c[n]$, the change in $v_{\rm cp}(t)$ is given by

$$\Delta V_{\rm cp} = \pm\frac{I_{\rm cp}\Delta t_{\rm dac}}{C_{\rm cp}} = \frac{(I\_SEL \cdot I_{\rm cp0})(DT \cdot \Delta t_{\rm dac0})}{C_{\rm cp}} \quad (13)$$

where the control parameters $I_{\rm cp}$ and $\Delta t_{\rm dac}$ are proportional to $I\_SEL\langle 3:0\rangle$ and $DT\langle 3:0\rangle$, respectively.

The minimum charge-pump time-interval and current are denoted $\Delta t_{\rm dac0}$ and $I_{\rm cp0}$, respectively. The value of $\Delta t_{\rm dac0}$ is fixed by the delay-line bias current, while $I_{\rm cp0}$ can be adjusted digitally to tune the gain of the DAC. The CP-DAC decoder's digital input/output characteristic that results in a linear relationship between $\Delta i_c[n]$ and $\Delta V_{\rm cp}$ is shown in Fig. 8(a). Only one of the four current branches selected by $I\_SEL\langle 3:0\rangle$ is used at a time. The resulting product of $I\_SEL\langle 3:0\rangle$ and $DT\langle 3:0\rangle$ is linear, as shown in Fig. 8(b). The staircase-like function has a quantization error that grows with $|\Delta i_c[n]|$, thereby introducing a slight nonlinearity into the system. This quantization error has a very limited effect on the system's dynamic behavior, as shown in Section VI-A, since the error is inherently reduced as $|\Delta i_c[n]|$ approaches zero in steady-state operation, and $v_{\rm out}(t)$ approaches the zero-error bin. The CP-DAC architecture also has a guaranteed monotonic characteristic, since the sign of $\Delta i_c[n]$ determines the polarity of the change in $v_{\rm cp}(t)$. For example, using an 8-bit, 2's complement representation for $\Delta i_c[n]$, this simple decoding scheme allows $|\Delta V_{\rm cp}|$ to range from $I_{\rm cp0}\cdot\Delta t_{\rm dac0}$ to $15\times 8 = 120\times I_{\rm cp0}\cdot\Delta t_{\rm dac0}$. The voltage $V_{\rm cp}$ is monotonic with respect to the targeted digital current command $i_c[n]$. This is due to the fact that when an increase in $i_c[n]$ is demanded by the controller, $\Delta i_c[n]$ is positive and

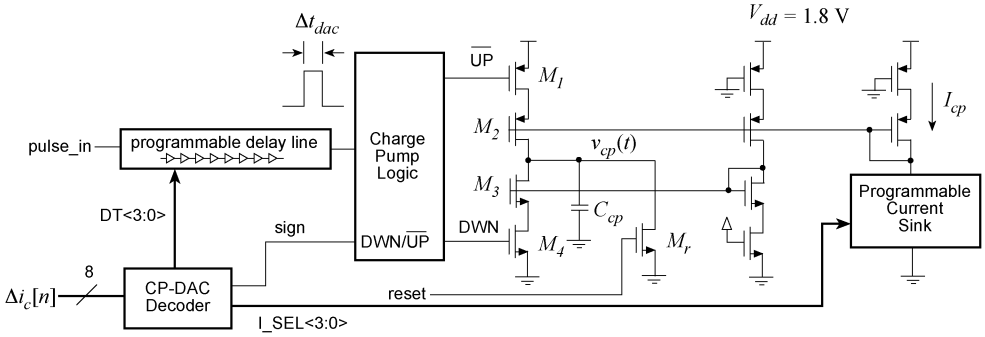

Fig. 7. Charge-pump DAC architecture.

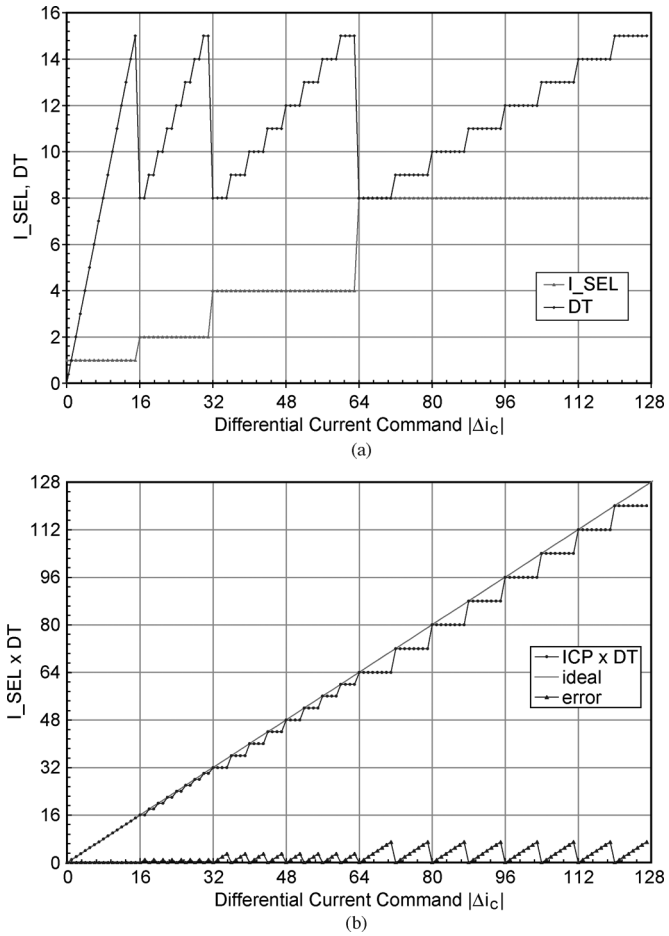

Fig. 8. (a) Input/output characteristic of the CP-DAC decoder; (b) Product of $I\_SEL\langle 3:0\rangle \times DT\langle 3:0\rangle$.

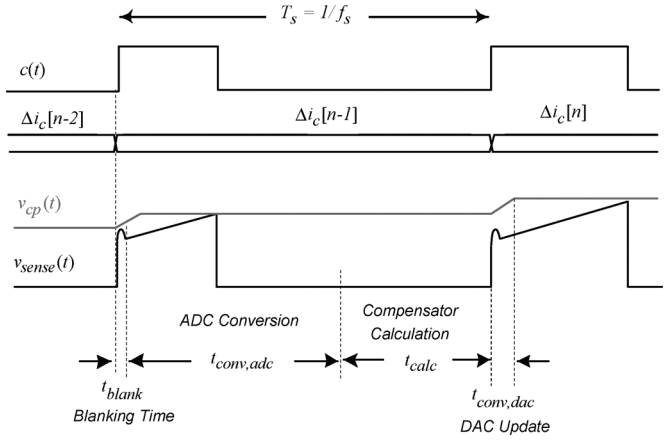

Fig. 9. Timing for the digital control loop.

$v_{\rm cp}(t)$ will necessarily increase in the correct direction, even if the magnitude $\Delta V_{\rm cp}$ has an error due to inaccuracies in the current reference. On the other hand, $\Delta V_{\rm cp}$ is clearly not guaranteed to be monotonic with respect to $\Delta i_c[n]$, due to the binary weighted currents are used in the programmable current sink. This effect is tolerable since it will only cause a slight variation in the dynamic behavior from the nominal case, as shown in Section VI-A.

One of the most attractive features of the CP-DAC is its ability to achieve small changes in $v_{\rm cp}(t)$, without resorting to high-resolution digital hardware. The limit-cycle expression from (2) can be rewritten for the CP-DAC

$$\Delta V_{\rm cp,min} = I_{\rm cp0} \cdot \Delta t_{\rm dac0} < \frac{\Delta V_{\rm adc} K_s}{G_{\rm vc0}}. \tag{14}$$

The condition given by (14) provides a guideline for choosing $I_{\rm cp0}$ and $\Delta t_{\rm dac0}$, for a given ADC quantization of $\Delta V_{\rm adc}$, and current-loop gain $G_{\rm vc0}$ from (8). The DAC conversion time, $t_{\rm conv,dac}$, varies according to $DT\langle 3:0\rangle$

$$t_{\rm conv,dac} = \Delta t_{\rm dac0} \cdot DT \tag{15}$$

where the maximum conversion time $t_{\rm conv,dac} = 15\Delta t_{\rm dac0}$ should be chosen to be less then the minimum PWM *on*-time. The number of bits assigned to the DAC input, $\Delta i_c[n]$, depends on the choice of compensator. In this case, it is determined by the PI compensator coefficients C_0 and C_1 in (12). The maximum value of $\Delta i_c[n]$ occurs for $\{e[n], e[n-1]\} = \{+e_{\max}, -e_{\max}\}$, giving $\Delta i_{\rm c,max} = (C_0 + |C_1|)e_{\max}$, where C_1 is usually < 0. For a given choice of coefficients, the DAC input bus width is therefore chosen to accommodate $\pm\Delta i_{c,max}$, which is quite conservative, since the condition $\{e[n], e[n-1]\} = \{+e_{\max}, -e_{\max}\}$ is unlikely to occur for realistic loads.

The timing for the closed-loop controller is shown in Fig. 9. The first half of the switching cycle is used for sampling the output voltage and generating the digital error signal $e[n]$. The compensator computes the new change in current command $\Delta i_c[n]$ in the second half of the cycle and the CP-DAC output $v_{\rm cp}(t)$ is updated at the start of the blanking time, following the rising edge of $c(t)$.

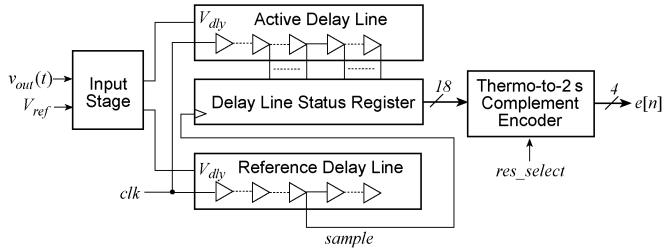

Fig. 10. Simplified architecture of the delay-line ADC.

IV. Delay-Line ADC

The on-chip delay-line ADC quantizes the difference between $v_{\rm out}(t)$ and $V_{\rm ref}$. The delay-line ADC [22]–[24] has several advantages over the comparator-based FLASH ADCs. These include improved noise-immunity due to inherent averaging, lack of sample-and-hold requirement, flexible choice of conversion-time and predominantly digital architecture [25]. The delay-line ADC used in this work is shown in Fig. 10 and was originally implemented in [26], for a voltage-mode controller application.

The converter operates as follows. The differential delay-cell bias circuit generates two control voltages, such that the difference between the propagation times of the two delay-lines is proportional to $v_{\rm out} - V_{\rm ref}$. The *sample* signal clocks the delay-line status register, which triggers the end of the conversion cycle. The thermometer-code output from the active delay-line, which depends on $v_{\rm out}$, is converted into a two's complement format that represents the error. As a result, the ADC output $e[n]$ is proportional to the average voltage error during the conversion time $t_{\rm conv,adc}$

$$e[n] \propto \int_0^{t_{\rm conv,adc}} (V_{\rm ref}(t) - v_{\rm out}(t))\, dt \tag{16}$$

The use of the reference delay-line to generate the *sample* signal ensures that the ADC characteristics are not affected by common-mode variations in the ADC inputs, $v_{\rm out}$ and $V_{\rm ref}$. IC design issues related to this architecture are covered in [25] and [26]. For debugging purposes, the ADC includes a resolution-select bit, res_select. This control bit can be used to double the ADC resolution by reducing the ADC voltage-bin size, $\Delta V_{\rm adc}$, by 50%.

V. Analog Current Sensor and Comparator

The integrated current sensor and high-speed comparator of Fig. 3 are described in this section.

A. Current Sensor

The current sensor is shown in Fig. 11. The topology is derived from the architecture demonstrated in [6]. All transistors in the current-sensor are implemented using thick gate oxide for 5 V compatibility. The sensing transistor M_1, or SenseFET [27], is embedded in the layout of the high-side power transistor and forms a current mirror with M_P. Using this current mirror, the

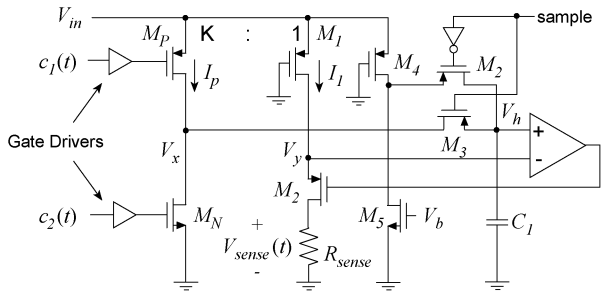

Fig. 11. Closed-loop high-side current sensor.

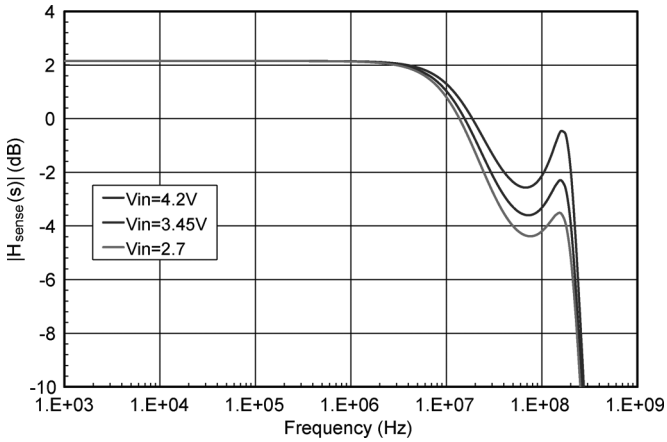

Fig. 12. Closed-loop frequency response of the benchmark current sensor for $2.7\ {\rm V} < V_{\rm in} < 4.2\ {\rm V}$.

sensed current $I_1 = I_P/K$ is converted into a voltage by the sense resistor $R_{\rm sense}$. The sensing ratio K_s is therefore given by

$$K_s = \frac{V_{\rm sense}(t)}{I_P(t)} = \frac{R_{\rm sense}}{K}. \tag{17}$$

A sensing gain of $K_s = 1.28\ \Omega$ (2.1 dB) is achieved using $K = 1170$ and $R_{\rm sense} = 1.5\ {\rm k}\Omega$. The maximum value of K, which determines the current overhead, is constrained by matching requirements. Accurate current mirroring from M_P to M_1 is achieved by forcing the drain of M_1, V_y, to equal the drain voltage of M_P, V_x, when M_P is *on*. This condition is enforced by the high-bandwidth amplifier and the voltage sampling circuit consisting of M_2, M_3, and C_1. The minimum duty-cycle is limited by the response time $V_{\rm sense}(t)$ following the turn-on of M_P. The transistors M_4 and M_5 are used to maintain a minimum bias current through M_1 when M_P is off. The internally compensated amplifier has a folded cascode topology and uses the 5 V compatible transistors in the 0.18 μm CMOS process. An n-channel differential pair is used in the input stage to accommodate the high voltage at the input, $V_x = V_{\rm in} - I_p \cdot R_{\rm on,p}$. The simulated closed-loop sensing response $H_{\rm sense}(s) = V_{\rm sense}/I_P$ is shown in Fig. 12. The closed-loop 3 dB bandwidth ranges from 25.5 MHz at $V_{\rm in} = 2.7$ V to 17.9 MHz at $V_{\rm in} = 4.2$ V, making this current sensor suitable for switching frequencies up to 5 MHz, based on system-level simulations. Slope compensation can easily be added to this circuit by introducing a compensation ramp at the $V_{\rm sense}$ node.

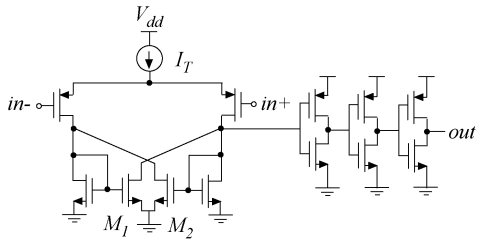

Fig. 13. CMOS High-speed analog comparator.

B. Analog Comparator

The analog continuous-time comparator used in the benchmark CPM design is shown in Fig. 13. The cross-coupled transistors M_1 and M_2 are used to increase the comparator switching speed when the differential input voltage changes polarity. Three cascaded inverters are used to regenerate a rail-to-rail output. A p-channel differential pair is used in the input stage to accommodate the low voltage at the input, $V_{\rm sense}(t)$. During steady-state, the comparator's negative input $in-$ is connected to the steady-state $v_c(t)$ from the compensator, while $in+$ is connected to the sense current $V_{\rm sense}(t)$. The comparator delay is heavily dependent on the slope of $V_{\rm sense}(t)$ during $t_{\rm on}$. During the tracking phase of the current-sensor, the voltage slope at the input of the comparator is obtained from (17) and given by (18) for a buck converter

$$m_v = \frac{\partial}{\partial t} V_{\rm sense}(t) = K_s m_1 = \frac{(V_{\rm in} - V_{\rm out}) R_{\rm sense}}{LK}. \qquad (18)$$

The simulated comparator delay ranges from 6.2 ns and 13.8 ns for $\mathrm{SR} = 2\ \mathrm{V}/\mu\mathrm{s}$ and $m_v = 0.1\ \mathrm{V}/\mu\mathrm{s}$ respectively. The total current consumption for the comparator is 59.4 μA from the internal 1.8 V supply, for a switching frequency of $f_s = 3\,\mathrm{MHz}$.

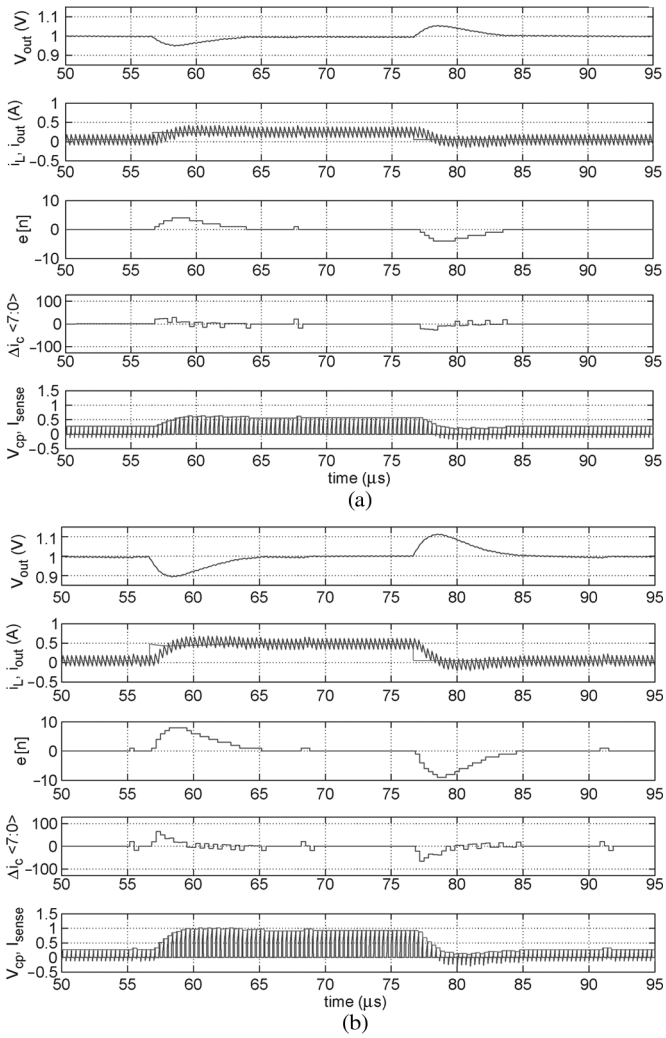

Fig. 14. Simulated response of the closed-loop system for: (a) 50–250 mA and (b) 50–500 mA load steps.

VI. Closed-Loop Response

An accurate system model was generated in Matlab/Simulink, based on the extracted parameters of the power-stage and the mixed-signal blocks, as well as the finite precision of the digital registers in the digital compensator. The simulated step-response for the closed-loop system is shown in Fig. 14(a) and (b) for 50–250 mA and 50–500 mA load steps, respectively. The output voltage is regulated back into the zero-error bin ($e[n] = 0$) within about 5 μs for a load-step of 50–250 mA. The differential current-command ($\Delta i_c[n]$) waveform shows that the CP-DAC immediately adjusts the peak inductor current following the load-step. The system parameters are summarized in Table I.

A. Effect of Nonlinearity in the CP-DAC

As mentioned in Section III, the mismatch in the binary-weighted sources in the programmable current sink can lead to a nonmonotonic characteristic from $\Delta i_c[n]$ to $\Delta V_{\rm cp}$, despite the fact that $v_{\rm cp}(t)$ is monotonic with respect to the target $i_c[n]$. This effect was investigated by simulating the converter in closed-loop with different combinations of mismatch in the binary weighted current sinks of Fig. 7, ranging from 0 to 20% of $I_{\rm cp0}$. The ideal ratios $\{1, 2, 4, 8\} \times I_{\rm cp0}$ were varied from $\{1, 1.8, 3.8, 7.8\} \times I_{\rm cp0}$ to $\{1, 2.2, 4.2, 8.2\} \times I_{\rm cp0}$ with 28 combinations. The overlapped CP-DAC input/output characteristics are shown in Fig. 15(a). The figure also includes the characteristic for an ideal DAC with uniform quantization.

The resulting 29 closed-loop responses are overlapped in Fig. 15(b). The simulation confirms that the response is stable in all cases, with only minor differences in the settling time and voltage fluctuation.

B. Effect of Charge Pump Mismatch

In traditional mixed-signal CPM, the steady-state value of the current command $i_c[n]$ can be very useful for performing efficiency optimization [28] or simply for protecting the power-stage. Unfortunately the standard CP-DAC architecture does not allow $i_c[n]$ to be accurately tracked in the digital compensator due to mismatches in the charging and dis-charging paths of the charge-pump in Fig. 7. The mismatch in the currents through M_2 and M_3 causes the $\Delta V_{\rm cp}$ in (13) to be dependent on the sign of $\Delta i_c[n]$. The effect of a 15% systematic mismatch in the

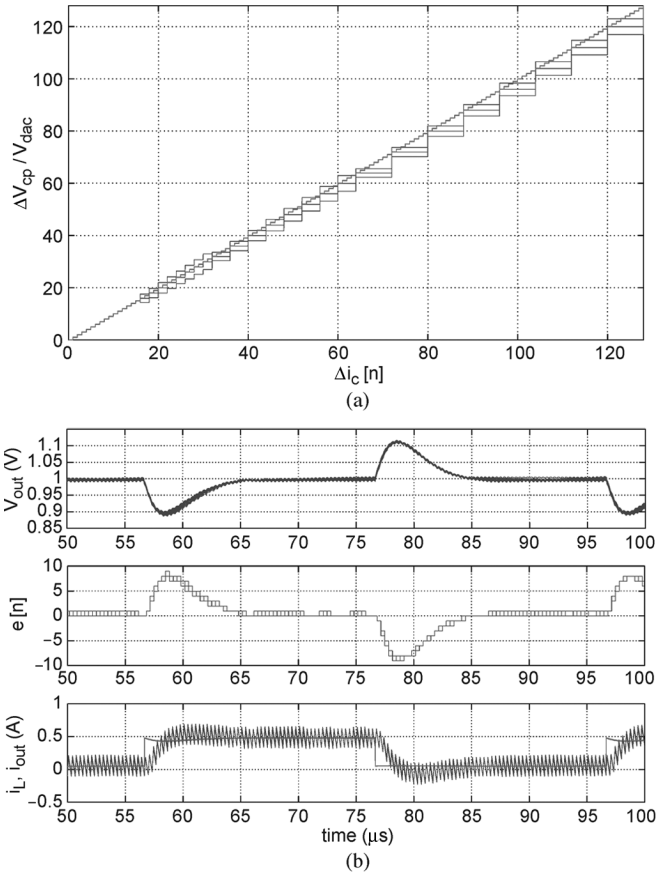

Fig. 15. (a) Overlapped CP-DAC input/output characteristic for different combinations of the current sink ratios in the CP-DAC. (b) Overlapped closed-loop 50–500 mA load-step responses for the 28 combinations of CP-DAC characteristics, showing the minor effect of the CP-DAC nonlinearity.

charge and discharge currents is shown in Fig. 16 for the system operating in closed-loop with repeated load steps. The current command $i_c[n]$ is generated in the digital compensator using $i_c[n] = \sum_{j=0}^{n} \Delta i_c[j]$. The 15% current mismatch causes the sum to diverge and the error between $i_c[n]$ and the scaled peak inductor current will grow with each load transient, eventually leading to saturation due to the finite width of the registers. In terms of the dynamic performance, a reasonable mismatch is not problematic, since it only causes a slight variation in the gain of the CP-DAC depending on the sign of $\Delta i_c[n]$. Instead of using $i_c[n]$ for efficiency optimization, it is more practical to periodically sample the average value of V_{sense} to estimate the load current, which is beyond the scope of this paper.

VII. Experimental Results

The converter shown in Fig. 3 includes a segmented power-stage similar to [29] for improved light-load efficiency. It was fabricated in a 0.18 μm CMOS process with 5 V transistors, which are sufficient to accommodate the single-cell lithium-ion battery voltage range of 2.7 V to 4.2 V. The chip micrograph is shown in Fig. 17. The die measures 2.7×1.25 mm^2, while the total active area for the controller (excluding the power-stage) is only 0.077 mm^2. The total controller current-draw, which is dominated by the on-chip senseFET current-sensor, is below 250 μA at $I_{\text{out}} = 50$ mA. The current-draw and active area of each block are given in Table II.

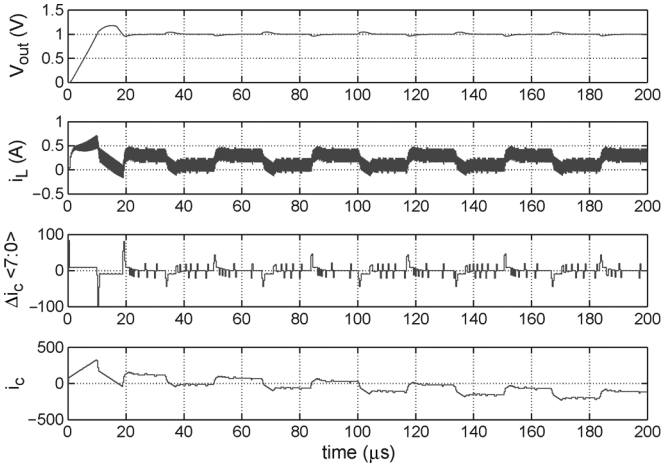

Fig. 16. Simulated closed-loop response with a 15% mismatch between the charge and discharge currents in the CP DAC.

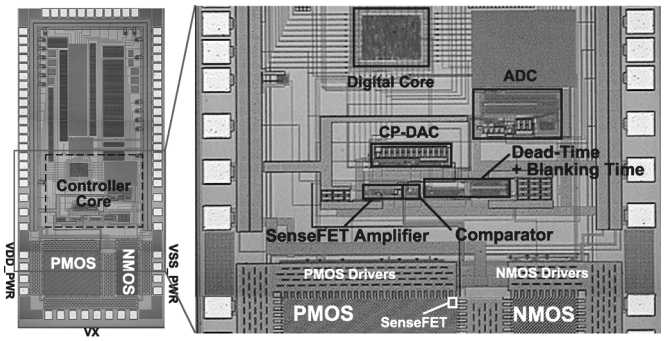

Fig. 17. Die photo of the hybrid CPM IC fabricated in a 0.18 μm CMOS process.

TABLE II
Summary of Area and Power Consumption for the Controller Portion of the CPM IC

IC Block	Area (mm^2)	Current-Draw (μA)	Current-Draw (μA/MHz)	Condition V_{in} = 3.7V, V_{out} = 1V, f_s= 3MHz
Charge Pump DAC	0.0135	2.96	0.98	Steady-state
Delay-Line ADC	0.0295	25.9	8.65	Steady-state
SenseFET Core	0.0029	123	41.2	I_{out} = 50 mA
		169	56.6	I_{out} = 250 mA
		227	75.8	I_{out} = 500 mA
CPM Comparator	0.0011	59	19.7	
Dead-Time	0.0078	5.46	1.82	
Bias+Reference	0.0018	23.2	7.73	
Digital Core	0.0205	10	3.3	Steady-state
Total	0.0770	249.5	83.2	I_{out} = 50 mA
		295.5	98.8	I_{out} = 250 mA
		353.5	117.8	I_{out} = 500 mA

A. Power-Stage Implementation

The segmented power-stage shown in Fig. 3 includes a pMOS high-side switch and an nMOS low-side switch. Each switch is divided into seven identical segments, with dedicated gate-drivers whose inputs are connected in a binary weighted fashion. The effective W/L of the power-stage transistors can be dynamically changes to optimized the gate-drive and conduction losses depending on the load current. The power-stage uses a hybrid-waffle layout pattern, where the source and drain cells are arranged in checkerboard structure with the associated routing

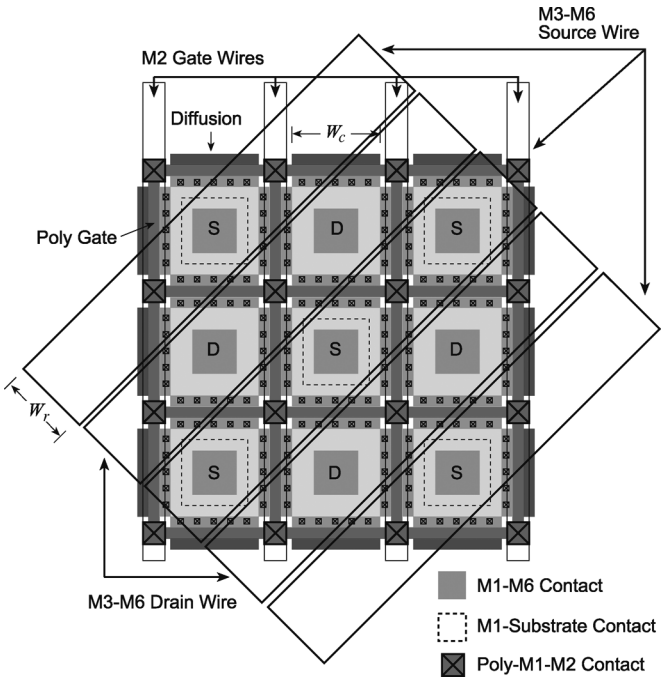

Fig. 18. Illustration of the basic cell for the power MOSFET hybrid-waffle layout structure.

TABLE III
POWER-STAGE PERFORMANCE

	Switch		Units	Condition
	pMOS	nMOS		(V_{in} = 3.6 V) (V_{out} = 1.8 V)
CMOS Process	0.18 μm HV			
Breakdown Voltage	>5		V	
Layout Pattern	Hybrid Waffle			
Total Width, W	34.6	13	mm	
Drawn Length, L	0.5	0.6	μm	
Active Area, A	0.200	0.074	mm^2	
R_{ch}	208	152	mΩ	Simulated
Q_g	213	78.2	pC	Simulated I_D = 500 mA
FOM$_1$	44.3	11.88	nC·mΩ	$Q_{gate} \cdot R_{ch}$
R_{on}	366	310	mΩ	Measured Packaged
P_{gate}	3.43	1.56	mW	Measured
				f_s = 4 MHz
Specific R_{on}	73.2	22.94	mΩ mm^2	Packaged
FOM$_3$	0.314	0.121	pJ·mΩ	$\frac{P_g}{f_s} \cdot R_{on}$
Peak Efficiency, η	91.3		%	V_{in} = 2.7 V
	88.8		%	V_{in} = 3.6 V
	87.8		%	V_{in} = 4.2 V

channels (drain and source) oriented at 45°, as in the standard waffle-type layout [30], [31]. The main difference lies in the use of a cell-pitch that intentionally exceeds the minimum spacing required to fit a single diffusion contact, as shown in Fig. 18, where the cell pitch is exaggerated. This flexible choice of cell pitch W_c allows the relative area allocation for contacts and active area to be optimized. The power-stage characteristics are given in Table III. The efficiency of the power-stage was measured at $f_s = 4$ MHz and with $L = 2$ μH, for comparison with the 1st generation power-stage in [29]. The result is shown in Fig. 19. The efficiency is shown for different values of the 3-bit segment enable codes en_P and en_N. The peak efficiency for different input voltages is shown in Table III. A peak efficiency

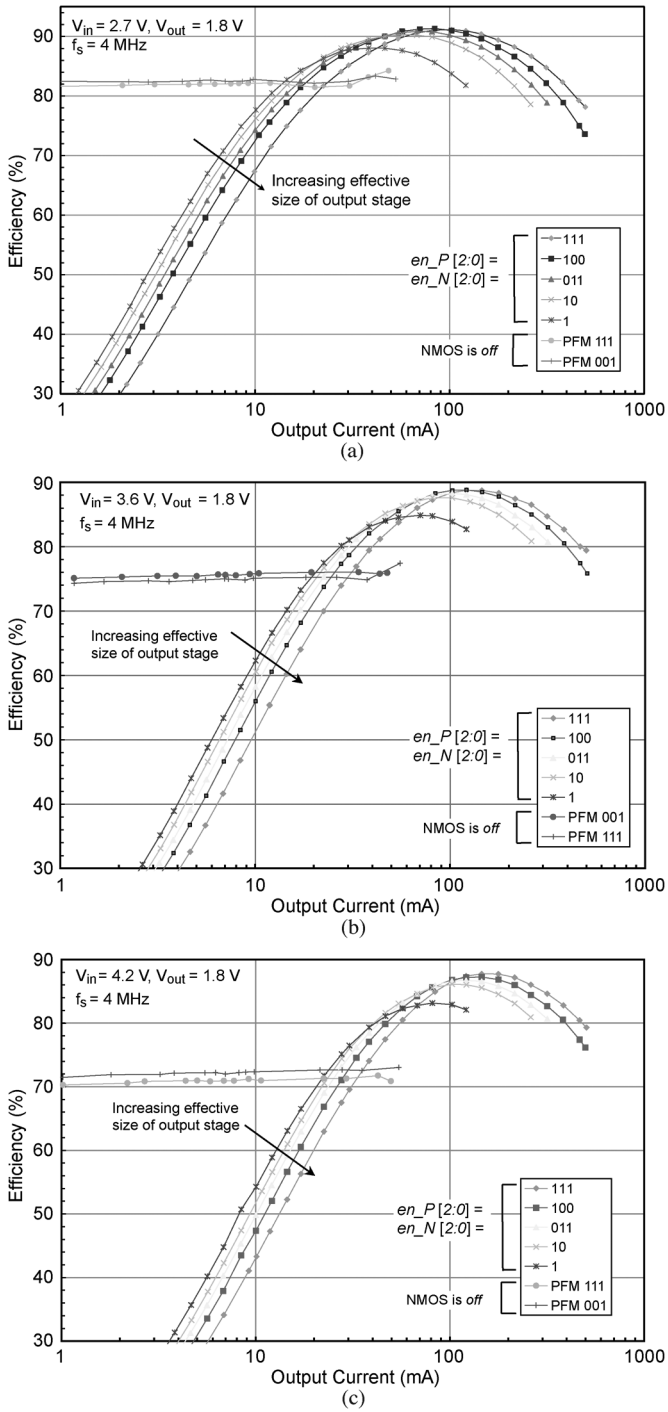

Fig. 19. Measured efficiency versus load current at: (a) $V_{\rm in} = 2.7$ V; (b) $V_{\rm in} = 3.6$ V; and (c) $V_{\rm in} = 4.2$ V with different segment enable codes and modes.

of 91.3% is obtained for $V_{\rm in} = 2.7$ V. The real-time control of the segmented power-stage for efficiency optimization [28], [29] is beyond the scope of this paper.

B. Closed-Loop Current Sensor

The closed-loop current-sensor output $V_{\rm sense}(t)$ is shown in Fig. 20(a) for the converter operating in continuous conduction mode (CCM) in open loop. Fig. 20(b) shows the sensor output when the inductor current is negative when the high-side switch is turned on. This causes $V_{\rm sense}(t)$ to saturate to 0 until $i_L(t)$ becomes positive. The sense voltage $V_{\rm sense}(t)$ is brought

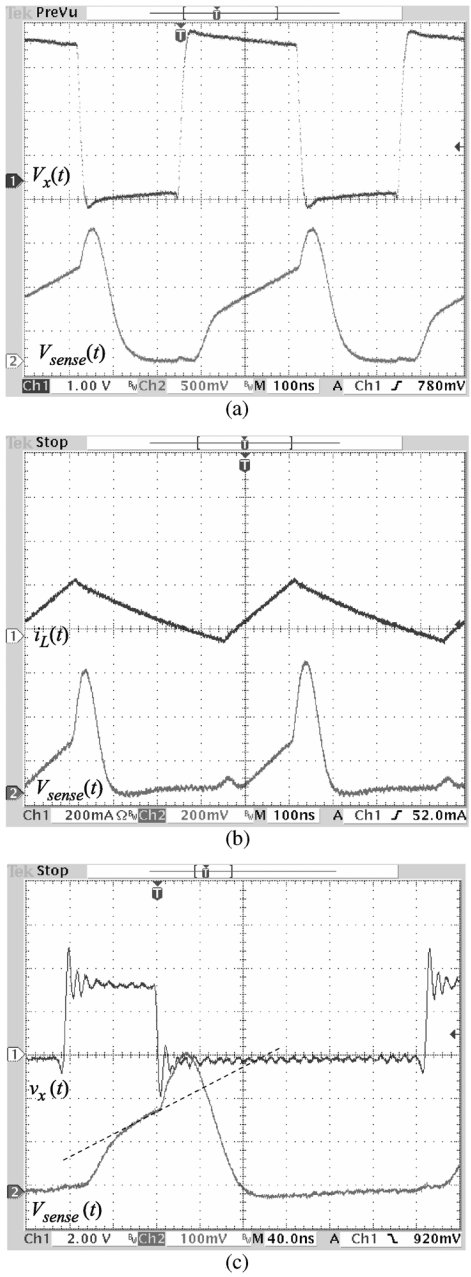

Fig. 20. (a) Steady-state waveforms for the integrated current sensor with $V_g = 4.2$ V, $f_s = 2$ MHz. (b) SenseFET waveforms at $I_{\rm out} = 125$ mA. (c) SenseFET waveforms operating at $f_s = 3$ MHz. The equivalent load capacitance at $V_{\rm sense}(t)$ is 20 pF.

off-chip without analog buffering, therefore the loading from the oscilloscope probes and the bond pads significantly reduces the bandwidth of current-sensing loop and limits the maximum switching frequency.

C. Charge-Pump DAC Measurement

The CP-DAC output, $v_{\rm cp}(t)$, is a sensitive analog node that is not accessible off-chip. The DAC was characterized by connecting an external ramp to the $V_{\rm sense}(t)$ node, while measuring the pulse-width of the comparator output. After discharging or precharging $C_{\rm cp}$, the CP-DAC digital input was held constant at $\Delta i_c[n]$. This causes the comparator output pulse-width to increase or decrease every cycle, depending on the sign of $\Delta i_c[n]$.

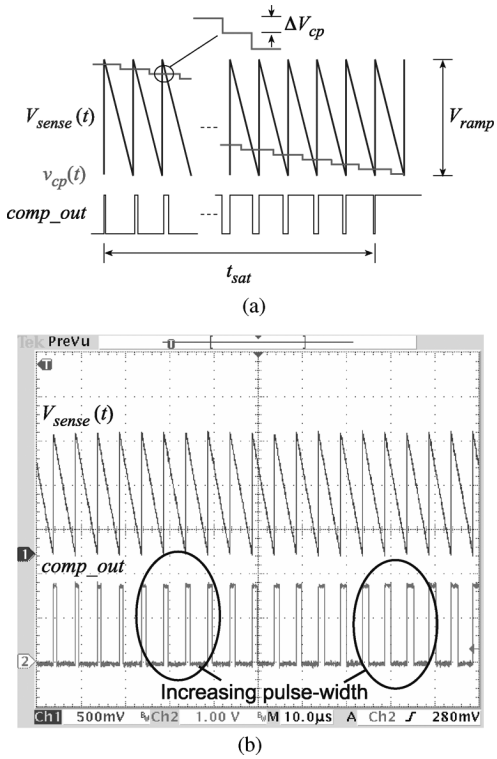

Fig. 21. (a) Characterization of the CP-DAC. (b) Measured ramp-down of the CP-DAC output.

The ideal waveforms are shown in Fig. 21(a), where $\Delta V_{\rm cp}$ can be estimated using (19) for $V_{\rm ramp} \gg \Delta V_{\rm cp}$. The measured comparator output is shown in Fig. 21(b) for $\Delta i_c[n] < 0$.

$$\Delta V_{\rm cp} \approx \frac{V_{\rm ramp}}{f_{\rm ramp} t_{\rm sat}} \tag{19}$$

The measured values for $\Delta V_{\rm cp}$ versus $DT\langle 3:0\rangle$, based on (19) are shown in Fig. 22(a).

The minimum value of $\Delta V_{\rm cp} = 2.11$ mV occurs at $DT\langle 3:0\rangle = 0001$, $ICP\langle 3:0\rangle = 0001$, and for the tuning parameter $DT\_TUNE\langle 3:0\rangle = 1111$. If a full-range flash DAC architecture were used to achieve the same $\Delta V_{\rm cp}$, a resolution of 10 bits would be required with $V_r = 1.8$ V. The extracted $\Delta V_{\rm cp}$ has a linear relationship with $ICP\langle 3:0\rangle$, as shown in Fig. 22(b). As mentioned in Section III, the CP-DAC has a guaranteed monotonic behavior. The leakage on the charge-pump capacitor, due to capacitive coupling, was investigated by precharging $v_{\rm cp}(t)$ and setting $ICP\langle 3:0\rangle = DT\langle 3:0\rangle = 0$; The resulting extracted $v_{\rm cp}(t)$ is shown in Fig. 23 for two different precharge values. In both cases, $v_{\rm cp}(t)$ drops by only $\approx 50\ \mu$V per clock cycle. The voltage-loop compensator is easily capable of compensating for this effect by periodically increasing $v_{\rm cp}(t)$ when the accumulated leakage causes $v_{\rm out}(t)$ to exit the zero-error bin.

D. Analog-to-Digital Converter

The measured transfer characteristic of the ADC is shown in Fig. 24, where the results are over-lapped for different values of $V_{\rm ref}$. The ADC functions correctly for $V_{\rm ref}$ down to 0.2 V. The ADC has two resolution settings, where the size of the quantization bins (apart from the zero-error bin) can be controlled. The

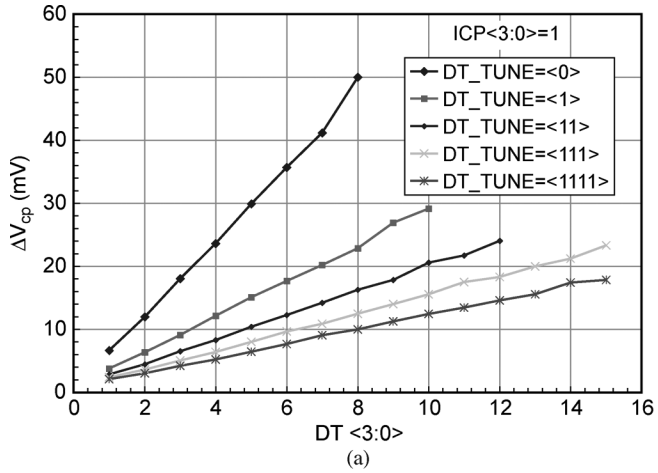

Fig. 22. Measured (a) $\Delta V_{\rm cp}$ versus $DT\langle 3:0\rangle$ for different tuning values of $DT\_TUNE\langle 3:0\rangle$. (b) $\Delta V_{\rm cp}$ versus $ICP\langle 3:0\rangle$.

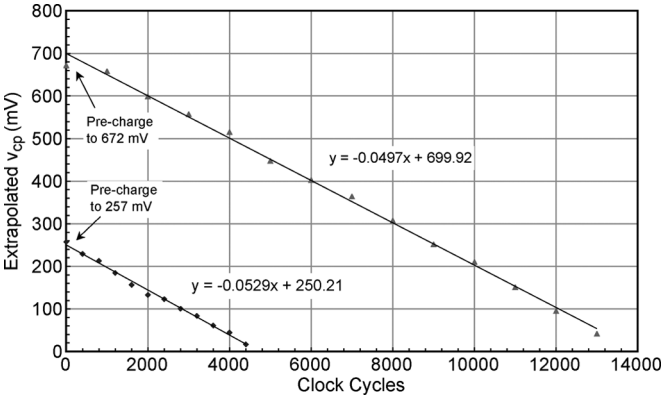

Fig. 23. Measured leakage of $v_{\rm cp}(t)$ due to charge coupling. The extracted slope is $-50\ \mu$V/clock cycle.

zero-error voltage bin $\Delta V_{\rm adc}$ varies from 13 mV to 15 mV for $0.2\ {\rm V} < V_{\rm ref} < 1.8\ {\rm V}$, while the other voltage bins correspond to 6 mV. An average conversion time of 162 ns is achieved, with less then 2% variation over the reference voltage range.

E. Closed-Loop Response

The closed-loop system's response to a 45 mA–250 mA load-step at $V_{\rm out} = 1$ V, $f_s = 3$ MHz, is shown in Fig. 25. The controller has a fast settling-time of $t_{\rm res} = 4\ \mu$s and a voltage deviation of only $\Delta V_{\rm res} < 50$ mV at $f_s = 3$ MHz. This transient

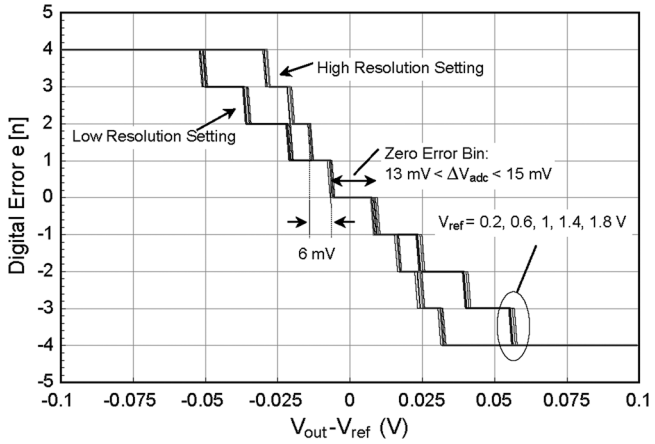

Fig. 24. Measured and overlapped ADC characteristics for $0.2\ {\rm V} < V_{\rm ref} < 1.8$ V, for both ADC resolution settings.

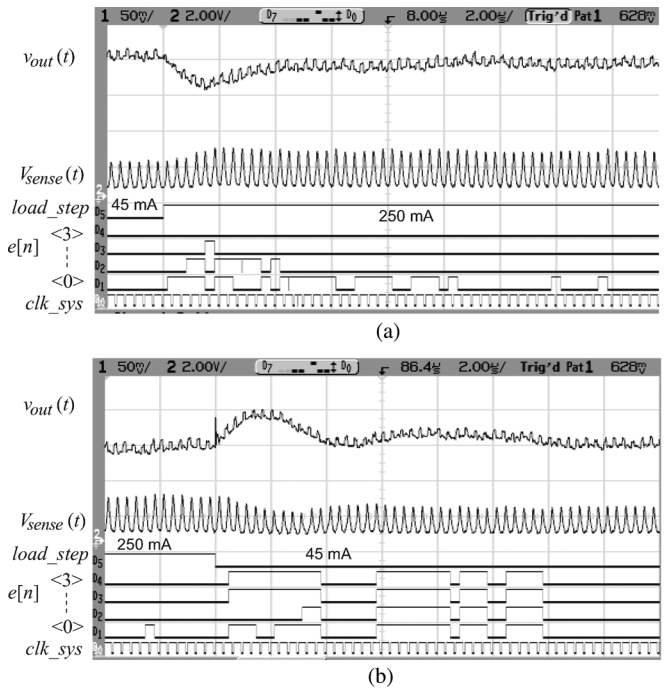

Fig. 25. (a) Light-to-heavy and (b) heavy-to-light load-step response. Ch-1: $v_{\rm out}(t)$, 50 mV/div. Ch-2: $V_{\rm sense}(t)$, 2 V/div. Time scale: 2 μs/div.

behavior is nearly identical to the system simulation shown in Fig. 14. The rapid control of the inductor current is apparent from $V_{\rm sense}(t)$ waveform, which is the output of the on-chip high-bandwidth current-sensor. The dc load regulation of the converter is shown in Fig. 26, which shows a total deviation of 45 mV.

VIII. Conclusion

A low-power solution has been proposed for implementing mixed-signal peak current-mode control in dc–dc converters for portable applications. The charge-pump DAC has relatively poor linearity compared to more expensive DAC topologies; however, this can be tolerated since the system runs in closed-loop. The CP-DAC has a guaranteed monotonic behavior from the digital current command $i_c[n]$ to the peak inductor current which is essential for maintaining stability. It was shown that mismatches in the charge and discharge

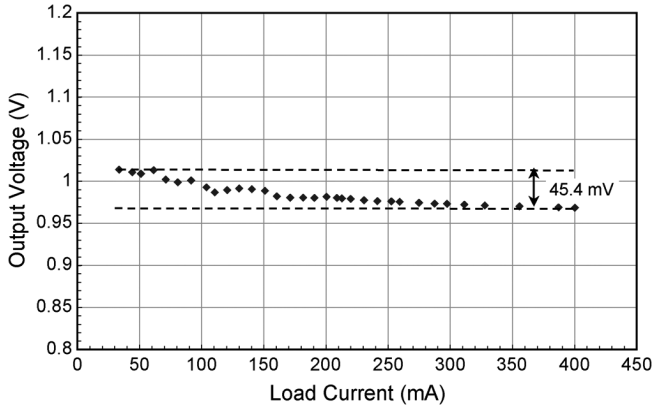

Fig. 26. DC load regulation curve in closed loop.

currents in the charge-pump make it impossible to internal store $i_c[n]$ in the digital domain without using some form of calibration. This is not a major limitation since many linear and nonlinear digital compensators can be implemented simply by calculating $\Delta i_c[n]$ each cycle. A major advantage of the CP-DAC over flash and $\Delta\Sigma$ architectures is the fact that it consumes nearly zero current when the dc–dc converter is in steady-state. The power consumption of the CP-DAC scales with the frequency of the load transients. The prototype IC has a fast transient response which can be further improved by using a more sophisticated compensator. The operating frequency was primarily limited by the bandwidth of the current sensor, since the power-stage can easily operate beyond 10 MHz. The output voltage range can easily be extended by implementing traditional analog slope compensation.

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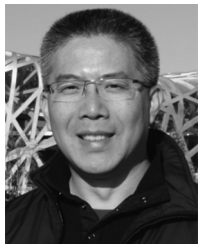

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