Sensorless Self-Tuning Digital CPM Controller With Multiple Parameter Estimation and Thermal Stress Equalization

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***Abstract*—This paper introduces a practical sensorless average current-programmed mode controller for low-power dc–dc converters operating at high switching frequencies. The controller accurately estimates inductor currents and identifies main converter parameters. Namely, total conduction losses in each of the phases as well as the inductors and output capacitance values are identified. The estimate of the losses is used to monitor temperature of the components without costly thermal sensors and for current sharing based on thermal stress equalization increasing system reliability. The identified filter values are utilized in a transient-mode controller for obtaining response with virtually minimum output voltage deviation. The key element of the new controller is a self-tuning digital multiparameter estimator that operates on the inductor time-constant matching principle. It estimates the average inductor current over one switching cycle using an adaptive IIR filter and, in the same process, identifies other converter parameters. The operation of the controller is verified with a single-phase 12 to 1.5 V, 15 W and a dual-phase 12 to 1.8 V, 80 W buck converter prototypes operating at 500 kHz switching frequency. The results show that the controller estimates the current and temperature of the components with better than 10% accuracy, effectively equalizes phase temperatures, and provides virtually minimum output voltage deviation during load transients. The implementation also shows that the controller is well suited for on-chip implementation. Its full realization requires less than 16 000 logic gates and two relatively simple ADCs that, in a standard 0.18-μm CMOS process, can be implemented on a small silicon area, no larger than 0.6 mm^2.**

***Index Terms*—Current sharing, digital control, low-power dc–dc converters, parameter estimation, self-tuning.**

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I. Introduction

In LOW-POWER switch-mode power supplies (SMPS) used in applications, such as computers, medical, automotive and telecommunication equipment, reliable operation, and small volume implementation are of key importance. To ensure reliable operation, dedicated controllers usually employ current measurement for overload protection [1], as well as for desired current sharing [2]–[6] between the converter phases in multiphase dc–dc converter topologies.

Generally, the current measurement methods can be divided into voltage drop measurement and observer (i.e., estimator) based. In the first category, the voltage drop caused by the current passing through a sense resistor or a MOSFET is measured [7]–[11]. Observer-based systems usually estimate current from the voltage across the power stage inductor [12]–[14]. In most cases, existing solutions are not well suited for integration with rapidly emerging digital controllers for low-power high-frequency dc–dc converters [15]. Voltage drop methods either decrease power processing efficiency [7] or require a large gain-bandwidth amplifier, which is costly and challenging to realize in the latest CMOS digital processes [15]. This is mostly due to unacceptably large silicon area requirement and power consumption of such an amplifier [16]. Also, the conventional analog architectures often cannot operate at the limited supply voltages of standard CMOS digital circuits [15]. On the other hand, the observers suffer from a limited accuracy [7], [14]. Current estimation method relies on a prior knowledge of the inductance and equivalent series resistance values [12], [13], i.e., the inductor time constant, which changes with operating conditions and external influences [14]. To solve for this, a mixed-signal system relying on digital adjustment of a multibank analog filter is proposed [17]. The system effectively minimizes influence of the time-constant mismatch at the price of an increased external part count.

In multiphase converters, regulation of phase currents is also required. Even if all phases are designed equally some of them can take significantly larger currents than others, due to mismatches in actual component values. Consequently, current and thermal stress-related system failures occur [1]. To minimize the current mismatch, direct and indirect current equalizing methods are applied. Direct methods [3]–[5] usually utilize current sensors in each of the phases to match phase currents using control algorithms. Indirect methods match the duty ratios of control signals for all phases, such that the maximum processing

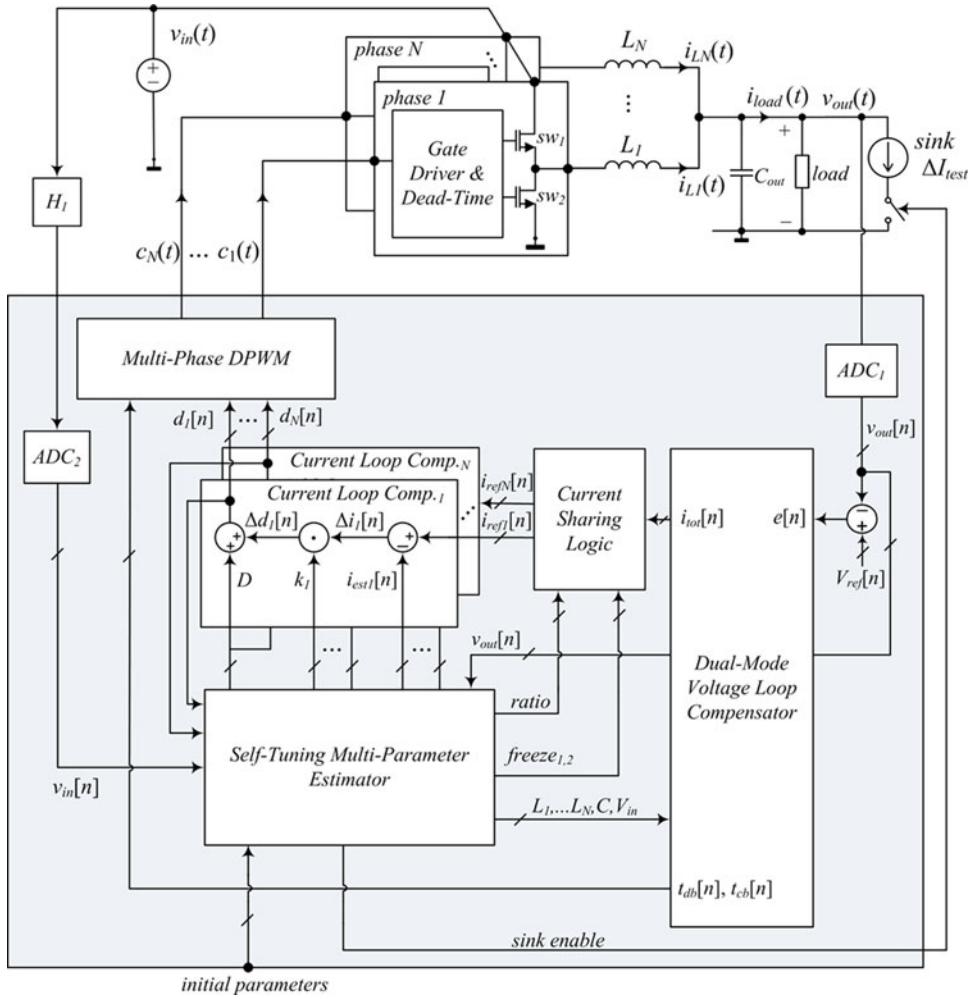

Fig. 1. *N*-phase buck converter regulated by the sensorless self-tuning controller with multiparameter estimation.

efficiency is achieved [18], [19]. However, from the reliability standpoint, neither of the schemes is optimal. In both cases, a possible significant mismatch in the phase temperatures causes frequent thermal cycles of the power stage resulting in a premature system failure [20]. A current sharing method based on maintaining equal temperature of all phases is proposed in [21] and [22]. However, though very useful, the proposed solution has not been widely adopted, mainly due to practical implementation problems. The system requires costly temperature sensors [23], [24] placed next to the heat generating components that, with the exception of high-end systems, are not suitable for the targeted high-volume low-power applications. In addition, the temperature sensors further increase component counts, circuit layout area, and the overall size of the system.

The main goal of this paper is to introduce a practical fully digital controller of Fig. 1 that eliminates the need for costly current and temperature sensors, and is well suited for a single-chip implementation. It accurately estimates phase currents, provides temperature monitoring, and equalizes thermal stress. In addition, the controller also has a fast dynamic response achieving minimal output voltage deviation during transients. The key controller element is novel self-tuning multiple parameter estimator. It estimates the average inductor currents over one switching cycle, the total conduction losses of all phases, the inductance values, and the output capacitance. The estimator relies on the well-known current observer architecture [13] widely used in analog systems. In this case, its fully digital implementation, not only improves the observer accuracy, but also allows estimation of other converter parameters.

The paper is organized as follows. In Section II, the operation of the controller is briefly explained. Section III describes the self-tuning multiparameter estimator. First, the principle of operation is described on a single-phase dc–dc converter example. Then, the concept is extended to multiphase solutions. Section IV gives details of a practical estimator implementation. Section V describes a new implementation of the current sharing method that utilizes loss estimation to equalize thermal stress, without a temperature sensor. In Section VI, the operation of the minimum deviation transient-mode compensator is explained. Finally, experimental systems and results verifying effectiveness of the introduced controller are presented in Section VII.

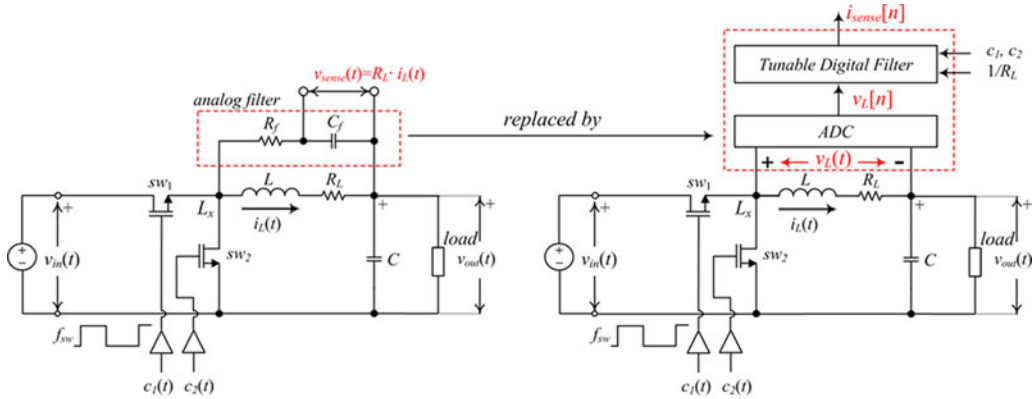

Fig. 2. Current sensing principle. (a) Conventional analog implementation. (b) Implementation with a self-tuning digital filter.

II. System Description

The system of Fig. 1 operates as a modification of an average current-programmed mode (CPM) controller [25]. It is comprised of a dual-mode voltage compensator, current sharing logic, and current-compensating loops. In steady state, the *dual-mode compensator* samples the error signal $e[n]$ and calculates $i_{\rm tot}[n]$, a digital value proportional to the total current of all phases (i.e., to the load current). The $i_{\rm tot}[n]$ is then passed to *current sharing logic* that sets current references for all converter phases $i_{\rm ref1}[n]$ to $i_{{\rm ref}N}[n]$, such that the temperature of all phases is the same, minimizing the thermal stress. Those references are compared to estimates of the inductors currents $i_{\rm est1}[n]$ to $i_{estN}[n]$ obtained with the multiparameter self-tuning estimator. The resulting current differences $\Delta i_1[n]$ to $\Delta i_N[n]$ are then passed through current compensators to the multiphase digital pulsewidth modulator (DPWM) that, based on the input signals $d_1[n]$ to $d_N[n]$, creates modulating signals for all phases.

In addition, to accurately estimate phase currents, the estimator also extracts information about the total conduction losses, i.e., equivalent resistance, of each phase. The information about the losses is utilized for temperature monitoring and thermal equalization. Furthermore, the controller also extracts the values of power stage inductors and the output capacitor. The dual-mode compensator uses the *LC* values in its transient suppression algorithm, to achieve a response with virtually minimum output voltage deviation [26].

As described in the following section, the estimation of all parameters is based on the measurement of the input and output converter voltages, and on the inherently available duty ratio value only, while its self-calibration is performed with the help of a known current sink.

III. Self-Tuning Multiparameter Estimator

Fig. 2(a) and (b) explains the principle of operation of the conventional analog current estimator [13] and the self-tuning digital system introduced in this paper, respectively, on a single-phase dc–dc converter example. In the analog implementation, which is frequently used in low-power SMPS, the inductor current $i_L(t)$ is extracted by placing an *R-C* filter in parallel with the power stage inductor and measuring the filter's capacitor voltage $v_{\rm sense}(t)$. The relationship between the voltage and the inductor current is given by the following transfer function:

$$V_{\rm sense}(s) = I_L(s)\, R_L \frac{1+s(L/R_L)}{1+sR_fC_f} = I_L(s)\, R_L \frac{1+s\tau_L}{1+s\tau_f} \tag{1}$$

where L and R_L are the inductance and its equivalent series resistance values, respectively, and R_f and C_f are the values of the filter components. When the filter parameters are selected so that $\tau_f = R_fC_f = L/R_L = \tau_L$, the capacitor voltage becomes an undistorted scaled version of the inductor current (the zero and pole cancel each other) allowing the inductor current to be reconstructed from the capacitor voltage measurements.

As mentioned earlier, the main drawback of this method is that the inductor parameters are not exactly known and do change over time, often causing large errors in the estimation [14]. To minimize this effect, an analog filter with programmable resistive network is proposed in [16] and [17], where, in the latter publication, an on-chip implementation of the filter is shown. Even though the method significantly improves the estimator accuracy, its implementation still requires a relatively large number of external/passive components and the sensed current is still an analog signal, making it less suitable for integration with digital controllers.

In the estimator introduced here, the analog filter is replaced with a fully digital equivalent, where the digital filter is tunable, as shown in Fig. 2(b). The voltage across the inductor is converted into a digital value $v_L[n]$, and then, processed to result in the output $i_{\rm sense}[n]$ directly proportional to the average inductor current over one switching cycle.

By manipulating (1) and applying bilinear transformation [27], the following difference equation for the digital filter is derived:

$$\begin{aligned} i_{\rm sense}[n] &= \frac{v_{\rm sense}[n]}{R_L} \\ &= G\left\{c_1 R_L\, i_{\rm sense}[n-1] + c_2(v_L[n]+v_L[n-1])\right\} \end{aligned} \tag{2}$$

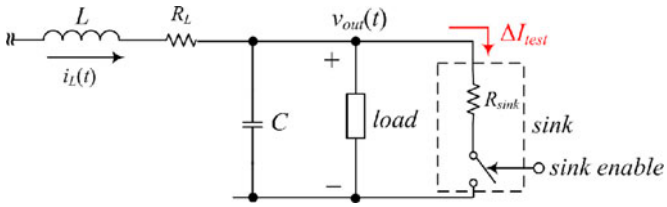

Fig. 3. Test current sink circuit used for the filter calibration.

where $G = 1/R_L$ is the estimator gain, and c_1 and c_2 are filter coefficients

$$c_1 = \frac{(2(L/R_L T_s) - 1)}{(1 + 2(L/R_L T_s))} \tag{3}$$

$$c_2 = \left(1 + 2\frac{L}{R_L T_s}\right)^{-1} \tag{4}$$

and T_s is the sampling rate. The estimator adjusts the filter gain and coefficients c_1 and c_2 through a self-calibrating process. It is obtained with a help of a test current sink connected to the converter output, as shown in Figs. 1 and 3. During brief calibration periods, the sink, implemented as a resistor with known value, takes a small portion of the nominal load current. Then, based on the response of the filter, the *self-tuning estimator* adjusts the filter gain and coefficients, so that the increase in $i_{\text{sense}}[n]$ corresponds to the exact increase in the load current. The calibration technique introduced here is similar to the one presented in [16], where a known test current is injected through the inductor during the converter start-up, to adjust an analog filter of a conventional *RC* current estimator [21]. However, the previously proposed current injection method requires both converter switches to be turned OFF during the calibration, making the procedure challenging to apply during regular converter operation. As a consequence, the estimation accuracy might be compromised, since the R_L and *L* vary with operating conditions [14].

In the method introduced here, the current sink of Fig. 3 does not require any change in converter operation allowing the calibration to be performed regularly, during closed-loop converter operation.

A. Gain and Time Constant Calibration

The proper values of the filter gain $G = 1/R_L$ and its time constant $\tau_f = \tau_f = L/R_L$ of (1)–(3) are determined from the estimator and the converter output voltage transient waveforms, caused by a single ON–OFF action of the test current sink. The waveforms of Fig. 4(a) and (b), which shows converter output voltage, inductor current, and the estimated average current over one switching cycle, demonstrate the gain and time constant adjustment procedure. Initially, the gain value is found and, in the following step, the time constant is determined.

To find the estimator gain, its output value is compared before and after the sink turn-ON transient, once the new steady state is reached. Those two points are labeled as A and B in the diagram of Fig. 4(*a*). At point B, which is selected long after the transient relative to the time constants τ_L and τ_f of (1), i.e., $T_{AB} > 5\tau_f$ and $T_{AB} > 5\tau_L$, the output of a well-tuned estimator should increase by $R_L \Delta I_{\text{test}}$, where ΔI_{test} is the known amplitude of the calibrating sink step. For the digital implementation of Fig. 2(b), this increase should be equal to the digital equivalent of ΔI_{test}. At the point B, the actual response of the estimator ΔI_m is measured and the proper value of the gain is calculated as follows:

$$G = \frac{1}{R_L} = \frac{\Delta I_{\text{test}}}{\Delta I_m} G_{\text{initial}} \tag{5}$$

where G_{inital} is the initial gain value.

In the system of Fig. 1, point A is selected during the time when error signal *e*[*n*] is zero over several cycles (indicating steady state) and point B is chosen when both the compensator and the filter of Fig. 2(b) reach steady state. At the end of this first phase of the calibration, the current sink is left in the ON-state consuming current ΔI_{test}.

B. Time Constant Calibration

Equations (1) and (2) indicate that the calibration of the gain *G* results in an accurate dc current measurement, but does not guarantee that the output of the estimator will follow the inductor waveform accurately. The variations in R_L and *L* values, due to operating conditions [14], external influences, and production tolerance affect the time constant τ_L (1), and therefore, result in a distortion of the estimator waveform.

The closed-loop calibration procedure of the time constant τ_F is based on the observation and, consequent, correction of the undershoot/overshoot in the estimator response to the transient caused by a turn-OFF of the test current sink. The procedure is demonstrated in Fig. 4(b), showing key waveforms of the converter (see Fig. 1) and the estimator for both an untuned and tuned cases. To find the value of the estimator undershoot/overshoot, its output is captured at the output capacitor voltage peak point (on the diagram labeled as D), where the instantaneous inductor and the load current of a closed-loop dc–dc converter are the same [28]. At this point, the output of a properly tuned estimator decreases by ΔI_{test}, corresponding to the drop in the output current due to the turn-OFF of the current sink. On the other hand, an out-of-tune filter, whose time constant differs from the actual inductor time constant $\tau_L = L/R_L$ exhibits undershoot or overshoot. To compensate for this, the estimated value is captured at the peak point D, and its increment is compared to the expected value ΔI_{test}. Accordingly, the time constant of the filter is adjusted as follows:

$$\tau_f = \tau_{f\_\text{initial}} \left(1 + \frac{\Delta I_{\text{peak}}}{\Delta I_{\text{test}}} \frac{1}{1 - (\Delta T_{\text{peak}}/2\tau_{f\_\text{initial}})}\right) \tag{6}$$

where τ_{f_initial} is the initially set filter time constant and ΔT_{peak} is the time distance between points C and D, i.e., the initial transient and the peak voltage points. Equation (6) [29] is derived based on the assumption that the sensed current changes in an exponential fashion, with time constant τ_{f_initial}, and Taylor's expansions of that waveform. In this case, the first three elements of the series are taken into account, i.e., $e^{-x} \approx 1 - x + x^2/2$, and the sensed and actual current step values equalized at the point $x = \Delta T_{\text{peak}}/\tau_{f\_\text{initial}}$.

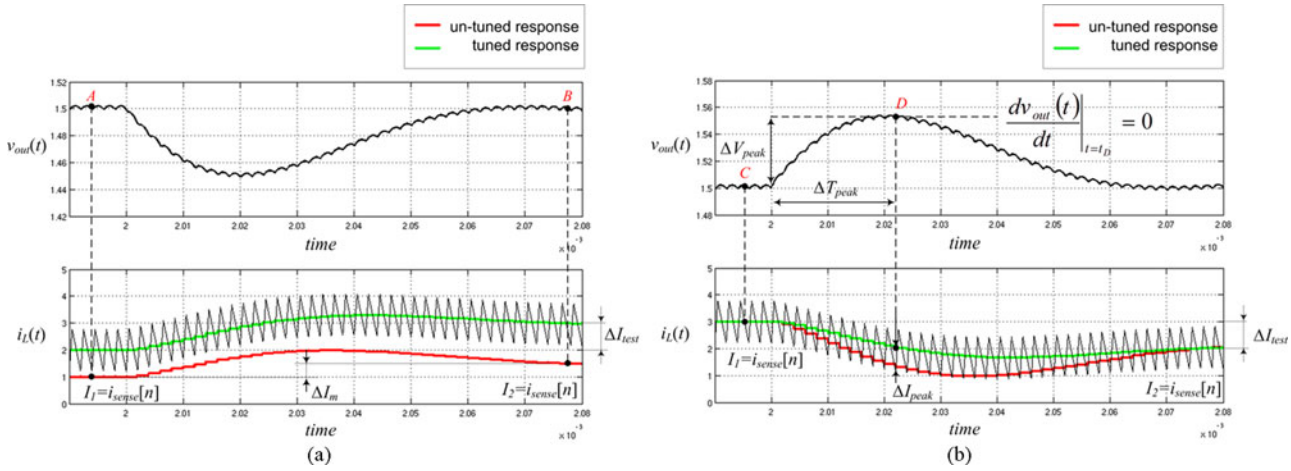

Fig. 4. Filter calibration procedure. (a) Gain calibration. (b) Time constant calibration.

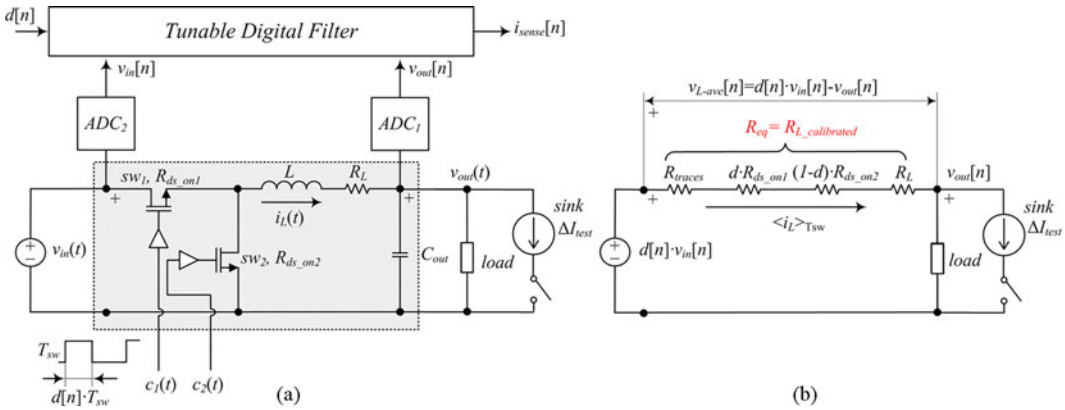

Fig. 5. Buck converter (a) and its steady-state dc equivalent circuit $R_{\rm eq}$ (b) used for current estimation.

It should be noted that the filter time constant tuning procedure presented here is significantly faster than previous iterative solutions [16], [17], [30], allowing one-step adjustment and consequent use of the estimator for overcurrent protection and monitoring in a dynamic environment.

C. Estimation of Conduction Losses

The gain calibration procedure described in the previous section inherently provides information about the inductor resistance (5), i.e., $R_L = 1/G$, allowing for the estimation of its conduction losses. To estimate not only the inductor conduction losses but also those of the switching components and printed circuit board (PCB) traces, the circuit of Fig. 2(b) is modified, as shown in Fig. 5(a). In this case, instead of measuring instantaneous voltage drop across the inductor, the average voltage (over one switching cycle) between the input and the output of the converter is measured. The modification effectively changes the series resistance connected to the inductor "seen" by the estimator, such that it also encompasses effects of the other losses. For a buck converter similar to that in Fig. 2(a), these losses can be represented with the dc equivalent circuit shown in Fig. 5(b), obtained by circuit averaging over one switching cycle [31]. In this figure, d is the converter duty ratio, $R_{\rm traces}$ represents the equivalent resistance of the PCB traces, while $R_{ds\_{\rm ON}1}$ and $R_{ds\_{\rm ON}2}$ are ON-state resistances of the main switch and synchronous rectifier, respectively.

Compared to the case described originally, the gain calibration procedure is not changed at all. However, the resulting gain of the estimator becomes

$$G = \frac{1}{R_L + d[n]R_{ds1\_\rm ON} + (1-d[n])R_{ds2\_\rm ON} + R_{\rm traces}} = \frac{1}{R_{\rm eq}}. \tag{7}$$

This value contains information of the total conduction losses, i.e., of the equivalent resistance $R_{\rm eq}$ of the entire converter. In the controller of Fig. 1, this value is used for the temperature monitoring of the converter components without utilization of costly temperature sensors, as described later.

In the following sections, it is also described that this modification not only allows estimation of the conduction losses and consequent thermal stress equalization but also drastically reduces hardware requirements for the ADCs of Fig. 1, further simplifying controller implementation.

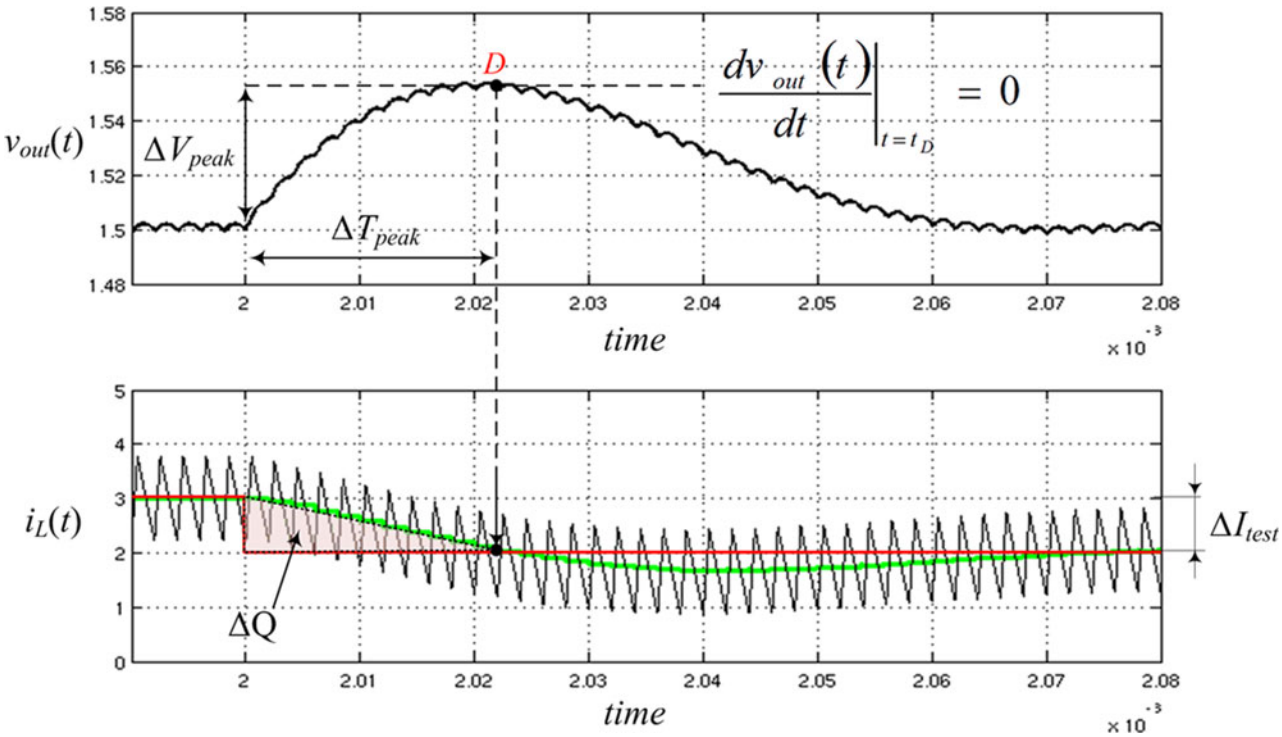

Fig. 6. Output capacitor identification procedure.

D. Power Stage Inductor and Capacitor Identification

In addition to estimate the inductor current and total conduction losses, at the same time, the estimator identifies values of the power stage inductor and capacitor. These parameters are utilized to obtain fast dynamic response of the controller approaching physical limitations of the powers stage, as shown in Section VI.

The inductor value L is simply calculated from the estimated total losses and the calibrated time constant of the filter as follows:

$$L = \tau_f R_{\text{eq}}. \tag{8}$$

During the filter time constant calibration procedure, the output capacitor value is also estimated, from the capacitor charge balance depicted with Figs. 4(b) and 6. At the peak point, labeled as D, the controller captures the time instant ΔT_{peak} and the amplitude deviation of the output capacitor voltage ΔV_{peak}. Based on these two values, the output capacitance is determined by equating the following two expressions:

$$\Delta Q = C\Delta V_{\text{peak}} \tag{9}$$

$$\Delta Q = \frac{1}{2}\Delta I_{\text{test}}\Delta T_{\text{peak}} \tag{10}$$

where, (9) represents the change of the capacitor charge, and (10) is the area shown in Fig. 6. This area is approximately equal to the excess of charge brought by the inductor current during the current sink turn-OFF transient. As a result, the following expression for the estimated capacitance is obtained:

$$C = \frac{\Delta I_{\text{test}}\Delta T_{\text{peak}}}{2\Delta V_{\text{peak}}}. \tag{11}$$

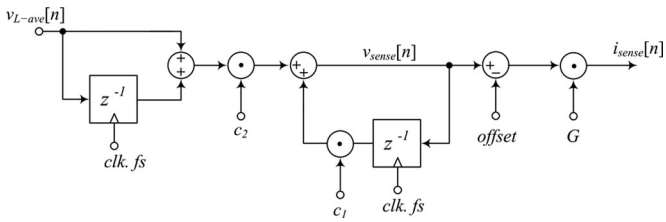

Fig. 7. Tunable digital IIR filter.

It should be noted that, in addition to using the estimate of LC for improving load transient response, the results of identification can also be used to monitor the converter stability margin, as shown in [32].

IV. Practical Implementation

Direct implementation of an estimator based on Fig. 2(b), which would reconstruct the instantaneous value of the inductor current, is challenging and, most probably, impractical for targeted cost-sensitive applications. It would require a very fast differential input ADC, theoretically with an infinite sampling rate, as well as an equally fast processor for the filter implementation. Hence, to reduce the hardware requirements, average inductor voltage over one switching cycle $v_{L\_\text{ave}}[n]$ is measured. Then, as shown in Fig. 7, this value is passed to an IIR tunable digital filter implementing (2), to obtain the average inductor current value.

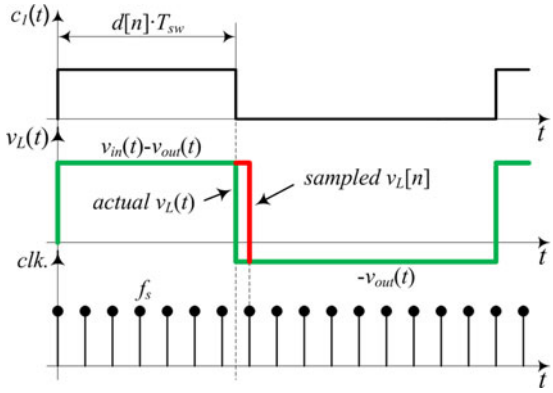

Fig. 8. Signals of a system implemented with an oversampling ADC.

A. Inductor Voltage Measurement

Direct measurement of the average inductor voltage still requires a differential-input ADC with a sampling rate significantly higher than the converter switching frequency. The need for a high sampling rate ADC can be explained by looking at Fig. 8, showing idealized inductor voltage of a buck converter, its gate drive signal $c_1(t)$, and the sampling signal of an oversampling ADC, labeled as *clk*. Here, it is assumed that the voltage is calculated by averaging the ADC samples over one switching period.

It can be seen that, due to a mismatch in synchronization, the state of the inductor voltage during switching transition happening in between two samples is not determined. As a consequence, an error in the average value calculation, proportional to the ratio of the sampling and averaging period, occurs. To minimize the error of this direct measurement approach, a very high-sampling rate differential ADC can be used. However, for low-power converters, operating at high switching frequencies, ranging from a fraction of megahertz to tens of megahertz, such an ADC represents a serious implementation obstacle [33], [34]. On the other hand, extension of the averaging process over several switching periods would slow down estimation process negatively affecting controller dynamic response and would delay reaction of the current protection.

To eliminate the need for a fast differential input ADC without sacrificing the speed of the estimation, the system of Fig. 2(b) is modified, as shown in Figs. 1 and 5(a). The input voltage of the power stage $v_{\rm in}(t)$ is converted into a digital equivalent $v_{\rm in}[n]$ with a slow ADC (in Fig. 1 labeled as $\rm ADC_2$), operating at a rate lower than the switching frequency, and the average value of the inductor voltage and current are estimated as follows:

$$\begin{aligned}\langle v_{L\_\rm estimate}[n]\rangle_{T_{\rm sw}} &= d[n]v_{\rm in}[n] - v_{\rm out}[n]\\ \langle i_{L\_\rm estimate}[n]\rangle_{T_{\rm sw}} &= G\left(d[n]v_{\rm in}[n] - v_{\rm out}[n]\right)\end{aligned} \tag{12}$$

where $d[n]$ is the DPWM's control variable and $v_{\rm out}[n]$ is the converter output voltage, both of which are readily available in the control loop of Fig. 1. The $v_{\rm out}[n]$ value is provided by the ADC of the voltage control loop and the duty ratio is given by the digital compensator. A lower sampling rate is possible because in most targeted dc–dc converter applications, the input voltage changes relatively slow.

B. Offset Calibration

In a realistic converter, the actual average inductor voltage usually differs from (12). Mostly due to a discrepancy between the actual, i.e., effective, duty ratio of the signal at the switching node (labeled as L_x in Fig. 2), and that issued by the controller $d[n]$. The difference is caused by the delays of nonoverlapping circuits, unbalanced timing of gate drivers, as well as, by the presence of voltage ringing at the switching node, due to the existence of a resonant circuit formed by parasitic components [35].

As a consequence, an offset between the estimate and the actual average value of the inductor voltage over one switching cycle $\langle v_{L\_\rm offset}\rangle_{T_{\rm sw}}$ exists. This offset can be expressed as follows:

$$\begin{aligned}\langle v_{L\_\rm offset}\rangle_{T_{\rm sw}} &= \frac{\langle i_{L\_\rm offset}[n]\rangle_{T_{\rm sw}}}{G}\\ &= \langle v_{L\_\rm actual}\rangle_{T_{\rm sw}} - \langle v_{L\_\rm estimate}\rangle_{T_{\rm sw}}\end{aligned} \tag{13}$$

where

$$\langle v_{L\_\rm offset}\rangle_{T_{\rm sw}} = d_{\rm eff}\, v_{\rm in}\,(t) - v_{\rm out}\,(t) \tag{14}$$

$d_{\rm eff}$ is the effective duty ratio value. This error in output voltage estimation also causes a proportional offset in the current measurement.

To eliminate the offset, a cancellation procedure is developed. The procedure relies on the fact that, in a steady state, a properly operating feedback always adjusts $d[n]$, so that

$$d_{\rm eff} = d[n] + \frac{\Delta t}{T_{\rm sw}} \tag{15}$$

is constant, where Δt models previously described delays of a realistic converter and is directly proportional to the offset. In other words, the controller regulates the converter output such that it keeps the effective duty ratio constant, compensating for all the delays existing in a realistic system.

To find the value $\Delta t/T_{\rm sw}$ and compensate for it, i.e., eliminate the offset

$$v_{L\_\rm offset} = \frac{\Delta t}{T_{\rm sw}} v_{\rm in}(t) \tag{16}$$

a dual-frequency operation-based offset cancellation procedure utilizing (15) is developed. In the procedure, the switching frequency of the converter is temporarily increased to $2f_{\rm sw}$ resulting in a new controller duty ratio value

$$d_{hf}\,[n] = d_{\rm eff} - \frac{2\Delta t}{T_{\rm sw}} \tag{17}$$

and this value is compared to the controller value at the nominal frequency (15).

By eliminating $d_{\rm eff}$ from (15) and (17), the offset is calculated as follows:

$$\frac{\Delta t}{T_{\rm sw}} = d[n] - d_{hf}[n] \tag{18}$$

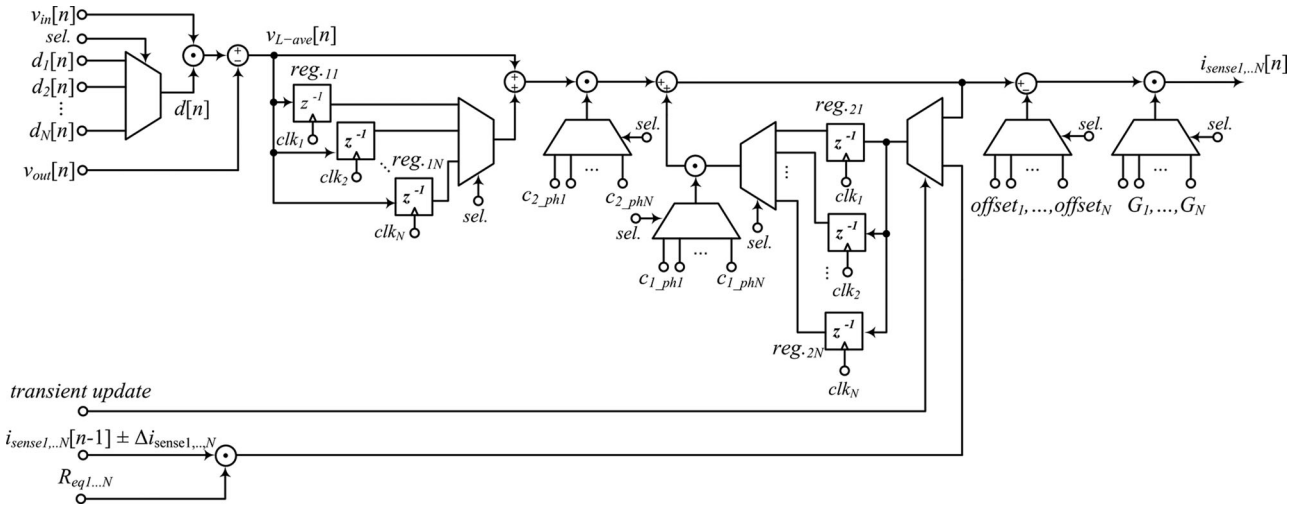

Fig. 9. Tunable IIR estimator filter for an *N*-phase converter.

and

$$v_{L\_\mathrm{offset}} = (d[n] - d_{hf}[n])\, v_{\mathrm{in}}[n] \tag{19}$$

and, by replacing (19) into (13), we obtain

$$i_{L\_\mathrm{offset}} = i_{L\_2f\mathrm{sw}} - i_{L\_f\mathrm{sw}} \tag{20}$$

where $i_{L\_2f\mathrm{sw}}$ and $i_{L\_f\mathrm{sw}}$ are results of frequency estimation for the operation at two times the switching and the switching frequency, respectively.

This simple equation is implemented to calculate the offset calibration value for the system of Fig. 6.

C. Multiphase Operation

To extend the operation of the estimator to multiphase converters without a significant increase in hardware complexity, the system of Fig. 6 and tuning procedure are slightly modified, such that the same ADCs and current sink are shared between all the phases. Furthermore, in this modification, shown in Fig. 9, the same set of adders and multipliers process individual phase parameters, which are separately determined through a step-by-step calibration procedure described in Section IV-C. The individual parameters are sent to common elements through a set of multiplexers, as shown in Fig. 9.

1) Step-by-Step Calibration Procedure: The inductor parameters, i.e. *L* and R_L, and other resistive losses usually vary from phase to phase, both in the cases, when the phases are intentionally sized in a nonuniform manner [5] and when an identical design for all of them is targeted. This implies that the previously described multiparameter estimation procedure needs to be conducted for each of the phases. Multiphase operation also requires a modification in the current-sink-based self-calibrating procedure described in the previous section.

Due to the differences in the equivalent resistances of individual phases, for an untuned system, the current step is likely to be shared in an unknown manner, even if the phases are designed equally [18], [19]. Hence, no reliable information about the current increase per phase, which is a key parameter for the estimator, can be obtained by directly applying the previously described single-phase procedure.

To solve this problem, a phase-by-phase calibration procedure of the system shown in Fig. 1 is applied. In this procedure, during the current sink action, the currents of all phases but the one under the calibration are "frozen," by allowing only the control signal $i_{\mathrm{ref}}[n]$ of the phase under calibration, i.e., phase *k*, to change while keeping all the others at their precalibration values. As a result, only the current in the active phase increases by the value equal to that of the current sink, allowing the estimation process to be conducted as for the single-phase case. The obtained set of parameters for the phase *k* is then passed to the corresponding inputs and registers of the system shown in Fig. 8, and the procedure is repeated for all the other phases.

V. Current Sharing Based on Thermal Stress Equalization

This section demonstrates how the new estimator can be utilized to improve the reliability of multiphase converters by minimizing thermal stress through current sharing, without the use of dedicated thermal sensors.

In dc–dc multiphase low-power converters with identically designed converter phases, most frequently, the load current is either shared equally [3] or such that the maximum efficiency of the converter is obtained. In the later case, peak efficiency is obtained by precisely matching the duty ratio control values of all of the phases [18]. In practice, such precise matching is challenging to achieve due to the variations in the time delays of gate drive circuits and other parasitic delays [19].

From the reliability point of view, neither of the two previously mentioned methods is a favorable solution. In both cases, parasitic resistance, mismatches of power switches, and board traces result in significantly higher power losses (temperature) for some phases. This is demonstrated in Fig. 10, showing dependence of the temperature on the mismatch in equivalent phase resistances for a commercial two-phase 35 A/phase converter. It can be seen that, even when the mismatches are

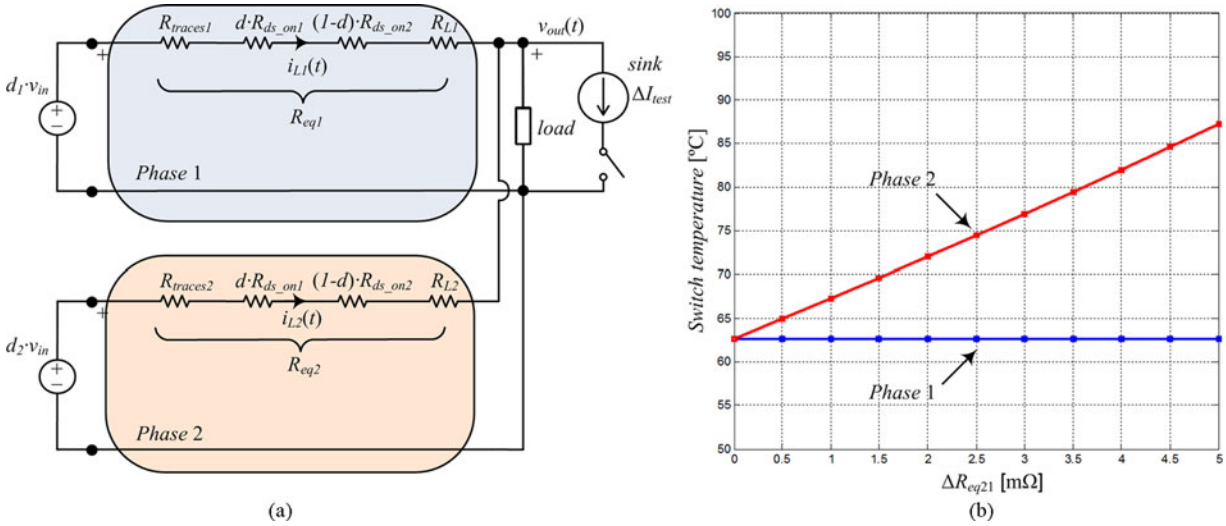

Fig. 10. DC-equivalent circuit of a two-phase converter and a diagram of the temperature dependence on the mismatch in the equivalent resistance values.

relatively small, the phases with higher losses become significantly warmer than the others.

This temperature difference is a serious reliability problem. It causes shear (mechanical) stress due to the mismatch in the thermal expansions of the warmer and colder parts [36], [37] of the converter circuit. Since converters usually go through frequent thermal cycles, depending on the load variations, this mismatch leads to accelerated aging and premature mechanical failures [36]. As shown in [37], this mechanism is one of the most frequent reasons of failures in modern electronic devices.

In the previous art [21], [22], systems with dedicated thermal sensors measuring the temperature of critical components of each phase are utilized, to minimize thermal stress. The sensors provide information about the temperature of each phase to a modified current loop, whose task is to equalize the phase temperatures. Even though, the presented systems significantly reduce the thermal stress, they have only found application in very specialized low-volume highly reliable systems. The presented thermal-sensor-based implementation has not been widely accepted in the targeted cost-sensitive low-power applications, due to the increased component count, size, and circuit complexity.

To eliminate the need for the external temperature sensors, the controller presented here utilizes results of the previously described equivalent resistance estimation (11). It equalizes the thermal stress of the phases by balancing the sources of the temperature mismatch, i.e., phase conduction losses. This is performed with the current sharing logic block of Fig. 1, which sets the reference for the current loop, such that the following sharing is obtained:

$$R_{\mathrm{eq}1} I_{L1}^2 = R_{\mathrm{eq}2} I_{L2}^2 = \ldots = R_{\mathrm{eq}N} I_{LN}^2 \qquad (21)$$

and, consequently, the temperature mismatch is eliminated.

It should be noted that, since the inherent property of the method introduced here is that it controls the sources of the temperature mismatch instead of temperature, it is able to reduce several other problems of the temperature-sensor-based solutions. Namely, the new controller eliminates potential stability problems related to latency in temperature measurements. The latency caused by relatively large temperature time constants of the measured devices, compared to the changes of conditions in the converter circuit, can cause a significant delay or even incorrect action of a temperature-matching controller during frequent load changes. Since the introduced system has virtually immediate information about the current and can perform parameter estimation at a much faster rate, it minimizes the latency problem. The presented solution is also able to minimize problems with rapid overheating of components that, in methods based on surface temperature measuring [21], [22], is detected only after the internal parts are already overheated or damaged. Furthermore, this implementation eliminates problems of faulty temperature sensor readings impacted by the surrounding components, PCB layout, and airflow.

VI. Transient-Mode Controller

The transient-mode compensator introduced here, which is a part of the dual-mode voltage compensator of Fig. 1, utilizes estimated *LC* output filter parameters to achieve a fast transient response. It combines dead-beat algorithm [25] with the capacitor-charge balance principle [28] to achieve response with virtually minimum output voltage deviation and recovery in two switching cycles.

After detecting a significant load current change ΔI_{load}, the transient compensator overrides the operation of a conventional proportional-integral compensator and recovers to new steady state in two switching cycles, as shown in Fig. 11. In the first switching cycle, it matches the sum of the inductor currents with the new load value and, in the following cycle, it replaces the lost capacitor charge, recovering the output voltage.

Like systems shown in [28] and [38], the load change is calculated by observing the time derivative, i.e. difference, of the output capacitor voltage between two samples $e[n-1]$ and $e[n]$

$$\Delta I_{\mathrm{load}} = C \frac{\Delta v_{\mathrm{slope}}}{\Delta t} = C \frac{e[n] - e[n-1]}{T_{\mathrm{sample}}} \qquad (22)$$

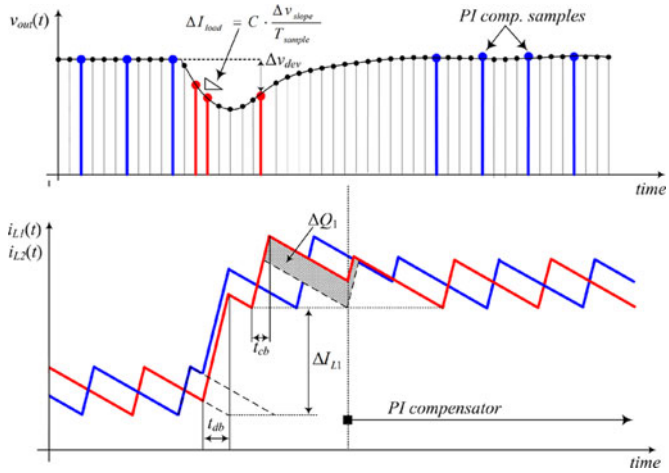

Fig. 11. Transient-mode operation.

where $\Delta v_{\rm slope}$ is the slope of the output voltage, $T_{\rm sample}$ is the sampling period, and C is the output capacitance. This value is used to calculate the ON and OFF times of the main switches resulting in the sum of all phase inductor currents to be the same as the new load current. The calculation is performed using a digital dead-beat algorithm [25], providing dead-bit control time $t_{\rm db}$. For the multiphase buck converter, the dead-beat times for light-to-heavy and the opposite transient are given with the following expressions:

$$t_{\rm db\_1} = \frac{L_{\rm eq}}{v_{\rm in} - v_{\rm out}} \Delta I_{\rm load} \tag{23}$$

$$t_{\rm db\_2} = \frac{L_{\rm eq}}{v_{\rm out}} \Delta I_{\rm load} \tag{24}$$

where $L_{\rm eq} = L_1||L_2||...||L_N$ is the equivalent inductance of all converter phases connected in parallel.

At this point, the average load and inductor currents are matched, but the output voltage is still not at the reference. To compensate for this, at the end of the first switching cycle, the voltage deviation $\Delta v_{\rm dev}$ is captured and the lost charge (ΔQ_1 for phase 1, etc.) is calculated from the charge balance principle [28], [39], based on the known capacitance and the sampled voltage deviation. This is then used to calculate the ON-time (t_{cb_1}) or OFF-time (t_{cb_2}) for the second, voltage recovery, cycle. It should be noted that this sampling point is determined only by the end of the first switching cycle, and generally, does not coincide with the peak/valley point of the output capacitor voltage. This eliminates the need to accurately detect the point, where the capacitor current changes sign [40], i.e., the peak or valley point [28], which is a hardware demanding process requiring a high sampling rate ADC or a fast detection circuit [26].

VII. Experimental Systems and Results

Based on the diagrams of Figs. 1, 5(a), and 7, two experimental systems are designed to verify the operation and various features of the novel sensorless controller and multiparameter estimator. First, the functionality, accuracy, and the dynamic performance of the estimator are tested with a single-phase 15 W, 1.5 V, 500 kHz buck converter prototype, with input voltage ranging between 2 and 6.5 V. This prototype is also used to demonstrate sensorless current and temperature protection features. Then, the current sharing based on the thermal stress equalization and load transient performances are demonstrated on a two-phase, 12 to 1.8 V, 80 W buck prototype, also operating at a switching frequency of $f_{\rm sw} = 500$ kHz.

TABLE I
Gate Counts of the Multiphase Controller Blocks and Silicon Area Estimates

Design Block	Area [mm^2]	Number of gates
PI compensator	0.051	1767
Current sharing logic	0.017	632
Two-phase current estimator	0.080	2716
Current compensators	0.022	830
Transient compensator	0.075	2643
Current estimator tuning logic	0.172	6168
Two-phase DPWM (8-bits resolution)	0.021	854
Total (digital blocks)	0.438	15610

The dual-phase controller is designed using a field-programmable gate array (FPGA) based development board and two ADCs for input and output voltage measurements, with respective quantization steps of 4 and 16 mV. The input voltage is sampled at $f_{\rm sw}/8$ and the output at a modest rate of $8f_{\rm sw}$, which is significantly lower than the rate of time-optimal solutions presented in [40]. The number of gates needed for the implementation of each functional block is given in Table I. The table also shows an estimate of the equivalent silicon area needed for the implementation of each of the blocks in a standard 0.18 CMOS process, commonly used in the targeted applications. The size estimate is obtained by exporting the complete design into an automated IC design tool and measuring the dimensions of the created components.

It can be seen that the complete digital logic takes less than 16 000 gates and can be implemented on a smaller than 0.45 mm^2 silicon area. Taking into account that application specific ADCs [33], [34] can be implemented on a less than 0.1 mm^2 [34], it can be estimated that the entire controller could be implemented on a less than 0.6 mm^2 of silicon. This area is no larger than that needed for the implementation of standard analog controllers [41] without any additional features. The result confirms that the controller and estimator architectures introduced here are hardware efficient and, as such, suitable for on-chip implementation in the targeted cost-sensitive applications.

A. Functional Verification

Fig. 11 and its zoomed parts, Figs. 12–14, and 16, demonstrate closed-loop operation of the single-phase system during self-tuning process and its effect on the measurement accuracy. The calibration is performed with the help of a current sink that introduces a 1-A current step equivalent to a 10% of the maximum load.

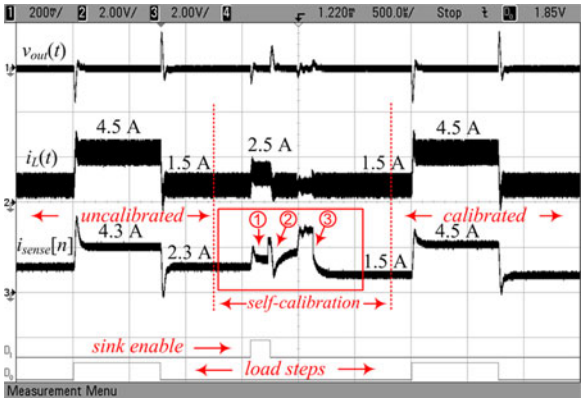

Fig. 12. Closed-loop self-tuning of the controller. Ch1: Output converter voltage (200 mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D_0–D_1: load step and sink enable signals; and time scale is 500 μs/div.

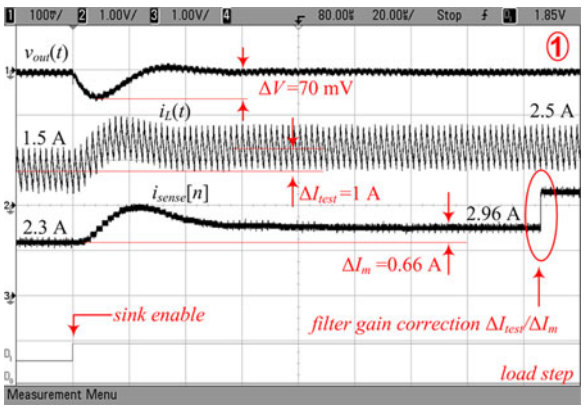

Fig. 13. Gain calibration process. Ch1: Output converter voltage (100 mV/div); Ch2: actual inductor current $i_L(t)$–2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D_0–D_1: load step and sink enable signals, and time scale is 20 μs/div.

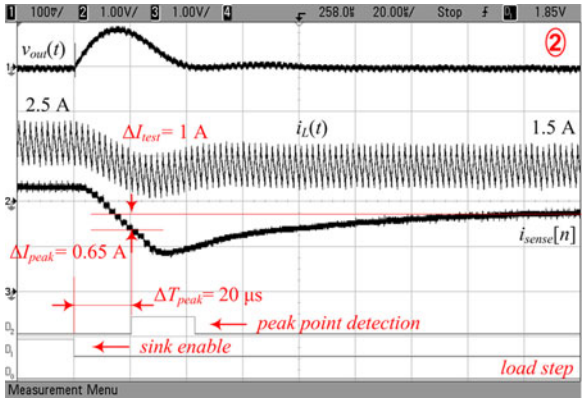

Fig. 14. Filter time constant calibration procedure for $\tau_f = 0.5\tau_L$. Ch1: Output converter voltage (100 mV/div); Ch2: actual inductor current $i_L(t)$–2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D_0–D_1: load step and sink enable signals; and time scale is 20 μs/div.

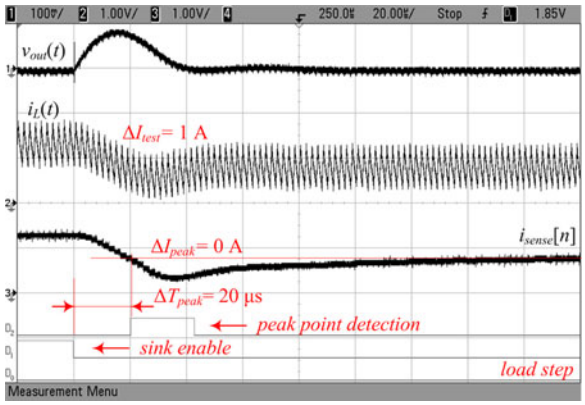

Fig. 15. Operation with calibrated gain and time constant. Ch1: Output converter voltage (100 mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D_0–D_1: load step and sink enable signals; and time scale is 20 μs/div.

In Fig. 12, the response of the controller and estimator to a 3-A load change, prior and after the self-calibration, is demonstrated. The response is divided into three distinctive regions, labeled as uncalibrated, self-calibration, and calibrated operation. The waveforms show actual inductor current and its estimation that, for visualization purpose, is presented by passing the digital signal $i_{\mathrm{ref}}[n]$ (see Fig. 1) through a fast digital-to-analog converter (DAC). It can be seen that the uncalibrated system produces inaccurate average current estimate, erroneously measures the size of the load step, and produces transient waveforms that are significantly different from the actual ones. As described in Section II, the self-calibration consists of three steps: gain and time-constant adjustments, followed by the offset calibration. In Fig. 15, the steps are labeled with numbers 1 to 3, respectively.

1) Gain Calibration: The gain calibration, which as described in Section II-b, which also gives an estimate of the conduction losses (7), is shown in Figs. 12 and 13 (zoomed view). It can be seen that, after applying a 1-A calibrating current step by the sink, error in the initial gain estimation is detected, through a faulty representation of the increment (0.66 A instead of 1 A) and, consequently, corrected, in accordance with the previously described procedure.

2) Time Constant τ_f Calibration: A zoomed-in view of time constant τ_f calibration and a simultaneous L estimation process, performed during transient following turn-OFF of the current sink, is shown in Fig. 14. By comparing the current estimate with the actual current drop at the output voltage peak, τ_f is also calibrated. During the same process, the output capacitor value is estimated from the output voltage deviation, as described in Section II-c. In this case, to test the tuning performance, the initial value of the time constant is set to be a half of the actual one, i.e., $\tau_f = 0.5\tau_L$. It can be seen that, at the peak point, the output current is not equal to the expect 1 A value and that the estimate shows a larger undershot. Fig. 15 shows results of an additional test (not a part of the tuning procedure shown in Fig. 12) used to verify a proper time constant tuning. It demonstrates response of the same estimator after the calibration procedure is completed and another 1-A step-down change of the output current is performed. The estimated current waveforms accurately following the shape of the inductor current confirm that the time-constant calibration procedure is effective.

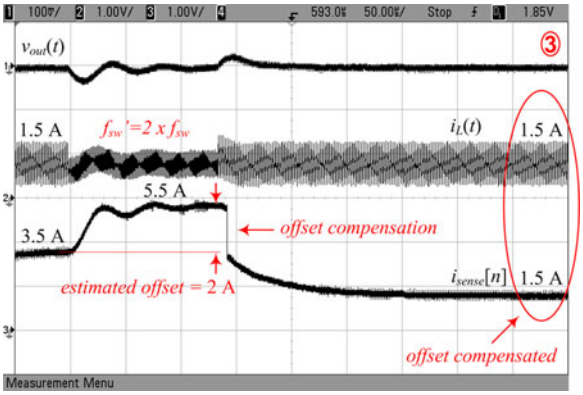

Fig. 16. Offset calibration procedure. Ch1: Output converter voltage (100 mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; and time scale is 50 μs/div.

3) Offset Calibration: Fig. 16 shows zoomed-in view of the offset calibration procedure. Even though the filter gain and time constant are adjusted in the previous two correction steps, the estimator still exhibits a large offset (showing 3.5 A instead of 1.5 A) prior the offset calibration. As described in Section IV-b, this offset, caused by the discrepancy between the actual and controller-issued duty ratio, is cancelled through the proposed two-frequency-based calibration. In the first step, the switching frequency is increased two times and the resulting change in the estimation (i.e., offset value) is measured. It can be seen that, the offset is increased by an additional 2 A. Based on (19) and (20), this offset is calculated and automatically cancelled by the controller.

B. Estimation Speed and Accuracy

Fig. 17 shows operation of the tuned system during load transients. It can be seen that the estimate of the average inductor current closely follows the actual value. The results also show that the delay of the estimator is only one switching cycle allowing the system to be used for overload protection and for obtaining fast dynamic response of the controller as demonstrated later.

Experimental results demonstrating how the estimator can be used for the overload protection are shown in Fig. 18. The overload protection is set to shut down converter when the estimate exceeds a threshold value, which in this case is set to 7 A. To test the protection, a sudden load change from 2 to 7.5 A is applied. It can be seen that the protection quickly interrupts operation of the converter preventing potential damages.

1) Accuracy of Current Estimation: The worst case analysis of the system accuracy [29], obtained through partial deviation of (12), shows that the measurement error is a function of the ADCs resolution, size of the output capacitor, and the current step introduced by the test sink. It predicts that, for the selected experimental system parameters, about a 5% error in the estimation can be expected.

These results are confirmed by Fig. 19, showing the relative measurement error, over the full range of operation of the single-phase system. It can be seen that, over the 10% to 100% load range, the relative error is less than a 6% and that absolute error never exceeds 0.5 A.

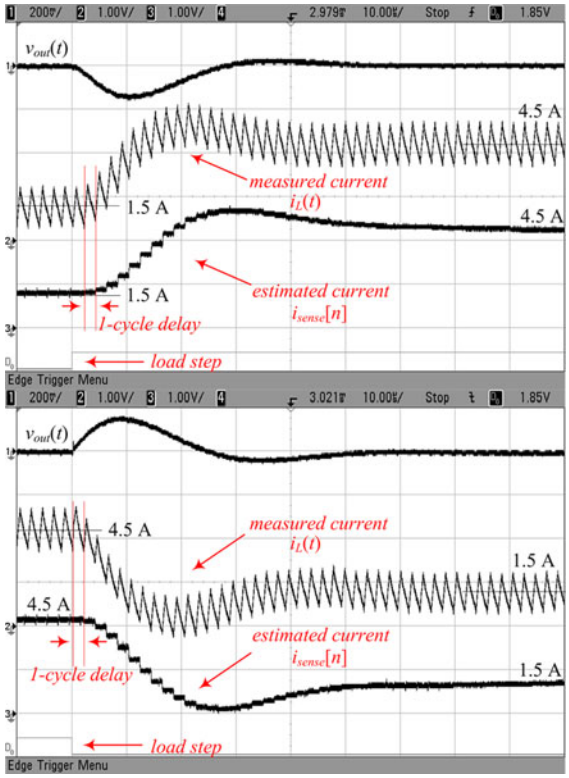

Fig. 17. Inductor current and its estimate during 3 A light-to-heavy and heavy-to-light load transients. Ch1: Output converter voltage (200 mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; and time scale is 10 μs/div.

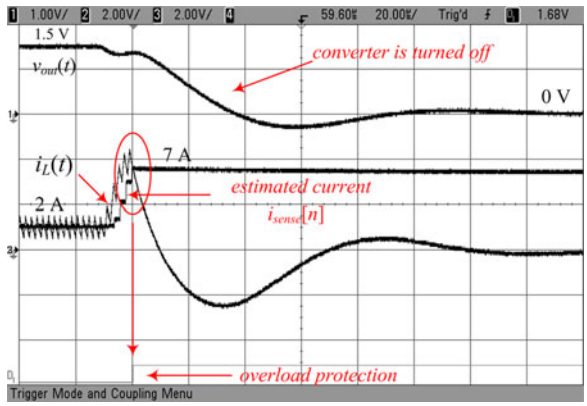

Fig. 18. Overload protection. Ch1: Output converter voltage (1 V/div); Ch2: actual inductor current $i_L(t)$, scale 2 A/V; and Ch3: estimated average current $i_{\text{sense}}[n]$, scale 2 A/V.

2) Temperature Monitoring and Protection: As mentioned earlier, the multiparameter estimator can also be used for remote sensorless temperature monitoring and protection. To obtain approximate information about the components temperature, the equivalent resistance of the single-phase power stage is estimated, as described in Section II-C. The results are then compared with a lookup table stored data containing relations between the equivalent resistance and temperature of the

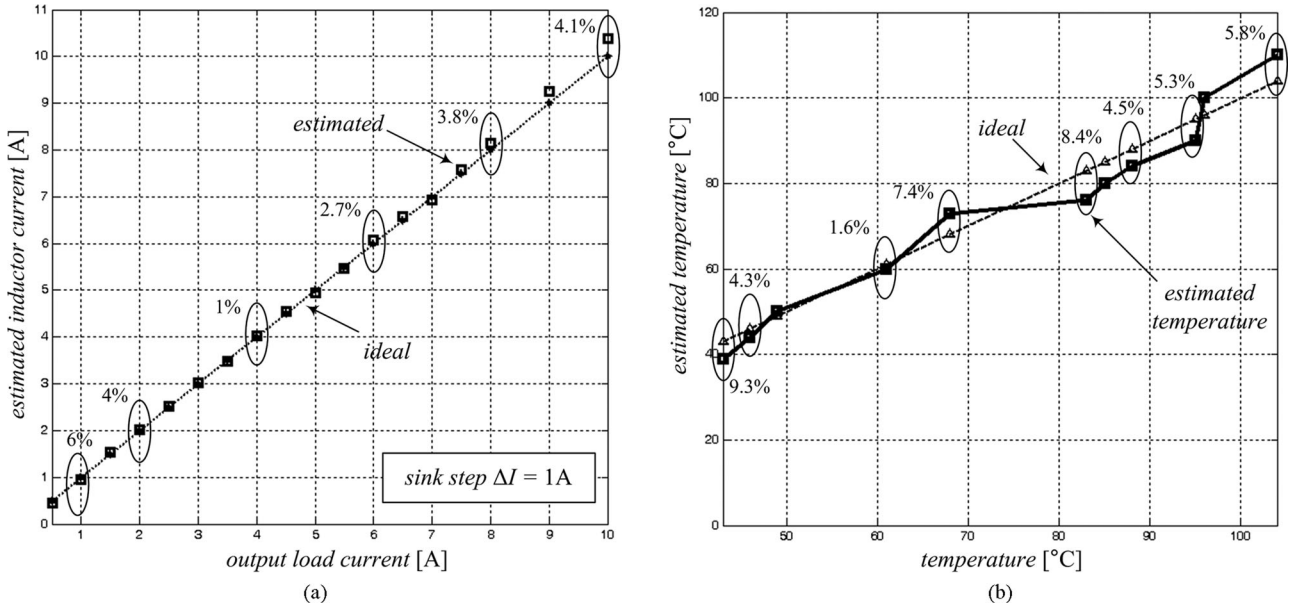

Fig. 19. Relative error of the current (a) and temperature (b) estimation.

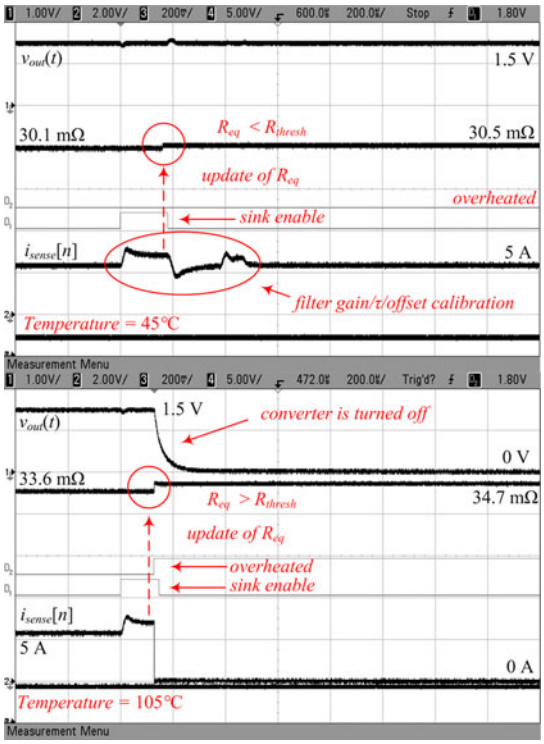

Fig. 20. Operation of the thermal protection. Ch1: Output converter voltage (1 V/div); Ch2: estimated steady-state current $i_{\rm sense}[n]$ – 2 A/V; Ch3: estimated $R_{\rm eq}$ – 1 mΩ/32.5 mV; Ch4: MOSFET temperature – 25 °C/V; and D_1–D_2: sink enable and overheating flag signal. Time scale is 200 μs/div.

components, provided by components manufacturers. The accuracy of the estimation is tested such that the power stage is intentionally heated and the estimated temperature of the components is compared with actual measurements. Fig. 19(b) shows the estimation error over a 50 °C temperature change. The results confirm that fairly accurate temperature estimation with an error less than 10% over the full range is obtained.

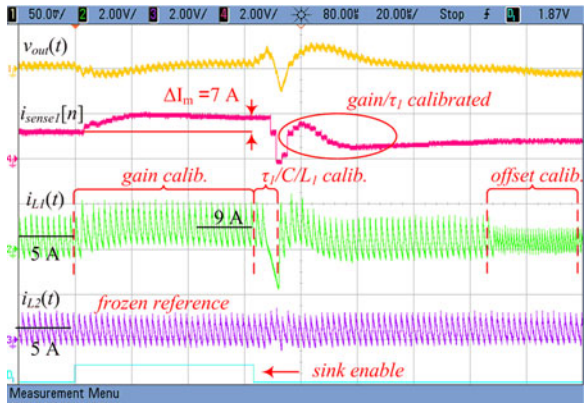

Fig. 21. Current estimator tuning and component identification with the multiphase converter. Ch1: Output converter voltage (50 mV/div); Ch2: actual phase 1 inductor current $i_{L1}(t)$ – 10 A/V; Ch3: actual phase 2 inductor current $i_{L2}(t)$ – 10 A /V; Ch4: estimated current $i_{\rm sense1}[n]$ – 10 A/V; and D_1: sink enable signal. Time scale is 20 μs/div.

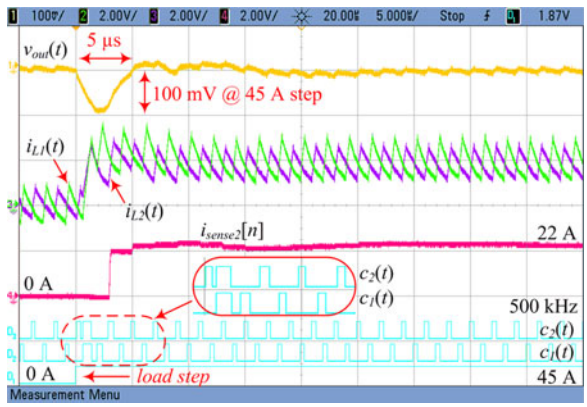

Fig. 22. Transient response of the nonlinear average current-mode controller. Ch1: Output converter voltage (50 mV/div); Ch2: inductor current $i_{L1}(t)$ – 10 A/V; Ch3: inductor current $i_{L2}(t)$ – 10 A/V; Ch4: estimated phase 2 current $i_{\rm sense2}[n]$ – 10 A/V; and D_1–D_3: sink enable and control signals. Time scale is 5 μs/div.

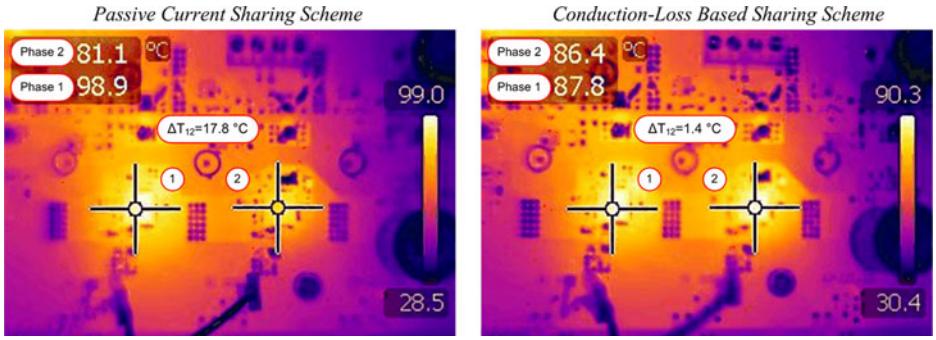

Fig. 23. Thermal images for equal duty ratio based (left) and conduction-loss-based (right) current sharing.

This feature is utilized for temperature protection of the power stage, as demonstrated in Fig. 20. A threshold for the equivalent resistance corresponding to the maximum allowable temperature is set (34 mΩ corresponding to 100 °C for the tested converter) and the temperature of the power stage is increased from 45 °C to 105 °C. During the monitoring, the test current sink is activated periodically, and based on the subsequently estimated resistance, the temperature is determined. It can be seen that the remote temperature monitoring recognizes overheating conditions and attempts to protect components by turning OFF the power stage and sending a flag signal.

C. Multiphase Operation and Thermal Stress Equalization

Figs. 21–23 verify operation of the estimator with the two-phase buck converter prototype described at the beginning of this section. Fig. 21 shows step-by-step calibration process, where during the self-tuning, the current of the phase that is not under calibration is kept constant and the parameter estimation is performed for the active phase only, as described in Section IV-C. In this case, a 4-A current sink is used for calibration.

During the calibration, output capacitance and the inductances of both phases are determined too, and used for obtaining minimum deviation response described in Section VI. Experimental results demonstrating dynamic response of the system for a zero-to-full load change are shown in Fig. 22. Results confirm that the proposed controller achieves small output voltage deviation and recovery to the new steady state in two switching cycles.

1) Thermal Stress Equalization: Fig. 23 shows thermal images of the converter prototype when the full-load current is shared based on commonly used equal duty ratio, i.e., maximum efficiency, approach, and when the sharing is based on the thermal stress equalization, described in Section V. A comparison of the results verifies that the multiphase parameter estimator and related control method significantly reduce thermal stress (for the experimental system by more than 16 °C) minimizing influence of one of the most common failure mechanism.

VIII. Conclusion

A sensorless self-tuning digital averaged CPM controller for low-power high-frequency SMPS is introduced. The key novel element of the controller is a self-tuning multiparameter estimator that, besides accurately measuring the average value of the inductor current over one switching cycle, also estimates converter parameters, such as filter components and equivalent conduction losses.

The estimation is based on the well-known *RC*-filter-based principle by replacing the analog filter with a self-tuning fully digital equivalent. In the self-calibration process, a current sink is used. Duty ratio information, inherent in the feedback loop, is used to minimize the requirements for a costly high sampling rate ADC needed for the acquisition of fast changing inductor voltage waveform. DC offset in estimation caused by errors and system delays is cancelled using a novel dual-frequency algorithm.

The estimated equivalent series resistance is used for remote temperature measurements and protection without costly thermal sensors. The controller also combines results of current and the resistance estimation to automatically provide current sharing based on the equal thermal stress minimizing the influence of a frequent failure mechanisms. The newly proposed implementation of equal thermal sharing not only eliminates the need for the dedicated thermal sensors but also eradicates large delays associated with temperature measurements causing potential stability problems. Furthermore, since the sharing is based on the calculation of the power losses (i.e., sources of the temperature rise), the implementation also minimizes the influence of external factors, such as airflow and the presence of other heat sources.

The *LC* estimation results are used in a fast transient-mode controller for obtaining virtually minimum possible output voltage deviation during load transients and recovery to steady state in two switching cycles. Compared to time-optimal methods, the presented two-cycle procedure reduces sampling requirements for the output voltage ADC further reducing hardware requirements.

The operation of the controller and the multiparameter estimator are verified with single-phase and dual-phase converter prototypes, demonstrating accurate current estimation, fast dynamic response, and effective minimization of the thermal stress. The FPGA implementation of the controller shows that it takes a small number of logic gates and, as such, is well suited for on-chip implementation with prospective silicon area no larger than that occupied but the existing analog solutions implementing only the basic feedback loop.

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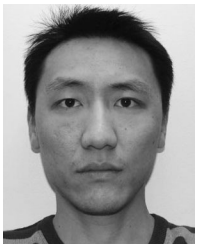

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