Letters

Buck Converter With Merged Active Charge-Controlled Capacitive Attenuation

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***Abstract*—This letter introduces a converter and a complementary digital controller that, compared to conventional buck, have a smaller output filter volume, improved dynamic response, and lower switching losses. To reduce the volume and switching losses, the input-to-output voltage difference is decreased with a capacitive attenuator that replaces the input filter capacitor and has approximately the same volume. Both the attenuator and the downstream buck converter share the same set of switches, minimizing conduction losses. A single digital controller governs operation of the both stages. The controller utilizes the inductor current to regulate the center tap voltage, through a charge-control algorithm. During transients, the attenuator is bypassed, so the inductor current slew rate is improved. Experiments with a 5–1.5-V, 2.5-A, 1-MHz prototype show that, compared to the conventional buck, the merged topology has 43% smaller inductor, 36% smaller output capacitor, up to 30% lower power losses, and a 25% faster transient response.**

***Index Terms*—Digital control, low-power switch-mode power supplies (SMPS), and small volume.**

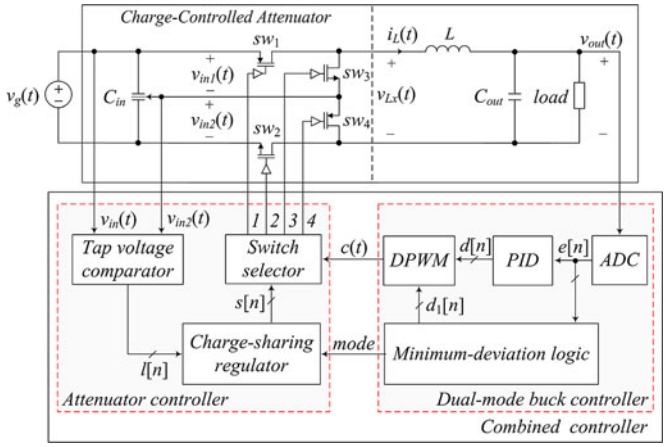

Fig. 1. Buck converter with active charge controlled input attenuator and corresponding digital controller.

I. Introduction

THE miniaturization of dc–dc switch-mode power supplies (SMPS) is of a key importance in portable devices, such as cell phones, tablet computers, and other volume-sensitive applications. In these systems, the SMPS often occupies more than 25% of the overall device size, where the filter components are contributing the most [1]. The reduction in the filter size is usually achieved by increasing the switching frequency [2]. The main drawback of this approach is an increase in switching losses that often nullify the effects of the filter miniaturization, due to increased cooling requirements.

The volume reduction has also been realized with inductorless switch-capacitor (SC) converters [3]–[7]. Compared to a conventional SMPS, the SC requires smaller reactive components and offers improved efficiency over a certain conversion range [4]. However, the absence of the inductor that stores energy during voltage variations [8] causes voltage regulation problems preventing a wider use of SC converters. To tightly regulate the output while maintaining high efficiency over a wide operating range, variable frequency control and/or multiple power stages increasing the system size are proposed in [3]–[7]. In [9] and [10], an SC and a buck converter are combined to minimize the size of filtering components without facing the voltage regulation difficulties. In addition to minimizing the buck filter, those solutions also have lower switching losses, due to reduced blocking voltages of the switches [2]. The topologies consist of a straightforward serial connection of an SC stage and a downstream buck that are regulated with two separate controllers. Besides increasing the controller complexity, those two-stage solutions also introduce a significant number of extra switches in the conduction path compared to the conventional buck.

The main goal of this letter is to introduce a buck converter with merged capacitive attenuator (BCMCA) and a complementary digital controller in Fig. 1. Compared to the other two-stage solutions [9]–[11], the BCMCA has a smaller number of switches, a simpler unified controller, and a faster transient response, allowing further filter reduction.

The BCMCA has some resemblance with the two-stage structures [9]–[11]. However, unlike the other systems, the converter in Fig. 1 does not require an extra flying or output capacitor and shares the same set of switches between the two stages minimizing their total number to four compared to at least six required for the previous solutions. A single digital controller regulates the output voltage and keeps the attenuator output constant, through a novel active-charge algorithm executed by the *Charge-sharing regulator*. The steady-state output regulation is performed with an analog-to-digital converter, a PID regulator, and a digital pulsewidth modulator. To suppress transients, the

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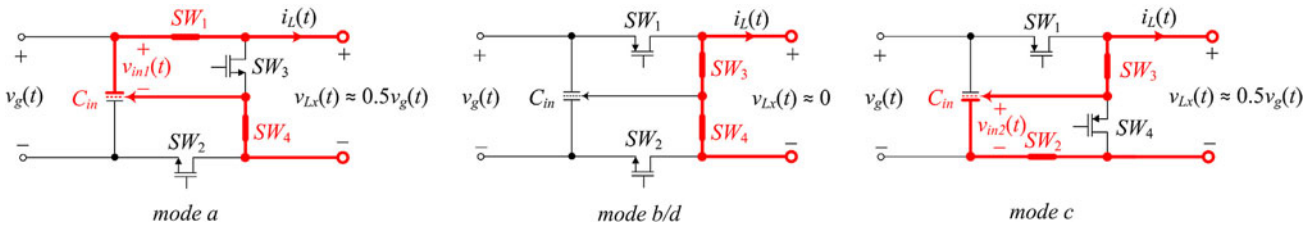

Fig. 2. Steady-state modes of operation of the BCMCA.

controller employs the minimum-deviation method [12] using *Minimum-deviation logic*. During transients, it also increases the slew rate of the inductor voltage, by bypassing the attenuator, largely improving dynamic performance.

II. Principle of Operation and System Description

The main purpose of the charge-controlled attenuator in Fig. 1 is to reduce the difference between the input and output voltage of the downstream buck converter and, in that way, reduce the output filter. Quantitatively, this effect can be described by looking at the expression for the inductor current ripple of a buck converter [2]

$$\Delta I_{\text{ripple}} \approx \frac{V_{\text{out}}\,(1-D)}{2Lf_{\text{sw}}} = \frac{V_{\text{out}}}{2L}\cdot\left(1-\frac{V_{\text{out}}}{V_{\text{in}}}\right)\cdot\frac{1}{f_{\text{sw}}} \quad (1)$$

where V_{in} and V_{out} are the input and output voltage, respectively, f_{sw} is the switching frequency, D is the steady-state duty ratio, and L is the inductor value. A similar expression for the capacitor voltage ripple can also be derived [2]. In conventional designs, the inductor is usually sized based on the minimum allowable ripple for the worst case operating condition, corresponding to the largest *difference between the input and the output* voltages. There, to minimize the filter while maintaining small ripple, operation at higher switching frequencies is usually targeted.

The system in Fig. 1 operates on the fundamental principles introduced in [9]–[11]. Instead of increasing the frequency, the *voltage difference between the input and output of the buck is reduced* allowing filter minimization and, concurrent, reduction of switching losses. In this implementation, a digitally controlled attenuator reduces the voltage difference. It is controlled such that, depending on the input voltage V_g, it sets the ratio $V_{\text{out}}/V_{\text{in}}$ to the value closest to 1, theoretically eliminating the need for the output filter, as seen in (1). For practical reasons, the ratio is adjusted in two discrete steps, still resulting in a significant size reduction.

Compared to the conventional buck, the converter in Fig. 1 practically does not increase the input filter volume. The charge-controlled attenuator is constructed by replacing the input filter capacitor C_{in}, shown in Fig. 1, with two serially connected capacitors with a half of the voltage rating and $2C_{\text{in}}$ capacitance value. Since the volume of the capacitors is primarily determined by its energy storage capability [13], $W_E = 1/2\ \text{CV}^2$, and the total energy in both cases is the same; this modification virtually has no influence on the input filter size.

A. Steady-State Operation

In the system in Fig. 1, during steady state for $V_g > 2V_{\text{out}}$, the attenuated supply voltage $V_{\text{in}} = V_g/2$ is provided to the downstream buck converter, and for $V_g < 2V_{\text{out}}$ the full input voltage $V_{\text{in}} = V_g$ is supplied. This minimizes maximum difference between the input and output voltages, relaxing the worst case operating condition, and, consequently, allowing the output filter minimization.

The attenuator operation for a high-supply voltage can be visualized with the help of Fig. 2 showing its simplified circuit over two consecutive switching periods, where the conduction path is highlighted. During the first period (*mode a*), SW_1 and SW_4 in Fig. 1 are turned ON and the top capacitor is connected to the input of the downstream converter. During the next mode, (*b*/*d*) SW_3 and SW_4 are turned ON and SW_1 and SW_2 are turned OFF, providing a path for the inductor current $i_L(t)$ (equivalent to the operation of a synchronous rectifier (SR) in the conventional buck). Over the following period (*mode c*), SW_2 and SW_3 are conducting and the bottom capacitor provides the current for the converter. Finally, *mode b*/*d* is reactivated and the entire process is repeated.

In this way, rather than using an extra flying capacitor for maintaining the voltage balance of the attenuator taps [9], or a large SC output capacitor [11], the buck inductor is utilized. A consequence of the elimination of an additional capacitor is that the input and output do not share the same ground.

It should be noted that the introduced topology also minimizes the problem of increased conduction losses characteristic for systems combining a capacitive converter and a buck stage [9]–[11], where at least three switches are always present in the conduction path. As discussed in the following section, due to a smaller number of switches and their reduced voltage rating, the conduction losses of the proposed are more comparable to that of a conventional buck.

1) Center-Tap Voltage Regulation: By operating as previously described, ideally, equal average current over the same period of time, i.e., equal charge, is taken from the both attenuator capacitors, resulting in a stable center-tap voltage. However, in practice, this is usually not the case. Due to different losses of the two current loops, mismatches of components, the tap voltages $v_{\text{in1}}(t)$ and $v_{\text{in2}}(t)$ (see Figs. 1 and 2) might diverge in time resulting in unbalanced operating conditions, affecting the output voltage regulation.

To compensate for this, a practical charge control-based algorithm is applied. The algorithm is described with the state diagram in Fig. 3. During each cycle, the center-tap voltage $v_{\text{in2}}(t)$ is compared to one-half of the input voltage using the comparator

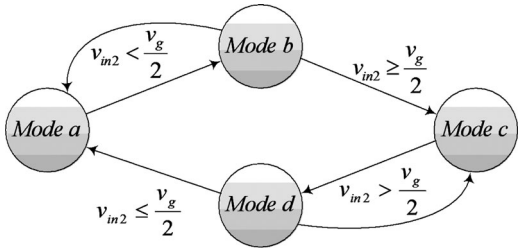

Fig. 3. State-diagram describing operation of the active charge controlled attenuator.

in Fig. 1. When a significant difference between the two voltages is detected, *Charge-sharing regulator*, i.e., state machine in Fig. 3, alters the previously described steady-state operation sequence. Instead of following the regular capacitor discharging pattern, the switching sequence is changed, such that the charge is taken from the capacitor with a higher voltage. In particular, instead of taking the current from the capacitors in alternating fashion, the inductor discharges only the higher voltage capacitor for several cycles, until the voltages are equalized. When the balance is achieved, the regular sequence is resumed. This control scheme simplifies regulation of the center-tap voltage, eliminating the need for a fully dedicated attenuator controller existing in other two-stage systems.

B. Load Transient Operation

Lowering the input voltage of a conventional buck generally reduces the inductor current slew rate during light-to-heavy load transients, negatively affecting the dynamic performance. In the topology of Fig. 1, a comparatively smaller inductor minimizes this effect and, at the same time, improves heavy-to-light load transient response. To further improve dynamics, during light-to-heavy transients, the controller directly connects the input port of the buck stage to V_g, by turning ON SW_1 and SW_2. Thus, compared to the conventional buck, the inductor slew rate is increased by the ratio proportional to the reduction in the inductance value. This is demonstrated in Fig. 4, where the inductances of the conventional buck and the introduced two-stage converter are labeled as $L_{\rm buck}$ and L_{2s}, respectively. To fully utilize the advantages of the reduced inductor, the minimum deviation control method [12] is applied and it is assumed that the same method is used for the conventional buck.

1) Output Capacitor Reduction in the Ideal System: In modern supplies, the output capacitor value is determined based on the voltage deviation during transients rather than on the ripple [1]. For such requirements, the size reduction can be found by comparing the responses of an optimum controller [12] to a step load change, for a conventional buck and the proposed topology, as shown in Fig. 4.

In both cases, the output capacitors are selected such that the same maximum allowable voltage deviation $\Delta v_{\rm max}$ occurs during a maximum load step change, $\Delta I_{\rm max}$. The value of the output capacitance C resulting in a $\Delta v_{\rm max}$ voltage deviation

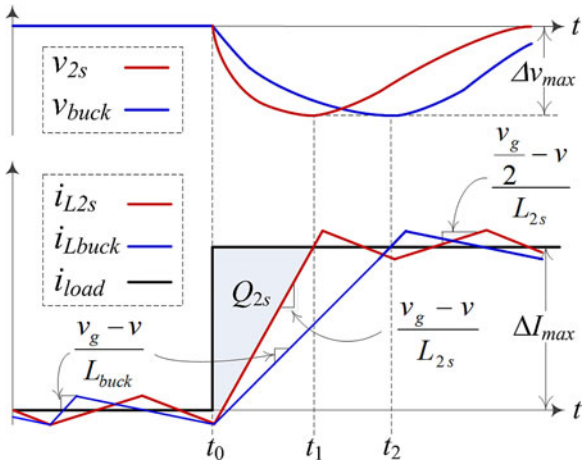

Fig. 4. Idealized transient response waveforms of a conventional buck and the BCMCA (2 s). (Top) AC components of the output voltages. (Bottom) Load and inductor currents.

during transient can be approximately calculated as

$$C \approx \frac{Q}{\Delta v_{\rm max}} = \frac{\Delta I_{\rm max}^2 L}{2\Delta v_{\rm max}\left(V_g - V\right)} \tag{2}$$

where V_g and V are dc values of the buck stage input and output voltages, respectively, and Q is the lost capacitor charge during transient (for the two-stage converter labeled as Q_{2s} in Fig. 4). This equation shows that, ideally, possible reduction of the output capacitor is directly proportional to that of the inductor resulting in a square minimization of the output filter LC product.

III. Practical Design

In a practical two-stage converter in Fig. 1, the maximum allowable reduction of the output capacitor compared to the conventional buck is smaller than what the previously analyzed ideal case predicts. This section gives a more realistic estimation of the output capacitor reduction and also discusses the tradeoff between switching and conduction losses.

A. Selection of the Output Filter Capacitor

Delays between the transient detection and the controller reaction increase the output capacitance. In the presence of a delay t_d, the maximum voltage deviation of a realistic system controlled by a near-optimal controller can be approximated as

$$\Delta v_{\rm max} \approx \frac{\Delta I_{\rm max} t_d}{C} + \frac{\Delta I_{\rm max}^2 L}{2C\left(V_g - V\right)} \tag{3}$$

where the first term on the right-hand side is contribution of the delay, during which the maximum difference between the load and the inductor current is taken from the capacitor. The second term, obtained from (2), is due to the lost capacitor charge. From (3), it can be seen that the delay in the controller reaction has a larger influence on the power stage with a smaller output capacitor not allowing a reduction in C directly proportional to that of L, predicted by the ideal case analysis. Still, as shown in

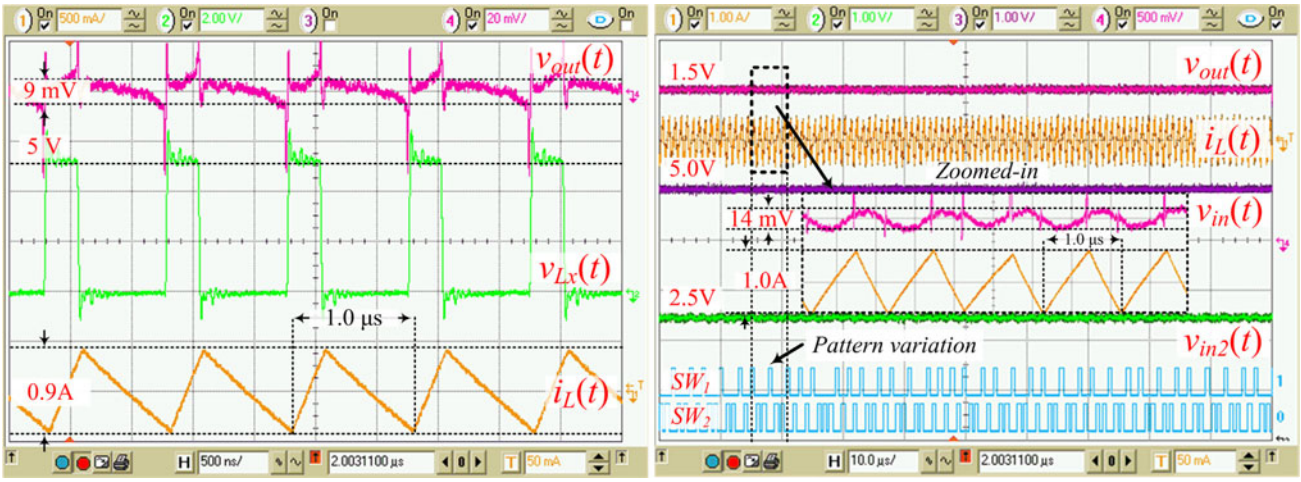

Fig. 5. Steady-state waveforms of (left) the buck converter and (right) BCMCA. For the left waveform, Ch.1: Inductor current $i_L(t)$; Ch.2: Switching node voltage $v_{Lx}(t)$; Ch.4: Output voltage $v_{\rm out}(t)$. For the right waveform, Ch.1: Inductor current $i_L(t)$; Ch.2: Capacitor center-tap voltage $v_{\rm in2}(t)$; Ch.3: Input voltage $v_{\rm in}(t)$; Ch.4: Output voltage $v_{\rm out}(t)$; D0: SW_2 control signal; D1: SW_1 control signal.

the following section, for realistic delays, a significant reduction in the output capacitor value, calculated from (3), is achievable.

B. Efficiency Analysis and Design Tradeoffs

To find losses of the BCMCA and compare them to the conventional buck, the analysis presented in [14] and [15], giving detailed expressions for conduction and switching losses of similar two-stage and single-stage topologies, is used.

Compared to the conventional buck, the BCMCA has lower switching losses, because of reduced transistor blocking voltages [14], [15], as seen from Fig. 2. This reduction comes at the expense of an increased number of switches in the conduction path. However, in an optimized design, where the transistors are constructed to safely sustain only the maximum blocking voltage, the extra switches do not cause a twofold increase in the conduction losses. Since the transistor ON-resistance per unit silicon area [16] is

$$R_{\rm on\_sp} = \alpha \cdot V_B^2 \tag{4}$$

where α is process-dependant constant and V_B is the breakdown voltage, in optimized design, a two times smaller blocking voltage results in the four times smaller resistance for the same area. For the BCMCA, this practically means that SW_3 and SW_4 can be designed such that each of them has a half of the ON-resistance of the conventional buck SR and that their total silicon area is the same as that of the SR. Consequently, the *mode b/d* (see Fig. 2) of the BCMCA does not increase the conduction losses. As far as SW_1 and SW_2 are concerned, in practice, they need to sustain a higher than $\frac{1}{2}v_g(t)$ voltage and, consequently, have a higher total resistance than the main switch (MS) of the buck. This is due to a possible temporary conduction of the body diodes of SW_3 and SW_4 during mode transitions, causing up to 1.2 V [17] increase in the blocking voltage. As a result during *modes a and b*, the conduction losses are slightly increased.

IV. Experimental System and Results

To verify the system, a 5–1.5-V, 2.5-A, 1-MHz experimental prototype based on Figs. 1 and 3 was created and compared to a conventional buck prototype having the same switching frequency and power ratings. The power stages of both prototypes are formed of discrete transistors, gate drivers, and filter components. The controller is based on a field-programmable gate array system and discrete components. To compare the inductor volumes, the inductors from the same production line are selected, such that the current ripple is about a 20% of the rated current. This results in a 1.0-μH (5.1 A/22 mΩ, 3.6 mm $\times$ 3.0 mm $\times$2.0 mm) inductor for the buck and a 0.56 μH (5 A/24 mΩ, 3.6 mm $\times$ 3.0 mm $\times$ 1.2 mm) for the BCMCA, i.e., about 40% reduction. The output capacitors are selected from (2), such that for the maximum load step $\Delta I_{\rm max} = 1.5$ A (exceeding common testing requirements of 50% $I_{\rm max}$ [1]), the voltage deviation is no larger than 50 mV. The capacitances of 14 and 9 μF for the conventional buck and the BCMCA, respectively, are obtained taking into account system delays, which are about 400 ns.

As discussed in the previous section, the BCMCA switches SW_3 and SW_4 are rated for a half of the conventional buck SR blocking voltage. The blocking voltages of SW_1 and SW_2 are larger than optimal ($\frac{1}{2}v_g(t) +$ forward drops of the body diodes), due to limited availability of discrete components. The MS of the conventional buck and $SW_{1/2}$ are identical, blocking the full input voltage.

A. Steady-State and Dynamic Operation

Fig. 5, showing steady-state waveforms of both converters, verifies that the reduction of the inductor has no influence on the current ripple. It can be seen that the ripples of both converters are approximately the same, even though the BCMCA inductor is 44% smaller. It can also be seen that the BCMCA has a larger output voltage ripple, due to the smaller output capacitor. The rms value of this ripple is still significantly smaller than a 1% of the rated output, commonly seen in state-of-the-art solutions [1].

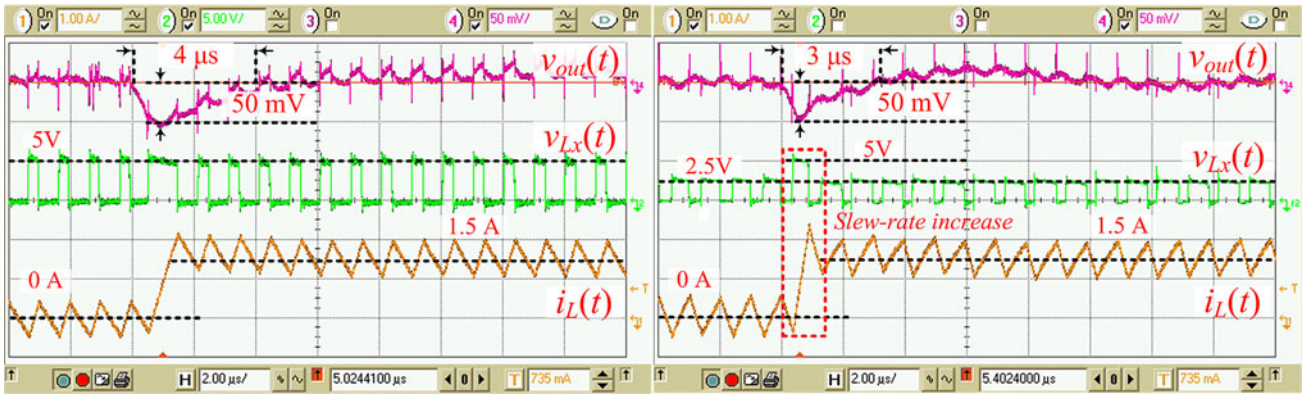

Fig 6. Response to a 1.5-A light-to-heavy load step of (left) the conventional buck and (right) BCMCA. Ch.1: Inductor current $i_L(t)$, 1 A/div; Ch. 2: Buck converter switching node voltage $v_{Lx}(t)$, 5 V/div; Ch. 4: Output voltage $v_{\rm out}(t)$, 50 mV/div-ac; The time scale is 5 μs/div.

Fig. 5 also confirms proper operation of the unified controller (see Fig. 1). Both the center-tap voltage of the capacitive attenuator and the output of the buck are tightly regulated. The figure also demonstrates operation of the charge balance algorithm described in Section II-A1. It can be clearly seen how the switching pattern of SW_1 and SW_2 is varied to maintain a constant center-tap voltage. To eliminate a possible jitter in duty ratio, the *center tap voltage comparator* with a relatively small hysteresis is used. As a result, the voltages of both attenuator capacitors are kept approximately the same and, consequently, no significant difference in the duty ratio during mode transitions (see Figs. 2 and 3) occurs.

In Fig. 6, the responses to a 1.5-A light-to-heavy load step of both systems are compared. In both cases, an optimal control method [12] is applied. It can be seen that the inductor current slew rate of the two-stage converter is increased by applying the full input voltage, i.e., bypassing the attenuator, as described in Section II. The results demonstrate that, although a much smaller output capacitor is used, the BCMCA has the same voltage drop as the conventional buck and about a 25% faster response.

B. Efficiency Comparison

Fig. 7 shows comparison of the efficiency for both converters over the full operating load range as well as a breakdown of the losses. At light-to-medium loads, where the switching losses are dominant, the BCMCA has up to 15% better efficiency. At heavier loads, the reduction in switching losses is partially canceled by increased conduction losses. The increased conduction losses are mostly caused by discrete implementation and, consequent, suboptimal voltage ratings of the transistors SW_1 and SW_2. Still, at the full load, the efficiency of both converters are the same and the higher efficiency of the BCMCA is maintained throughout the entire operating range. The suboptimal discrete implementation also has influence on the other losses of both converters resulting in lower efficiency than that of the integrated solutions [3]. To compare the efficiencies for optimized case, the efficiency of the BCMCA is calculated and plotted in Fig. 7 as well. The calculation is based on the analysis given in [14] and [15] assuming that SW_1 and SW_2 are rated for the

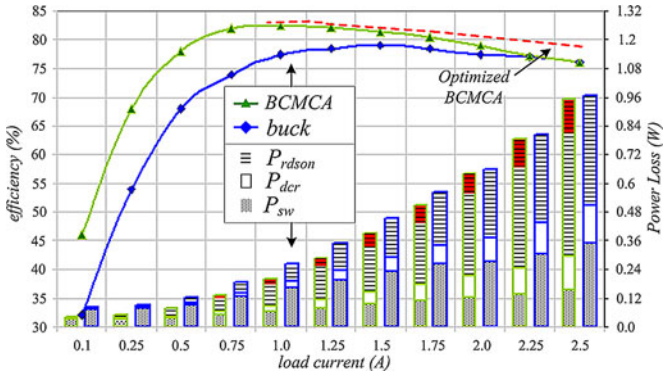

Fig. 7. Efficiency curves and breakdowns of the losses for the conventional buck and the BCMCA (experimental and optimized); $P_{\rm sw}$ indicates switching losses, $P_{\rm drc}$ conduction losses of the inductor, and $P_{\rm rdson}$ conduction losses of the switches.

optimal blocking voltage of 3.7 V, as described in the previous section. The combined resistance of SW_1 and SW_2 case is 42% larger than that of the buck MS [calculated from (4)] for the same silicon area. This can further improve efficiency, as shown in the diagram, and reduce the size of the suboptimal BCMCA prototype, for which both the resistance and silicon area of SW_1 and SW_2 are two times larger than that of the buck MS.

V. Conclusion

The BCMCA introduced here has a smaller output filter and lower switching losses than the conventional buck. The savings are obtained by reducing the difference between the input and output voltage with a capacitive attenuator, whose center-tap voltage is regulated with the buck inductor and a simple digital controller. Consequently, an extra capacitor existing in other systems combining a capacitive converter and an inductor-based power stage is eliminated. The attenuator controller, which is merged with that of the buck, implements a charge-control algorithm where the center-tap voltage is regulated by redirecting the current of the buck inductor. Also, to minimize conduction losses, the switching components of the attenuator and the buck converter are shared and advantages of transistor operating at lower blocking voltages are utilized. Experimental results

comparing the BCMCA with a conventional buck verify smaller volume, better dynamic response, and significantly improved light-to-medium load efficiency.

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